RJK0660DPA
60V, 40A, 5.1mΩ max.
N Channel Power MOS FET
High Speed Power Switching

Features

- High speed switching
- Low drive current
- High density mounting
- Low on-resistance
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PWSN0008DE-A
(Package name: WPAK(3F))

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source voltage</td>
<td>V_{DSS}</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>V_{GSS}</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>Drain current</td>
<td>I_{D}</td>
<td>40</td>
<td>A</td>
</tr>
<tr>
<td>Drain peak current</td>
<td>I_{D(pulse)}</td>
<td>160</td>
<td>A</td>
</tr>
<tr>
<td>Body-drain diode reverse drain current</td>
<td>I_{DR}</td>
<td>40</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>I_{AP}</td>
<td>20</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche energy</td>
<td>E_{AS}</td>
<td>30</td>
<td>mJ</td>
</tr>
<tr>
<td>Channel dissipation</td>
<td>Pch</td>
<td>65</td>
<td>W</td>
</tr>
<tr>
<td>Channel to case thermal impedance</td>
<td>θ_{ch-c}</td>
<td>1.93</td>
<td>°C/W</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>Tch</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td>−55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:
1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C
## Electrical Characteristics

(\(Ta = 25^\circ C\))

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source breakdown voltage</td>
<td>(V_{BRDSS})</td>
<td>60</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>(I_D = 10\ mA, \ V_{GS} = 0\ V)</td>
</tr>
<tr>
<td>Gate to source leak current</td>
<td>(I_{GS})</td>
<td>—</td>
<td>—</td>
<td>(\pm 0.1)</td>
<td>(\mu)A</td>
<td>(V_{GS} = \pm 20\ V, \ V_{DS} = 0\ V)</td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>(I_{DS})</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>(\mu)A</td>
<td>(V_{DS} = 60\ V, \ V_{GS} = 0\ V)</td>
</tr>
<tr>
<td>Gate to source cutoff voltage</td>
<td>(V_{GS(\text{off})})</td>
<td>2.0</td>
<td>—</td>
<td>4.0</td>
<td>V</td>
<td>(V_{DS} = 10\ V, \ I_D = 1\ mA)</td>
</tr>
<tr>
<td>Static drain to source on state resistance</td>
<td>(R_{DS(on)})</td>
<td>—</td>
<td>4.2</td>
<td>5.1</td>
<td>m(\Omega)</td>
<td>(I_D = 20\ A, \ V_{DS} = 10\ V) ^{Note4}</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td>(</td>
<td>Y_{Hs})</td>
<td></td>
<td>—</td>
<td>60</td>
<td>—</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>(C_{iss})</td>
<td>—</td>
<td>3600</td>
<td>—</td>
<td>pF</td>
<td>(V_{DS} = 10\ V, \ V_{GS} = 0\ V, f = 1\ MHz)</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>(C_{oss})</td>
<td>—</td>
<td>830</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>(C_{rss})</td>
<td>—</td>
<td>230</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Gate Resistance</td>
<td>(R_g)</td>
<td>—</td>
<td>1.1</td>
<td>—</td>
<td>(\Omega)</td>
<td></td>
</tr>
<tr>
<td>Total gate charge</td>
<td>(Q_g)</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>nC</td>
<td>(V_{DD} = 25\ V, \ V_{GS} = 10\ V, I_D = 40\ A)</td>
</tr>
<tr>
<td>Gate to source charge</td>
<td>(Q_{gs})</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Gate to drain charge</td>
<td>(Q_{gd})</td>
<td>—</td>
<td>7.5</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>(t_{(on)})</td>
<td>—</td>
<td>18</td>
<td>—</td>
<td>ns</td>
<td>(V_{GS} = 10\ V, I_D = 20\ A, V_{DD} = 30\ V, R_L = 1.5\ \Omega, R_g = 4.7\ \Omega)</td>
</tr>
<tr>
<td>Rise time</td>
<td>(t_r)</td>
<td>—</td>
<td>14</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>(t_{(off)})</td>
<td>—</td>
<td>43</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>(t_f)</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Body–drain diode forward voltage</td>
<td>(V_{DF})</td>
<td>—</td>
<td>0.8</td>
<td>1.1</td>
<td>V</td>
<td>(I_F = 40\ A, \ V_{GS} = 0\ V) ^{Note4}</td>
</tr>
<tr>
<td>Body–drain diode reverse recovery time</td>
<td>(t_r)</td>
<td>—</td>
<td>47</td>
<td>—</td>
<td>ns</td>
<td>(I_F = 40\ A, \ V_{GS} = 0\ V) (di/dt = 100\ A/\mu)s</td>
</tr>
</tbody>
</table>

Notes: 4. Pulse test
Main Characteristics

**Power vs. Temperature Derating**

- Channel Dissipation vs. Case Temperature
  - Channel Dissipation $P_{ch}$ (W)
  - Case Temperature $T_c$ ($^\circ$C)

**Maximum Safe Operation Area**

- Drain to Source Voltage $V_{DS}$ (V)
  - Drain Current $I_D$ (A)

**Typical Output Characteristics**

- Drain to Source Saturation Voltage vs. Gate to Source Voltage
  - $V_{DS_{(on)}}$ (mV)
  - Gate to Source Voltage $V_{GS}$ (V)

**Typical Transfer Characteristics**

- Drain to Source Voltage $V_{DS}$ (V)
  - Drain Current $I_D$ (A)

**Static Drain to Source on State Resistance vs. Drain Current**

- Drain to Source on State Resistance $R_{DS(on)}$ (mΩ)
  - $V_{GS}$ = 10 V
  - Drain Current $I_D$ (A)
Case Temperature $T_c$ (°C)

Static Drain to Source on State Resistance vs. Temperature

Source to Drain Voltage $V_{SD}$ (V)

Reverse Drain Current $I_D$ (A)

Reverse Drain Current vs. Source to Drain Voltage

Channel Temperature $T_{ch}$ (°C)

Avalanche Energy $E_{AS}$ (mJ)

Maximum Avalanche Energy vs. Channel Temperature Derating

Gate Charge $Q_g$ (nC)

Drain to Source Voltage $V_{DS}$ (V)

Gate to Source Voltage $V_{GS}$ (V)

Dynamic Input Characteristics

Typical Capacitance vs. Drain to Source Voltage

Capacitance $C$ (pF)

Pulse Test

Typical Capacitance vs. Source to Drain Voltage

Reversal Drain Current $I_R$ (A)

Source to Drain Voltage $V_{SD}$ (V)

Pulse Test

Maximun Avalanche Energy vs. Channel Temperature Derating

$V_{GS} = 0$ V

$V_{DD} = 50$ V

$V_{DD} = 25$ V

$V_{DD} = 10$ V

$I_D = 40$ A

$I_D = 20$ A

$I_A = 40$ A

$I_D = 20$ A

$duty < 0.1$

$R_g \geq 50$ Ω

$V_{GS} = 10$ V

$V_{GS} = 0$ V

$V_{DD} = 0$ V

$f = 1$ MHz

$C_{ss}$

$C_{oss}$

$C_{rss}$
Normalized Transient Thermal Impedance vs. Pulse Width

Avalanche Test Circuit

V_{DS} Monitor

\[ I_{AP} \]

D. U. T.

R_{g} = \text{60 \, \Omega}

V_{DD}

Vin 15 V

\[ \text{V}_{15 \text{ V}} \]

Switching Time Test Circuit

Vin Monitor

D.U.T.

R_{g}

D.U.T.

R_{L}

\leq 30 \text{ V}

V_{DS}

V_{out} 10 V

\[ \text{V}_{10 \text{ V}} \]

\[ \text{V}_{DS} \]

Avalanche Waveform

\[ E_{AS} = \frac{1}{2} L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}} \]

\[ V_{BRIDSS} \]

Switching Time Waveform

\[ \text{I}_{d} \]

\[ \text{V}_{DS} \]

\[ \text{V}_{DD} \]

V_{in} 10% 90%

V_{out} 10% 90%

t_{d(on)} t_{r} t_{d(off)} t_{f}
### Package Dimensions

<table>
<thead>
<tr>
<th>Package Name</th>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS[Typ.]</th>
<th>Unit: mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>WP(A3F)</td>
<td>—</td>
<td>PHSN0008DE-A</td>
<td>WP(A3F)</td>
<td>0.075g</td>
<td></td>
</tr>
</tbody>
</table>

![Package Dimensions Diagram]

*Notice: The reverse pattern of die-pad support lead described above exists.*

### Ordering Information

<table>
<thead>
<tr>
<th>Orderable Part No.</th>
<th>Quantity</th>
<th>Shipping Container</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJK0660DPA-00-J5A</td>
<td>3000 pcs</td>
<td>Taping</td>
</tr>
</tbody>
</table>

Note: The symbol of 2nd "-" is occasionally presented as ":#".
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