RJK0455DPB
40V, 45A, 3.8mΩ max.
Silicon N Channel Power MOS FET
Power Switching

Features
- High speed switching
- Low drive current
- Low on-resistance
  \( R_{DS(ON)} = 3.1 \text{ mΩ typ. (at } V_{GS} = 10 \text{ V) } \)
- Pb-free
- Halogen-free
- High density mounting

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source voltage</td>
<td>( V_{DSS} )</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>( V_{GSS} )</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>Drain current</td>
<td>( I_D )</td>
<td>45</td>
<td>A</td>
</tr>
<tr>
<td>Drain peak current</td>
<td>( I_D(\text{pulse}) )</td>
<td>180</td>
<td>A</td>
</tr>
<tr>
<td>Body-drain diode reverse drain current</td>
<td>( I_{DR} )</td>
<td>45</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>( I_{AP} )</td>
<td>45</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche energy</td>
<td>( E_{AB} )</td>
<td>16</td>
<td>mJ</td>
</tr>
<tr>
<td>Channel dissipation</td>
<td>( P_{ch} )</td>
<td>60</td>
<td>W</td>
</tr>
<tr>
<td>Channel to Case Thermal Resistance</td>
<td>( \theta_{ch-C} )</td>
<td>2.08</td>
<td>°C/W</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>( T_{ch} )</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>( T_{stg} )</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:
1. \( PW \leq 10 \mu s, \text{ duty cycle } \leq 1\% \)
2. Value at \( L=10\mu H, T_{ch} = 25^\circ C, R_{g} \geq 50 \Omega \)
3. \( T_{c} = 25^\circ C \)
## Electrical Characteristics

(Ta = 25°C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source breakdown voltage</td>
<td>V(BR)DSS</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>IO = 10 mA, VG = 0 V</td>
</tr>
<tr>
<td>Gate to source leak current</td>
<td>IGSS</td>
<td>—</td>
<td>—</td>
<td>±0.1</td>
<td>µA</td>
<td>VG = ±20 V, VDS = 0 V</td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>IDSS</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>µA</td>
<td>VDS = 40 V, VG = 0 V</td>
</tr>
<tr>
<td>Gate to source cutoff voltage</td>
<td>VGSOFF</td>
<td>2.0</td>
<td>—</td>
<td>4.0</td>
<td>V</td>
<td>VDS = 10 V, IO = 1 mA</td>
</tr>
<tr>
<td>Static drain to source on state resistance</td>
<td>RDS(on)</td>
<td>—</td>
<td>3.1</td>
<td>3.8</td>
<td>mΩ</td>
<td>IO = 22.5 A, VG = 10 V</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td></td>
<td>—</td>
<td>52</td>
<td>—</td>
<td>S</td>
<td>IO = 22.5 A, VG = 10 V</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>Ciss</td>
<td>—</td>
<td>2550</td>
<td>—</td>
<td>pF</td>
<td>VDS = 10 V, VG = 0 V, f = 1 MHz</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>Coss</td>
<td>—</td>
<td>760</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>Crss</td>
<td>—</td>
<td>210</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Gate Resistance</td>
<td>Rg</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Total gate charge</td>
<td>Qg</td>
<td>—</td>
<td>34</td>
<td>—</td>
<td>nC</td>
<td>VDD = 10 V, VG = 10 V, IO = 45 A</td>
</tr>
<tr>
<td>Gate to source charge</td>
<td>Qgs</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Gate to drain charge</td>
<td>Qgd</td>
<td>—</td>
<td>4.5</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>t(on)</td>
<td>—</td>
<td>12</td>
<td>—</td>
<td>ns</td>
<td>VG = 10 V, IO = 22.5 A, VDD = 10 V, RL = 0.4 Ω, Rg = 4.7 Ω</td>
</tr>
<tr>
<td>Rise time</td>
<td>tr</td>
<td>—</td>
<td>6.0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>t(off)</td>
<td>—</td>
<td>32</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>tf</td>
<td>—</td>
<td>7.2</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Body–drain diode forward voltage</td>
<td>VDF</td>
<td>—</td>
<td>0.8</td>
<td>1.1</td>
<td>V</td>
<td>IF = 45 A, VG = 0 V</td>
</tr>
<tr>
<td>Body–drain diode reverse recovery time</td>
<td>tr</td>
<td>—</td>
<td>39</td>
<td>—</td>
<td>ns</td>
<td>IF = 45 A, VG = 0 V, di/I/dt = 100 A/µs</td>
</tr>
</tbody>
</table>

Notes: 4. Pulse test
Main Characteristics

Power vs. Temperature Derating

Channel Dissipation, Pch (W)

Case Temperature, Tc (°C)

Drain to Source Voltage, VDS (V)

Drain Current, ID (A)

Maximum Safe Operation Area

Drain to Source Voltage, VDS (V)

Drain Current, ID (A)

Operation in this area is limited by RDS(on)

DC Operation

Typical Output Characteristics

Drain Current, ID (A)

Drain to Source Voltage, VDS (V)

Typical Transfer Characteristics

Gate to Source Voltage, VGS (V)

Typical Transfer Characteristics

Static Drain to Source on State Resistance vs. Drain Current

Drain to Source Saturation Voltage vs. Gate to Source Voltage

Drain to Source Saturation Voltage, VDS(on) (mV)

Gate to Source Voltage, VGS (V)

Pulse Test

VGS = 3.4 V

VDS = 10 V

Pulse Test

ID = 20 A

VGS = 4.0 V

Tc = 25°C

Operation in this area is limited by RDS(on)

Tc = 75°C

Tc = 25°C

-25°C

Tc = 75°C

Static Drain to Source on State Resistance

Drain to Source on State Resistance, RDS(on) (mΩ)

Drain Current, ID (A)

Pulse Test

VGS = 10 V

Pulse Test

VGS = 3.8 V

PW = 10 ms

10 µs
Avalanche Test Circuit

Avalanche Waveform

\[
E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}
\]

Switching Time Test Circuit

Switching Time Waveform
**Package Dimensions**

<table>
<thead>
<tr>
<th>Package Name</th>
<th>JETTA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS[Typ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPPAK</td>
<td>SC-100</td>
<td>P12Z0050DA-A</td>
<td>LPPARV</td>
<td>0.080g</td>
</tr>
</tbody>
</table>

Unit: mm

![ dimension diagram]

(Ni/Pd/Au plating)

**Ordering Information**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Quantity</th>
<th>Shipping Container</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJK0455DPB-00-J5</td>
<td>2500 pcs</td>
<td>Taping</td>
</tr>
</tbody>
</table>
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