Description
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features
- Logic level operation (4 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101 Compliant
- High endurance capability against to ESD.

Outline

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source voltage</td>
<td>$V_{DSS}$</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>$V_{GSS}$</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>$V_{GSS}$</td>
<td>–2.5</td>
<td>V</td>
</tr>
<tr>
<td>Drain current</td>
<td>$I_D$ Note 3</td>
<td>30</td>
<td>A</td>
</tr>
<tr>
<td>Body-drain diode reverse drain current</td>
<td>$I_D_R$ Note 4</td>
<td>30</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>$I_{AP}$ Note 2</td>
<td>6.7</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche energy</td>
<td>$E_{AR}$ Note 2</td>
<td>192</td>
<td>mJ</td>
</tr>
<tr>
<td>Channel dissipation</td>
<td>$P_{ch}$ Note 1</td>
<td>50</td>
<td>W</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>$T_{ch}$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>–55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:
1. Value at $T_c = 25$°C
2. $T_{ch} = 25$°C, $R_g \geq 50$ Ω
3. It provides by the current limitation lower bound value.
### Typical Operation Characteristics

**Item** | Symbol | Min | Typ | Max | Unit | Test Conditions
---|---|---|---|---|---|---
Input voltage | $V_{IH}$ | 3.5 | — | — | V | 
Input voltage | $V_{IL}$ | — | — | 1.2 | V | 
Input current (Gate non shut down) | $I_{IH1}$ | — | — | 100 | $\mu$A | $V_i = 8 \text{ V}, V_{DS} = 0$
Input current (Gate non shut down) | $I_{IH2}$ | — | — | 50 | $\mu$A | $V_i = 3.5 \text{ V}, V_{DS} = 0$
Input current (Gate non shut down) | $I_{IL}$ | — | — | 1 | $\mu$A | $V_i = 1.2 \text{ V}, V_{DS} = 0$
Input current (Gate shut down) | $I_{IH(sd)1}$ | — | 0.8 | — | mA | $V_i = 8 \text{ V}, V_{DS} = 0$
Input current (Gate shut down) | $I_{IH(sd)2}$ | — | 0.35 | — | mA | $V_i = 3.5 \text{ V}, V_{DS} = 0$
Shut down temperature | $T_{sd}$ | — | 175 | — | °C | Channel temperature
Gate operation voltage | $V_{op}$ | 3.5 | — | — | V | 
Drain current (Current limitation value) | $I_{D limt}$ | 30 | — | — | A | $V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$

Note: 4. Pulse test

### Electrical Characteristics

**Item** | Symbol | Min | Typ | Max | Unit | Test Conditions
---|---|---|---|---|---|---
Drain current | $I_{D1}$ | — | — | 45 | A | $V_{GS} = 3.5 \text{ V}, V_{DS} = 10 \text{ V}$
Drain current | $I_{D2}$ | — | — | 10 | mA | $V_{GS} = 1.2 \text{ V}, V_{DS} = 10 \text{ V}$
Drain current | $I_{D3}$ | 30 | — | — | A | $V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$
Drain to source breakdown voltage | $V_{(BR)DSS}$ | 60 | — | — | V | $I_{D} = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage | $V_{(BR)GSS}$ | 16 | — | — | V | $I_{G} = 800 \text{ mA}, V_{DS} = 0$
Gate to source breakdown voltage | $V_{(BR)GSS}$ | — | — | 2.5 | V | $I_{G} = -100 \text{ mA}, V_{DS} = 0$
Gate to source leak current | $I_{GS1}$ | — | — | 100 | $\mu$A | $V_{GS} = 8 \text{ V}, V_{DS} = 0$
Gate to source leak current | $I_{GS2}$ | — | — | 50 | $\mu$A | $V_{GS} = 3.5 \text{ V}, V_{DS} = 0$
Gate to source leak current | $I_{GS3}$ | — | — | 1 | $\mu$A | $V_{GS} = 1.2 \text{ V}, V_{DS} = 0$
Gate to source leak current | $I_{GS4}$ | — | — | -100 | $\mu$A | $V_{GS} = -2.4 \text{ V}, V_{DS} = 0$
Input current (shut down) | $I_{GS(OP)1}$ | — | 0.8 | — | mA | $V_{GS} = 8 \text{ V}, V_{DS} = 0$
Input current (shut down) | $I_{GS(OP)2}$ | — | 0.35 | — | mA | $V_{GS} = 3.5 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current | $I_{DS}$ | — | — | 10 | $\mu$A | $V_{DS} = 32 \text{ V}, V_{DS} = 0, T_c = 110 \text{ °C}$
Gate to source cutoff voltage | $V_{G(S)off}$ | 1.1 | — | 2.1 | V | $V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ mA}$
Forward transfer admittance | $|y_{fs}|$ | 12 | 27 | — | S | $I_{D} = 15 \text{ A}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance | $R_{DS(on)}$ | — | 33 | 40 | $\Omega$ | $I_{D} = 15 \text{ A}, V_{GS} = 4 \text{ V}$
Static drain to source on state resistance | $R_{DS(on)}$ | — | 25 | 30 | $\Omega$ | $I_{D} = 15 \text{ A}, V_{GS} = 10 \text{ V}$
Output capacitance | $C_{oss}$ | — | 523 | — | pF | $V_{DS} = 10 \text{ V}, I_{D} = 15 \text{ A}, f = 1 \text{ MHz}$
Turn-on delay time | $t_{(on)}$ | — | 3.8 | — | $\mu$s | $V_{GS} = 10 \text{ V}, I_{D} = 15 \text{ A}, R_{L} = 2 \text{ $\Omega$}$
Rise time | $t_{r}$ | — | 13.5 | — | $\mu$s | 
Turn-off delay time | $t_{(off)}$ | — | 4.1 | — | $\mu$s | 
Fall time | $t_{f}$ | — | 7.3 | — | $\mu$s | 
Body-drain diode forward voltage | $V_{DF}$ | — | 0.9 | — | V | $I_{C} = 30 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time | $t_{re}$ | — | 110 | — | ns | $I_{C} = 30 \text{ A}, V_{GS} = 0$ 
Over load shut down operation time | $t_{st}$ | — | 0.34 | — | ms | $V_{GS} = 5 \text{ V}, V_{DD} = 16 \text{ V}$

Notes: 6. Pulse test
6. Including the junction temperature rise of the over loaded condition.
Main Characteristics

Power vs. Temperature Derating

Maximum Safe Operation Area

Typical Output Characteristics

Typical Transfer Characteristics

Drain to Source Saturation Voltage vs. Gate to Source Voltage

Static Drain to Source on State Resistance vs. Drain Current
Static Drain to Source on State Resistance vs. Temperature

- Pulse Test
  - $I_D = 15 \, A$
  - $I_D = 10 \, A$
  - $I_D = 5 \, A$
  - $V_{GS} = 4 \, V$
  - $V_{GS} = 10 \, V$

Case Temperature $T_c \, (^{\circ}C)$

Body-Drain Diode Reverse Recovery Time

- $V_{DS} = 10 \, V$
- $T_c = -40 \, ^{\circ}C$
- $25 \, ^{\circ}C$
- $150 \, ^{\circ}C$

Forward Transfer Admittance vs. Drain Current

- $V_{DS} = 10 \, V$
- $V_{DD} = 30 \, V$
- $PW = 300 \, \mu s$
- duty $\leq 1 \%$

Switching Characteristics

- $V_{GS} = 0$
- $f = 1 \, MHz$

- $C_{oss}$
  - $V_{GS} = 0$
  - $f = 1 \, MHz$

- $V_{DS} = 0$
  - $f = 1 \, MHz$
### Switching Time Test Circuit

![Switching Time Test Circuit Diagram](image)

- **Vin Monitor**: 10 V
- **D.U.T.**: 50 Ω
- **R_L**: 50 Ω
- **V_DDD**: 30 V

### Waveform

- **Vin**: 10% 90%
- **Vout**: 10% 90%
- **t_d(on)**
- **t_d(off)**
- **t_f**

### Avalanche Test Circuit

![Avalanche Test Circuit Diagram](image)

- **Vin**: 10 V
- **R_g**: 50 Ω
- **IAP Monitor**: L
- **V_DS Monitor**: L

### Avalanche Waveform

- **E_AR** = \( \frac{1}{2} \) \( L \cdot I_{AP}^2 \) \( \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}} \)
- **V_{BRDSS}**: V_{DSS}
- **I_{AP}**: I_D
- **V_{DD}**: 0
Package Dimensions

<table>
<thead>
<tr>
<th>Package Name</th>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MAS[S]Typ.</th>
<th>Unit: mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDPAR(5)[17]</td>
<td>SC/RJ</td>
<td>PRRS0000AE-B</td>
<td>LDPAR(17)/PRL024(Y)</td>
<td>1.30g</td>
<td></td>
</tr>
</tbody>
</table>

ordering Information

<table>
<thead>
<tr>
<th>Orderable Part Number</th>
<th>Quantity</th>
<th>Shipping Container</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJF0619JPE-00-J3</td>
<td>1000 pcs</td>
<td>Taping</td>
</tr>
</tbody>
</table>

Note: The symbol of 2nd "." is occasionally presented as ".#".
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