Description
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features
- Logic level operation.
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V.
- AEC-Q101 Compliant

Outline

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source voltage</td>
<td>VDSS</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>VGSS</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>VGSS</td>
<td>–2.5</td>
<td>V</td>
</tr>
<tr>
<td>Drain current</td>
<td>ID</td>
<td>40</td>
<td>A</td>
</tr>
<tr>
<td>Body-drain diode reverse drain current</td>
<td>IoR</td>
<td>40</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>IAP</td>
<td>12</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche energy</td>
<td>EAR</td>
<td>960</td>
<td>mJ</td>
</tr>
<tr>
<td>Channel dissipation</td>
<td>Pch</td>
<td>100</td>
<td>W</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>Tch</td>
<td>150</td>
<td>ºC</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td>–55 to +150</td>
<td>ºC</td>
</tr>
</tbody>
</table>

Notes: 1. Value at Ta = 25°C
2. Tch = 25°C, Rg ≥ 50 Ω
3. It provides by the current limitation lower bound value.
### Typical Operation Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
</table>
| Input voltage                     |        |      |      |      |      | ![Image](image)
| (Gate non shut down)              |        |      |      |      |      | ![Image](image)
| Input current                     |        |      |      |      |      | ![Image](image)
| (Gate shut down)                  |        |      |      |      |      | ![Image](image)
| Shut down temperature             |        |      |      |      |      | ![Image](image)
| Gate operation voltage            | Vop    | 3.5  | —    | —    | V    | ![Image](image)
| Drain current (Current limitation value) | I_Dlim | 40   | —    | —    | A    | ![Image](image)

Notes: 4. Pulse test

### Electrical Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
</table>
| Drain current                     | I_D1   | —    | —    | 74   | A    | V_GS = 3.5 V, V_DS = 10 V ![Image](image)
| Drain to source breakdown voltage | V(BR)DSS | 40   | —    | —    | V    | I_D = 10 mA, V_GS = 0 ![Image](image)
| Gate to source breakdown voltage  | V(BR)GSS | 16   | —    | —    | V    | I_D = 800 μA, V_DS = 0 ![Image](image)
| Gate to source leak current       | I_GS1  | —    | —    | 100  | μA   | V_GS = 8 V, V_DS = 0 ![Image](image)
| Gate to source leak current       | I_GS2  | —    | —    | 50   | μA   | V_GS = 3.5 V, V_DS = 0 ![Image](image)
| Gate to source leak current       | I_GS3  | —    | —    | 1    | μA   | V_GS = 1.2 V, V_DS = 0 ![Image](image)
| Gate to source leak current       | I_GS4  | —    | —    | —100 | μA   | V_GS = –2.4 V, V_DS = 0 ![Image](image)
| Input current (shut down)         | I_GS(OP1) | 0.8  | —    | —    | mA   | V_GS = 8 V, V_DS = 0 ![Image](image)
| Zero gate voltage drain current   | I_DSS  | —    | —    | 10   | μA   | V_DS = 32 V, V_GS = 0, Tc = 110°C ![Image](image)
| Gate to source cutoff voltage     | V_GS(off) | 1.1  | —    | 2.1  | V    | V_DS = 10 V, I_D = 1 mA ![Image](image)
| Forward transfer admittance       | | 20   | 46   | —    | S    | I_D = 20 A, V_DS = 10 V ![Image](image)
| Static drain to source on state resistance | R_DSS(on) | 11.3 | 15   | mΩ   | I_D = 20 A, V_DS = 5 V ![Image](image)
| Output capacitance                | Coss   | 1098 | —    | —    | pF   | V_DS = 10 V, V_GS = 0, f = 1MHz ![Image](image)
| Turn-on delay time                | t_d(on) | 24.7 | —    | —    | μs   | V_GS = 10 V, I_D= 20 A, R_L = 1.5 Ω ![Image](image)
| Rise time                         | t_r     | 99.3 | —    | —    | μs   | ![Image](image)
| Turn-off delay time               | t_d(off) | 7.44 | —    | —    | μs   | ![Image](image)
| Fall time                         | t_f     | 13.3 | —    | —    | μs   | ![Image](image)
| Body-drain diode forward voltage  | V_DF    | 0.9  | —    | —    | V    | I_F = 40 A, V_GS = 0 ![Image](image)
| Body-drain diode reverse recovery time | t_r     | 122  | —    | —    | ns   | I_F = 40 A, V_GS = 0 ![Image](image)
| Over load shut down operation time | t_DSS1 | 0.63 | —    | —    | ms   | V_GS = 5 V, V_DD = 16 V ![Image](image)

Notes: 5. Pulse test
6. Including the junction temperature rise of the over loaded condition.
Main Characteristics

- **Power vs. Temperature Derating**
  - Channel Dissipation vs. Case temperature (Tc °C)

- **Maximum Safe Operation Area**
  - Drain to Source Voltage (VDS (V)) vs. Drain Current (ID (A))

- **Typical Output Characteristics**
  - Drain Current (ID (A)) vs. Drain to Source Voltage (VDS (V))
  - Drain to Source Saturation Voltage vs. Gate to Source Voltage

- **Typical Transfer Characteristics**
  - Drain Current (ID (A)) vs. Gate to Source Voltage (VGS (V))

- **Static Drain to Source State Resistance**
  - Drain Source On State Resistance (RDS(on) (mΩ)) vs. Drain Current (ID (A))

- **Pulse Test**
  - Operation with VDS = 10 V, PW = 10 ms
Gate to Source Voltage vs. Shutdown Time of Load-Short Test

Shutdown Case Temperature vs. Gate to Source Voltage

Normalized Transient Thermal Impedance vs. Pulse Width
Avalanche Test Circuit

\[ E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{BRIDSS}}{V_{BRIDSS} - V_{DD}} \]

Avalanche Waveform

Switching Time Test Circuit

\[ V_{DS} \]

\[ I_{AP} \]

\[ V_{DD} \]

\[ 0 \]

\[ V_{DD} \]

\[ V_{BRIDSS} \]

\[ I_{D} \]

Vin Monitor

D.U.T.

R\(_L\)

Vout Monitor

Vin

50 \(\Omega\)

10 V

Vout

10 V

RL

VDD

\( \geq \) 30 V

ID

VDS Monitor

IAP Monitor

Vin

10 V

Rg

50 \(\Omega\)

D.U.T.

\[ V_D \]

td(on)

td(off)

\( t \)

Vin

10%

10%

90%

90%

10%

10%

Vout

90%
Package Dimensions

<table>
<thead>
<tr>
<th>Package Name</th>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS[Typ.]</th>
<th>Unit: mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDPAK(S)-(1)</td>
<td>8C-EJ</td>
<td>PRS3000ARE-B</td>
<td>JP4035(T1)</td>
<td>1.30g</td>
<td></td>
</tr>
</tbody>
</table>

Ordering Information

<table>
<thead>
<tr>
<th>Orderable Part Number</th>
<th>Quantity</th>
<th>Shipping Container</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJF0410JPE-00-J3</td>
<td>1000 pcs</td>
<td>Taping</td>
</tr>
</tbody>
</table>

Note: The symbol of 2nd "-" is occasionally presented as "#."
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