

RJE0605JPD

Silicon P Channel MOS FET Series
Power Switching

REJ03G1803-0100
Rev.1.00
Apr 01, 2010

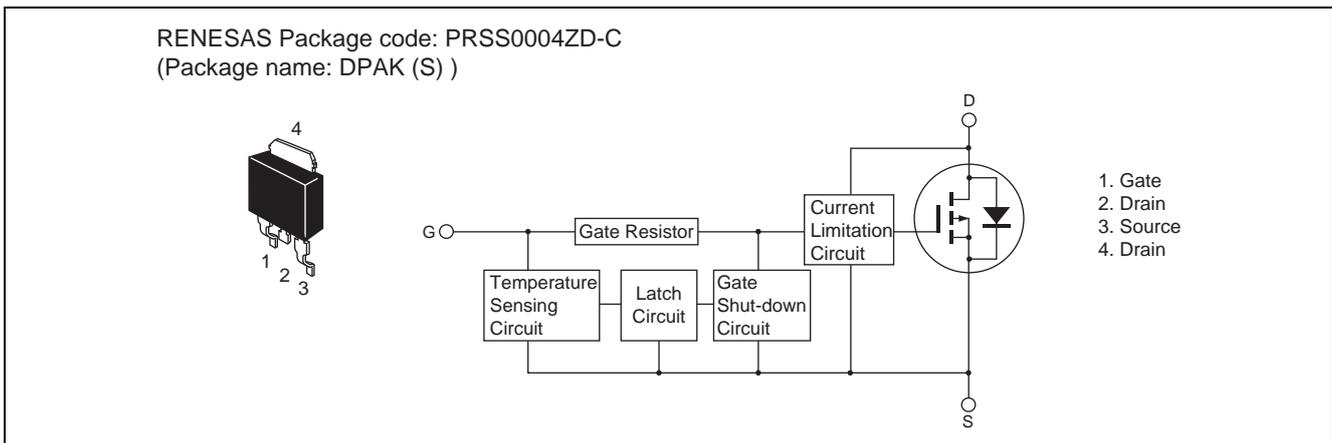
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (–6 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Low on-resistance $R_{DS(on)}$: 58 mΩ Typ, 75 mΩ Max ($V_{GS} = -10$ V)

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	-16	V
Gate to source voltage	V_{GSS}	2.5	V
Drain current	I_D ^{Note 3}	-10	A
Body-drain diode reverse drain current	I_{DR}	-10	A
Avalanche current	I_{AP} ^{Note 2}	-7	A
Avalanche energy	E_{AR} ^{Note 2}	210	mJ
Channel dissipation	P_{ch} ^{Note 1}	30	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 +150	$^\circ\text{C}$

- Notes: 1. Value at $T_c = 25^\circ\text{C}$
 2. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	-3.5	—	—	V	
	V _{IL}	—	—	-1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	-100	μA	V _i = -8 V, V _{DS} = 0
	I _{IH2}	—	—	-50	μA	V _i = -3.5 V, V _{DS} = 0
	I _{IL}	—	—	-1	μA	V _i = -1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	-0.8	—	mA	V _i = -8 V, V _{DS} = 0
	I _{IH(sd)2}	—	-0.35	—	mA	V _i = -3.5 V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature (dv/dt V _{GS} ≥ 500 V/ms)
Gate operation voltage	V _{op}	-3.5	—	-12	V	
Drain current (Current limitation value)	I _{D limit}	-10	—	—	A	V _{GS} = -12 V, V _{DS} = -10 V ^{Note 4}

Notes; 4. Pulse test

Electrical Characteristics

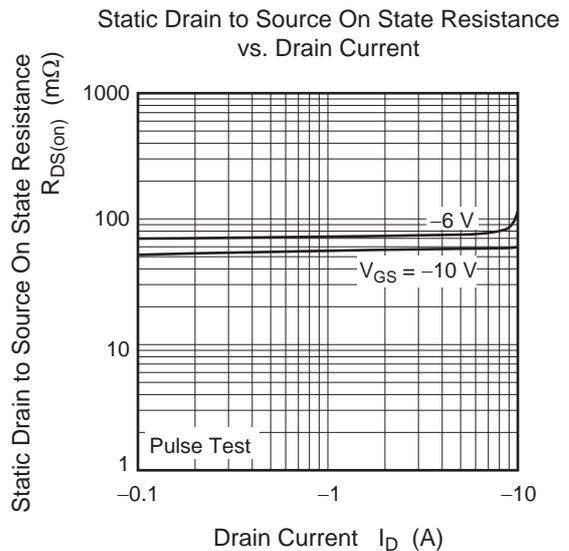
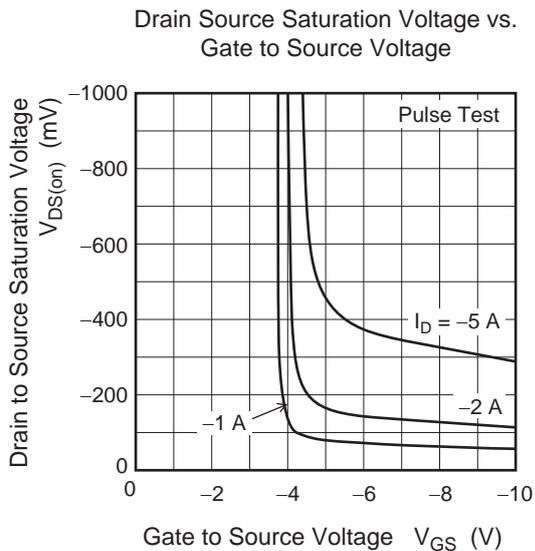
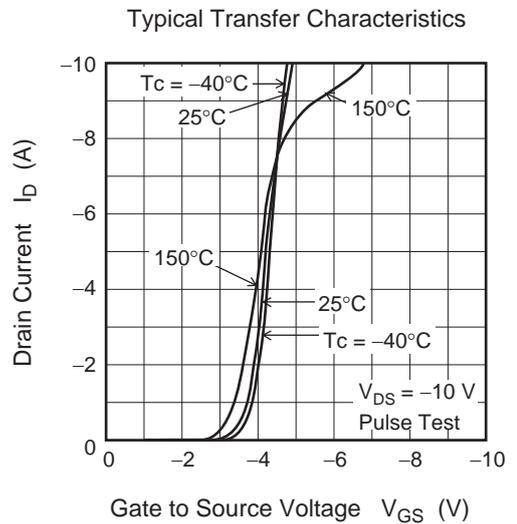
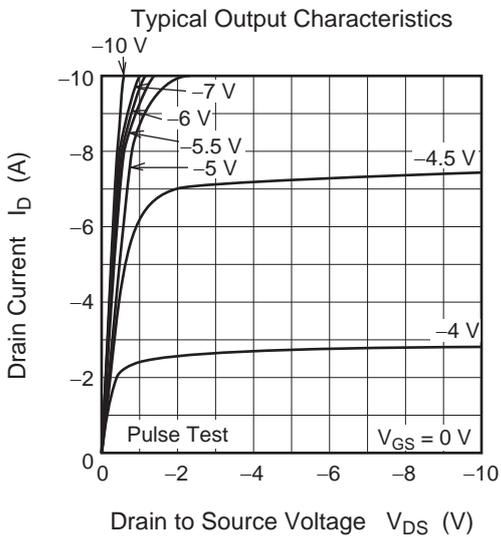
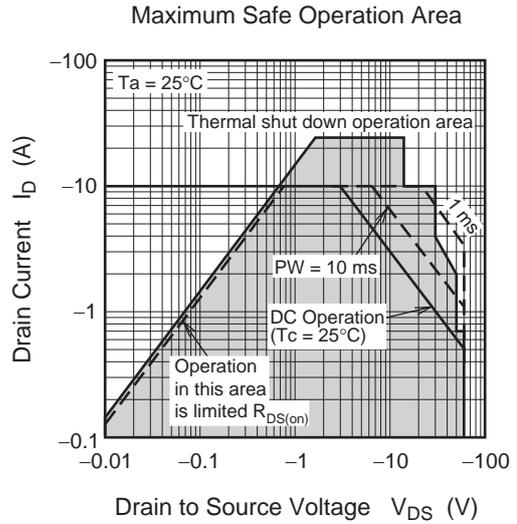
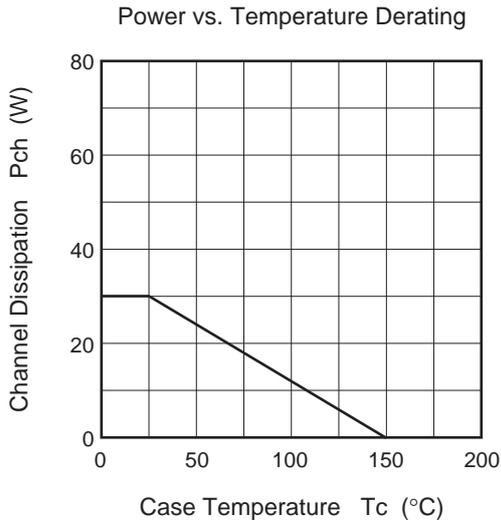
(Ta = 25°C)

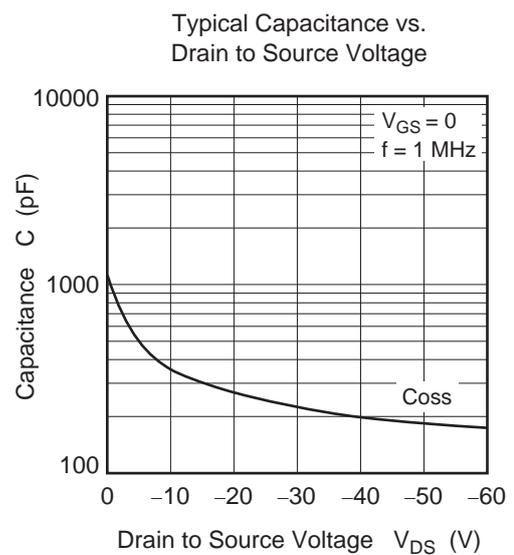
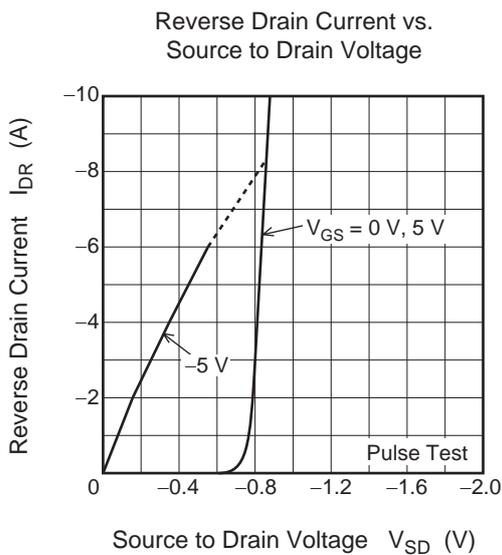
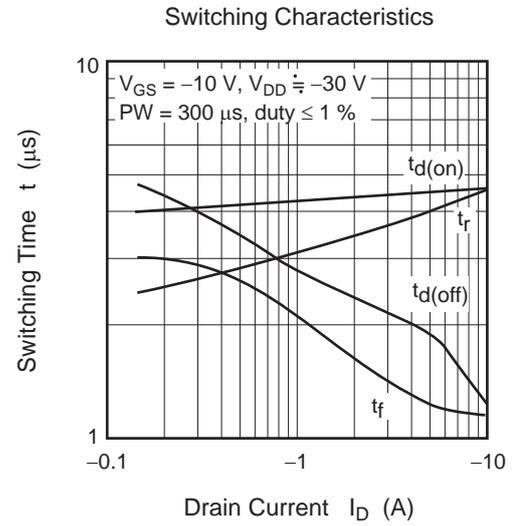
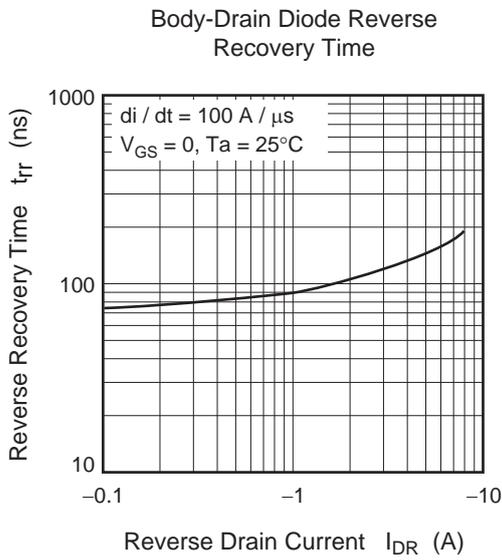
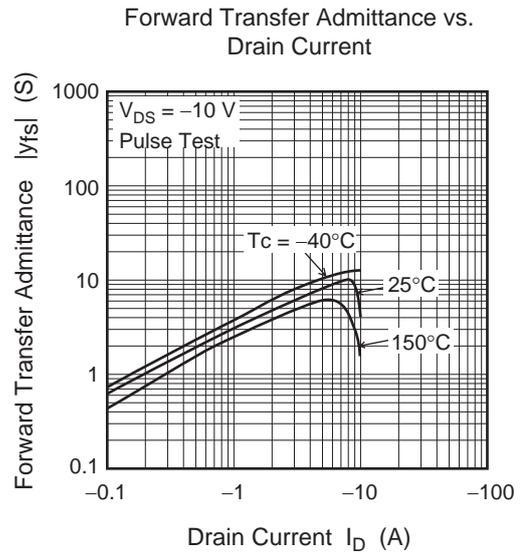
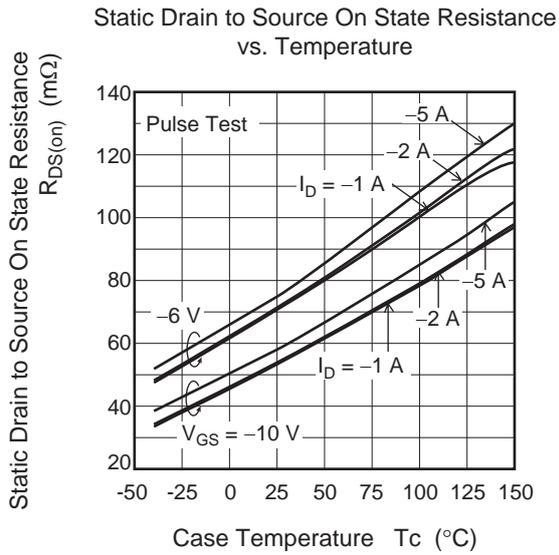
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	—	—	-4	A	V _{GS} = -3.5 V, V _{DS} = -10 V
	I _{D2}	—	—	-10	mA	V _{GS} = -1.2 V, V _{DS} = -10 V
	I _{D3}	-10	—	—	A	V _{GS} = -12 V, V _{DS} = -10 V ^{Note 5}
Drain to source breakdown voltage	V _{(BR)DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	-16	—	—	V	I _G = -800 μA, V _{DS} = 0
	V _{(BR)GSS}	2.5	—	—	V	I _G = 100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	-100	μA	V _{GS} = -8 V, V _{DS} = 0
	I _{GSS2}	—	—	-50	μA	V _{GS} = -3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	-1	μA	V _{GS} = -1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	100	μA	V _{GS} = 2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	-0.8	—	mA	V _{GS} = -8 V, V _{DS} = 0
	I _{GS(OP)2}	—	-0.35	—	mA	V _{GS} = -3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	-2.2	—	-3.4	V	V _{DS} = -10 V, I _D = -1 mA
Forward transfer admittance	y _{fs}	4	8	—	S	I _D = -5 A, V _{DS} = -10 V ^{Note 5}
Static drain to source on state resistance	R _{DS(on)}	—	75	110	mΩ	I _D = -5 A, V _{GS} = -6 V ^{Note 5}
	R _{DS(on)}	—	58	75	mΩ	I _D = -5 A, V _{GS} = -10 V ^{Note 5}
Output capacitance	C _{oss}	—	355	—	pF	V _{DS} = -10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	4.5	—	μs	V _{GS} = -10 V, I _D = -5 A, R _L = 6 Ω
Rise time	t _r	—	4.0	—	μs	
Turn-off delay time	t _{d(off)}	—	1.8	—	μs	
Fall time	t _f	—	1.3	—	μs	
Body-drain diode forward voltage	V _{DF}	—	0.87	—	V	I _F = -10 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	209	—	ns	I _F = -10 A, V _{GS} = 0 di _F /dt = 50 A/μs
Over load shut down operation time ^{Note 6}	t _{os1}	—	2.3	—	ms	V _{GS} = -6 V, V _{DD} = -16 V

Notes: 5. Pulse test

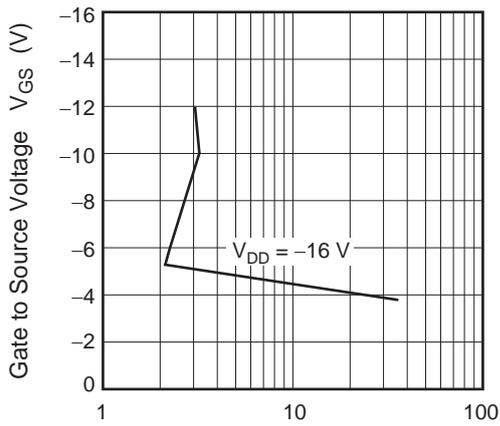
6. Including the junction temperature rise of the over loaded condition.

Main Characteristics



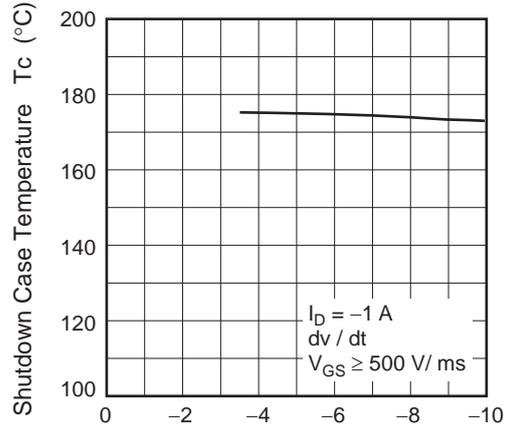


Gate to Source Voltage vs. Shutdown Time of Load-Short Test



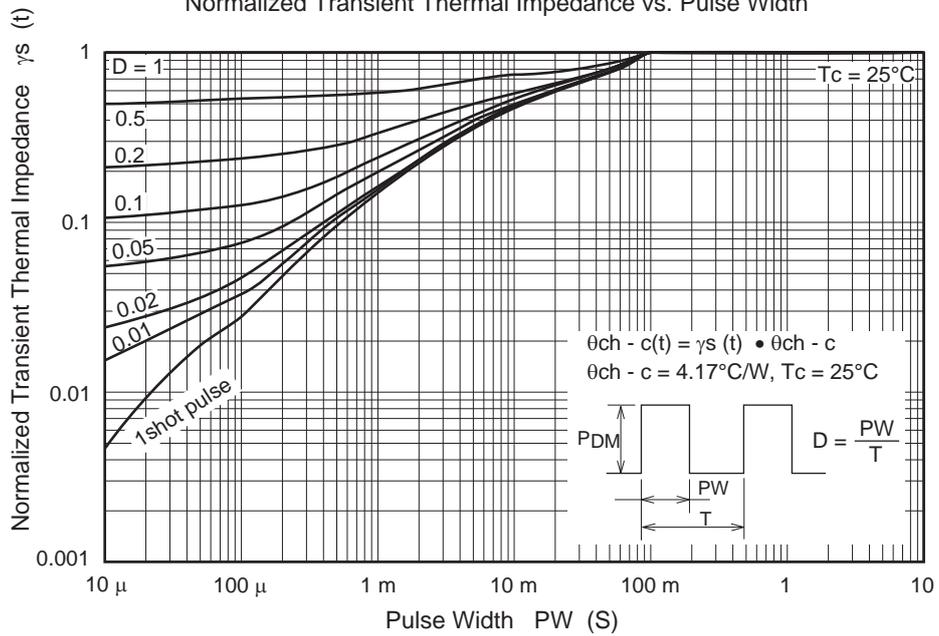
Shutdown Time of Load-Short Test P_w (ms)

Shutdown Case Temperature vs. Gate to Source Voltage

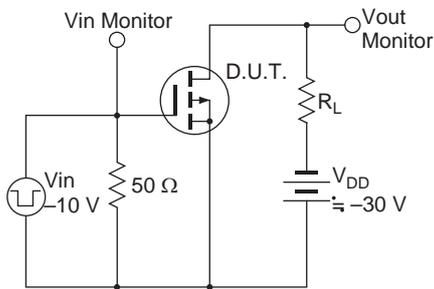


Gate to Source Voltage V_{GS} (V)

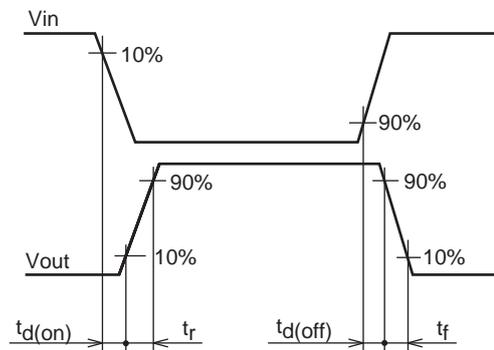
Normalized Transient Thermal Impedance vs. Pulse Width



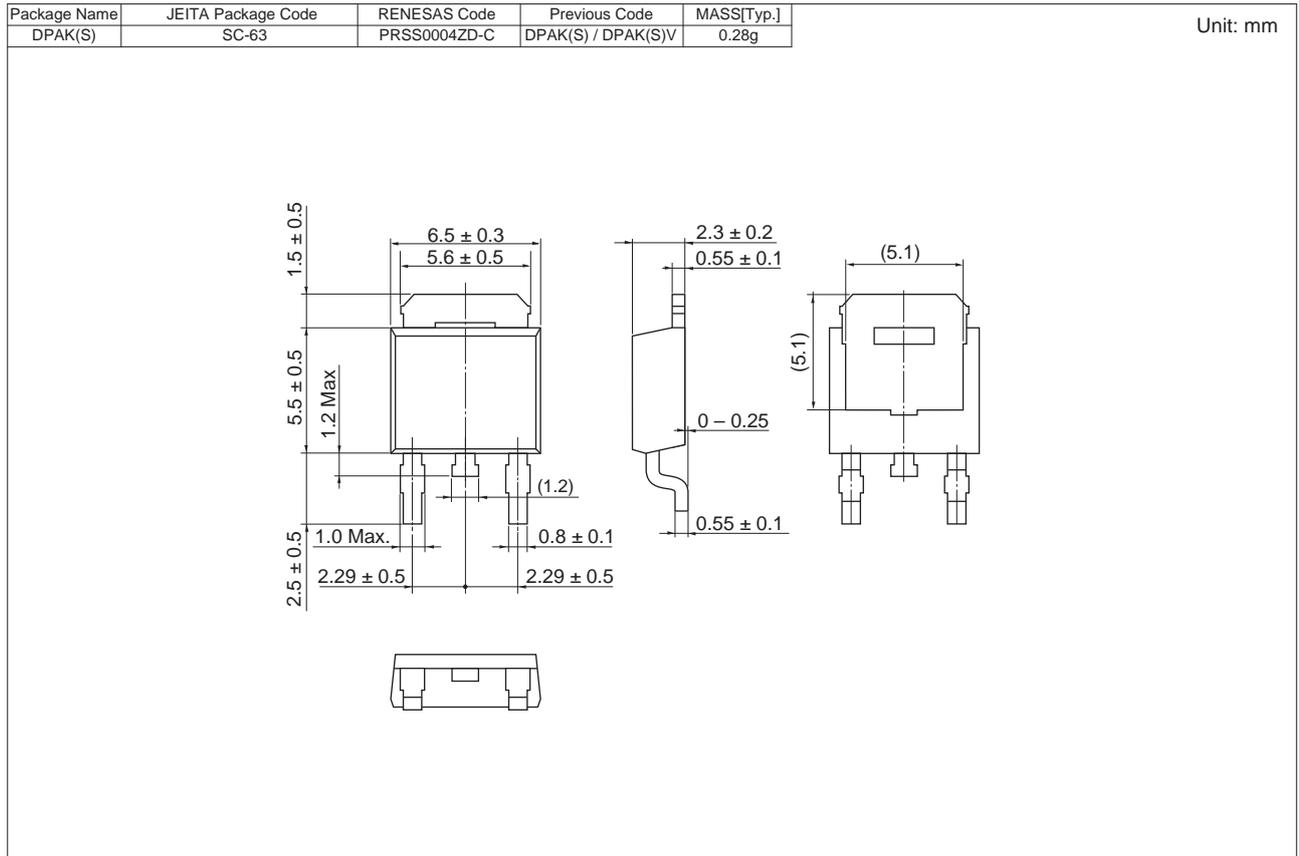
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJE0605JPD-00-J3	3000 pcs	Taping (Sinistrorse)

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