

READ2354J

High Drivability & High Slew Rate, Input Output Full Range,
CMOS Dual Operational Amplifier

R03DS0163EJ0100

Rev.1.00

$V_{IO} \leq \pm 6\text{mV}$, $SR = 8\text{V}/\mu\text{s}$, $GBW = 6\text{MHz}$

2022.5.12

Description

The READ2354J is input and output full range dual CMOS Operational Amplifier realizing high drivability and high slew rate. This IC can be used in minimum operating supply voltage from 2.5V, and in wide ambient temperature range from -40°C to $+125^{\circ}\text{C}$.

Available in ultra-small 8 pins TSSOP packages.

Features

- AEC-Q100 Compliant
- Low voltage single supply operation
- Low input offset voltage
- Low input bias current
- Wide output voltage range
- Supply current (per channel)
- High slew rate

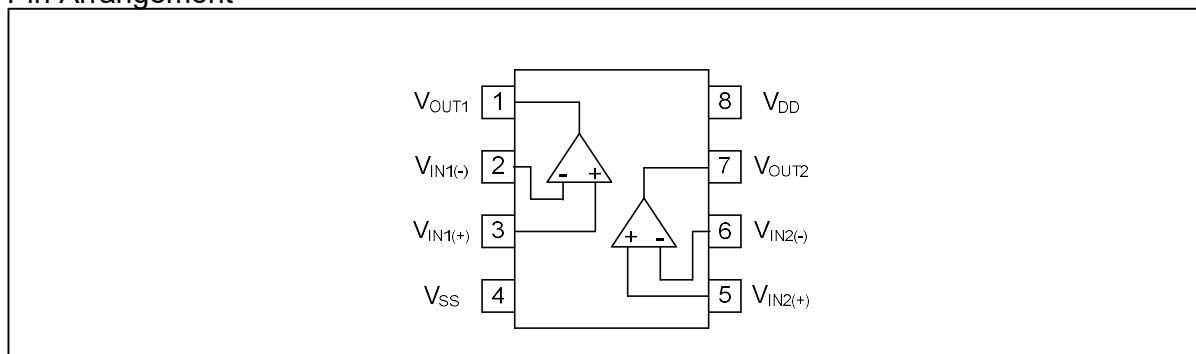
 $V_{DD} = 2.5\text{V to } 5.5\text{V}$
 $V_{IO} \leq \pm 6.0\text{mV}$
 $I_B \leq (1\text{pA})$
 $V_{OUT} : V_{SS} + 0.1\text{V to } V_{DD} - 0.1\text{V} (@I_o = 5\text{mA})$
 $I_{DD} = 0.75\text{mA Typ.}$
 $SR = 8\text{V}/\mu\text{s Typ.}$

() reference value of design

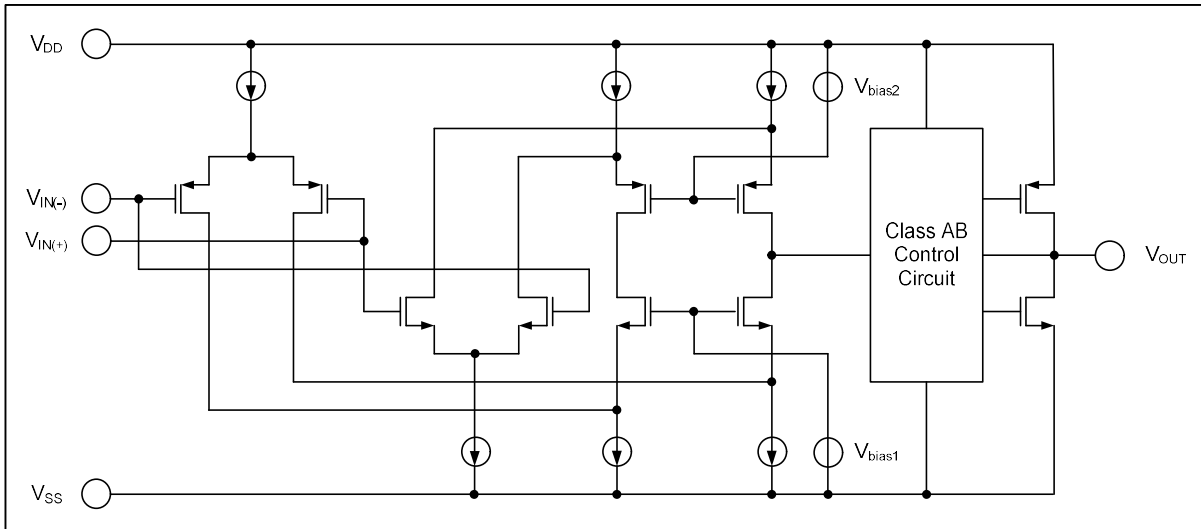
Product Line-up

Type name	Product type quality level	Package
READ2354JSP	High slew rate with high quality level	8 pins plastic TSSOP

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

<TA=25 °C >

Items	Symbol	Ratings	Unit
Supply voltage ^{Note.1}	V _{DD}	-0.3 to +6.5	V
Differential input voltage	V _{ID}	-V _{DD} to +V _{DD}	V
Input voltage ^{Note.2}	V _I	-0.3 to V _{DD} +0.3	V
Maximum output current	I _O	20	mA
Power dissipation ^{Note.3}	P _T	440	mW
Junction temperature	T _j	+150	°C
Operating temp. range	T _A	-40 to +125	°C
Storage temp. range	T _{stg}	-55 to +150	°C

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of GND-0.3V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm×100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern).

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

READ2354JSP: Derate at -5.5 mW/°C when T_A > 69 °C

(Junction – ambient thermal resistance R_{th(J-A)} = 183 °C/W)

Electrical Characteristics<V_{DD}=5V, T_A=25 °C >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Supply voltage	V _{DD} - V _{SS}	2.5		5.5	V	
Input offset voltage	V _{IO}			±6.0	mV	
Input offset current	I _{IO}			(1)	pA	
Input bias current	I _B			(1)	pA	
Output high voltage	V _{OH}	V _{DD} -0.2			V	I _L = 10mA
Output low voltage	V _{OL}			V _{SS} +0.2	V	I _L = 10mA
Voltage gain	A _V	60	90		dB	R _L ≥100kΩ
Channel supply current	I _{DD} /ch		0.75	1.5	mA	R _L =∞, I _o =0
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V _{ICM}	V _{SS}		V _{DD}	V	
Gain bandwidth product	GBW		6		MHz	C _L =20pF
Slew rate	SR		8		V/μs	C _L =20pF

() reference value of design

Notes

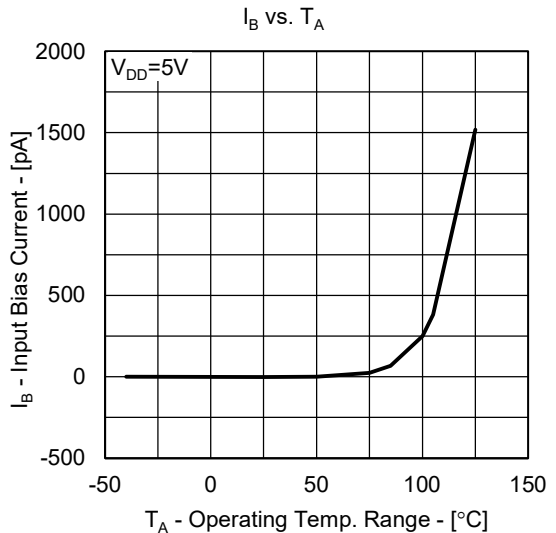
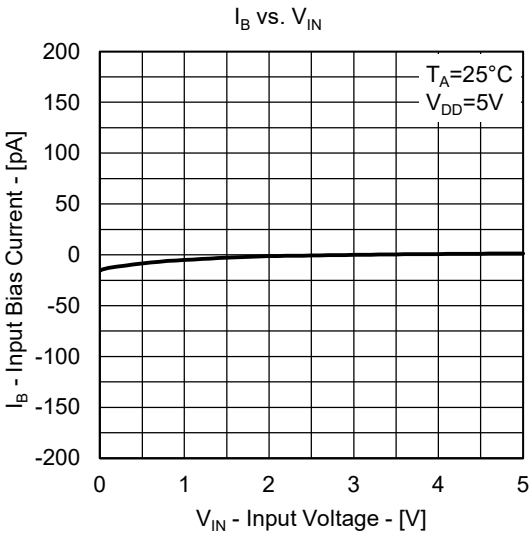
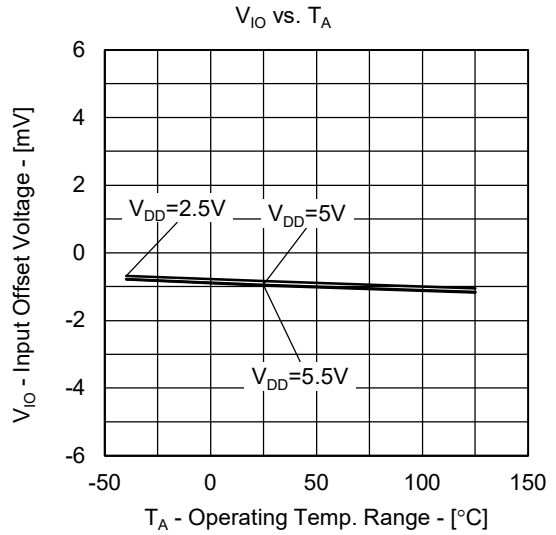
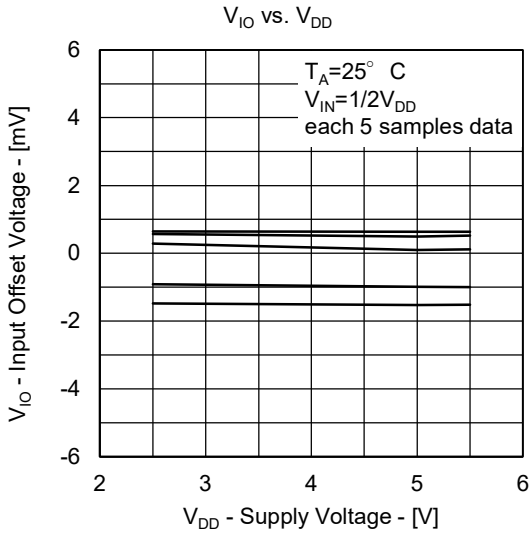
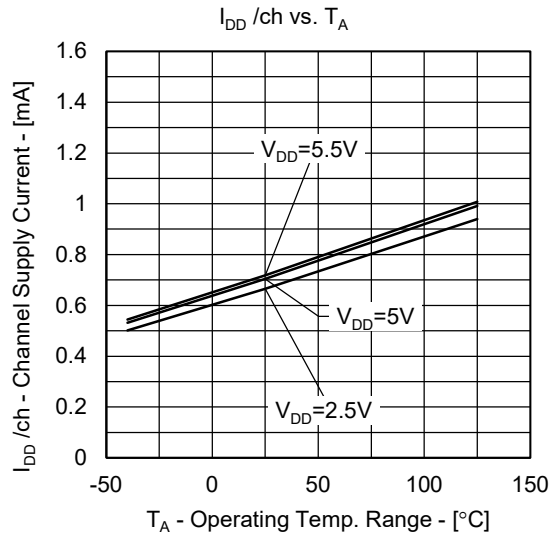
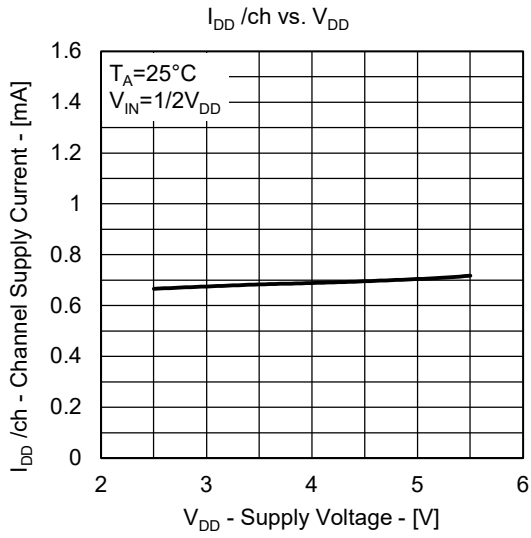
Output terminal : The over-current protection feature is not built in the output terminal of this product.

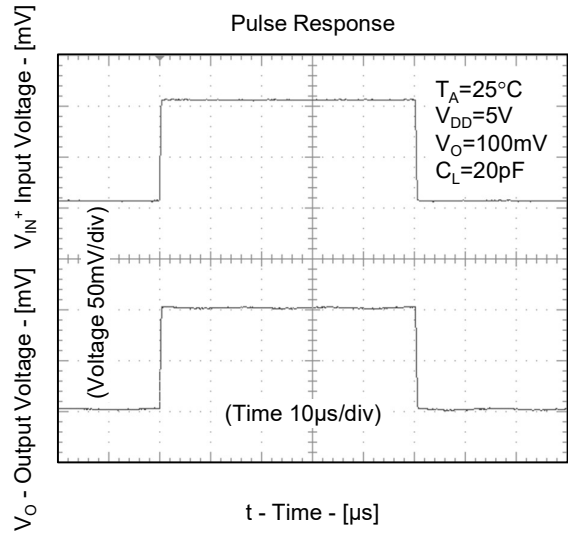
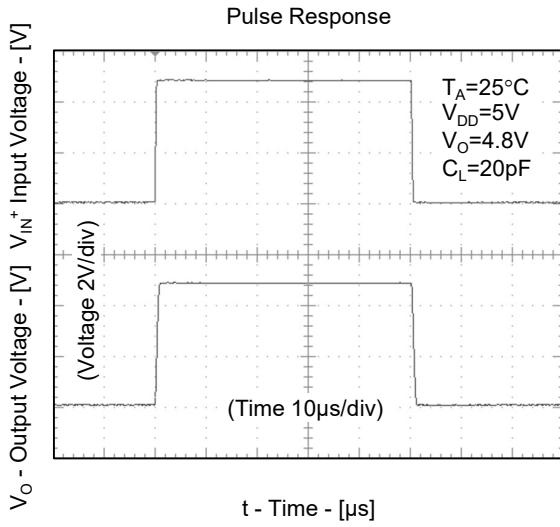
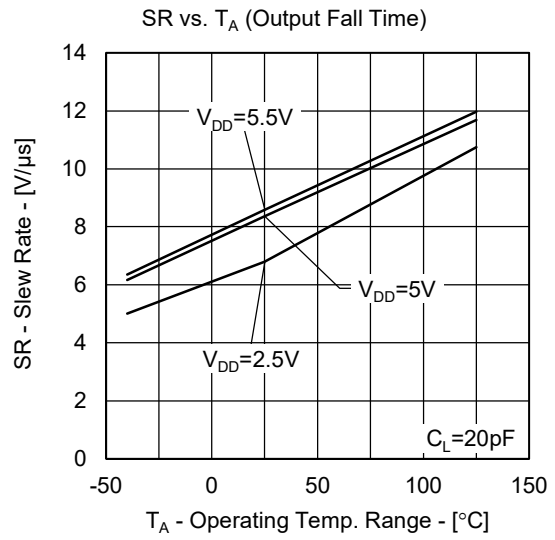
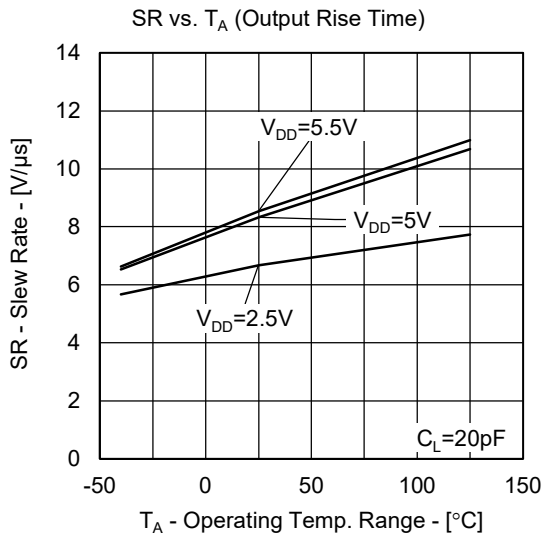
Therefore, please insert resistance to output port.

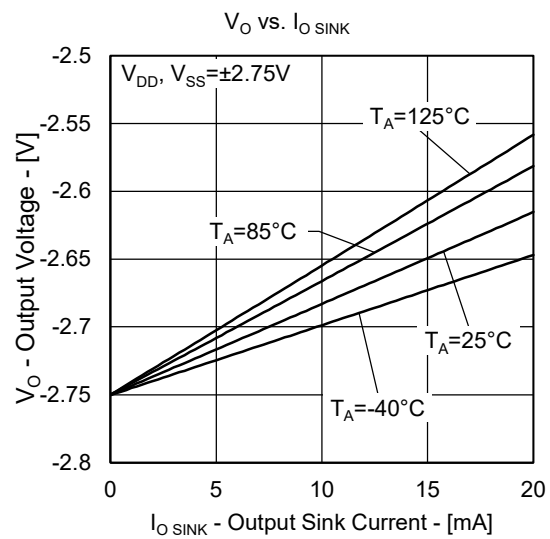
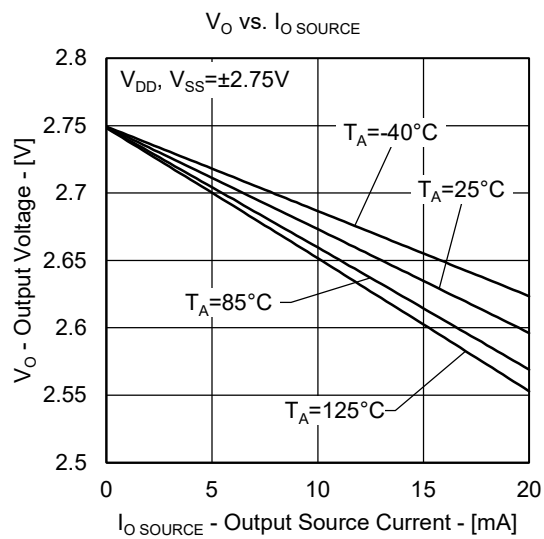
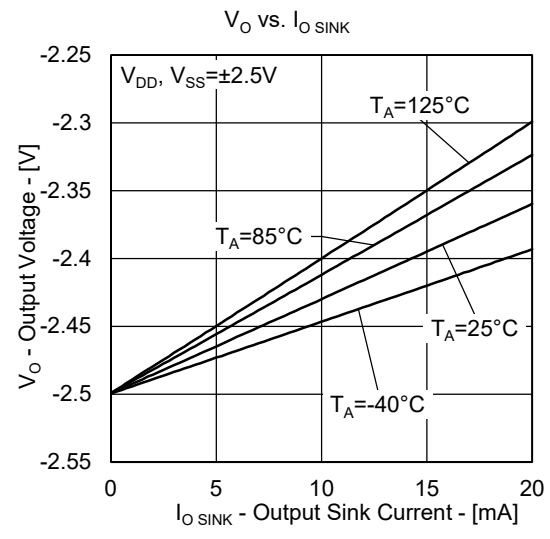
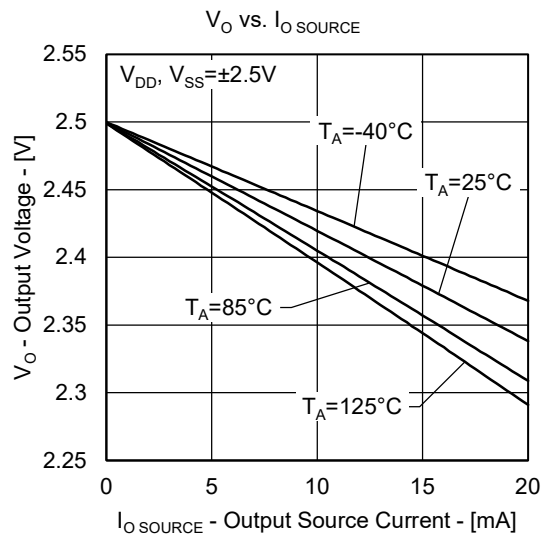
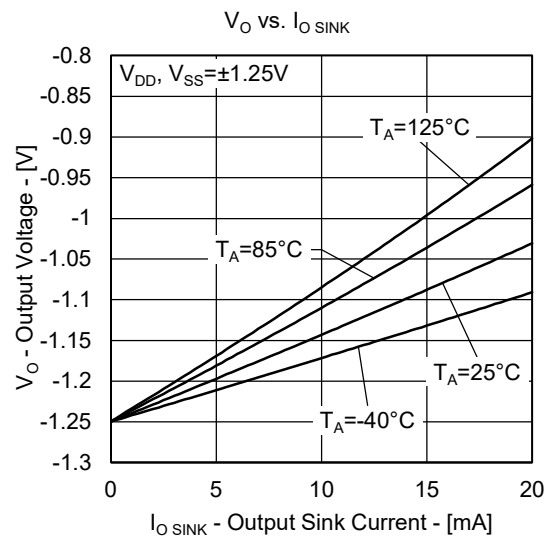
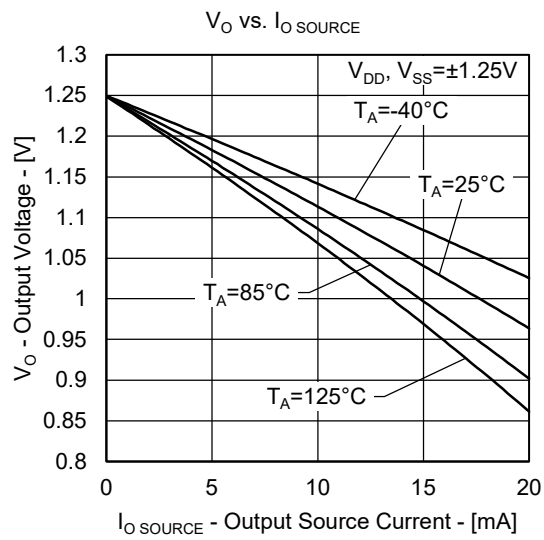
Input offset voltage : The amplifier circuit of the first block of operational amplifier.

A circuit suitable for operation near GND, and a circuit suitable for operation near +power supply. In case of input voltage of overlap point output port has a minute voltage shift or distortion.

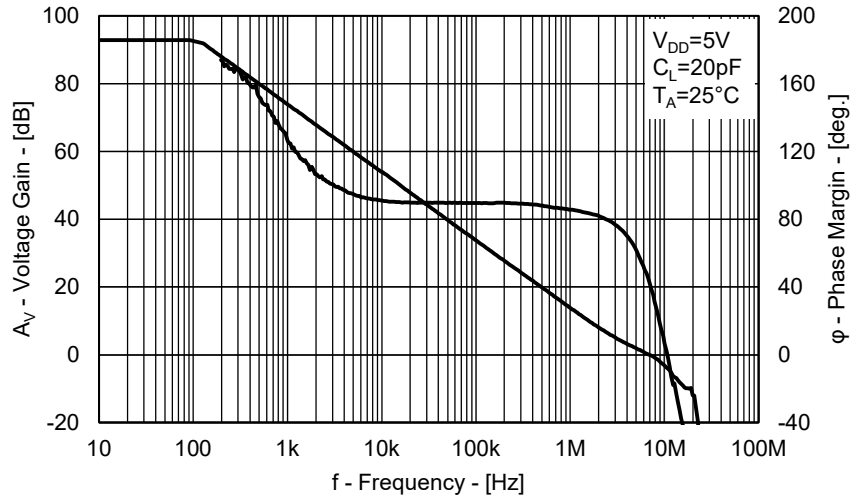
Electrical Characteristics



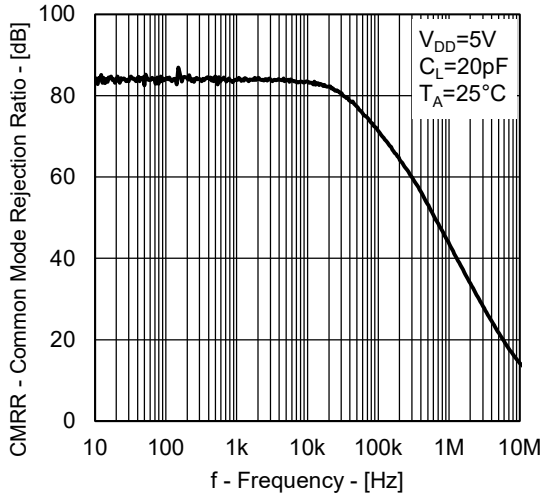




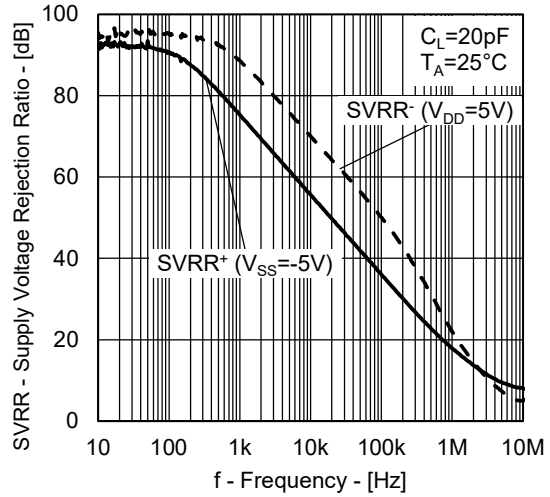
A_v, ϕ vs. f



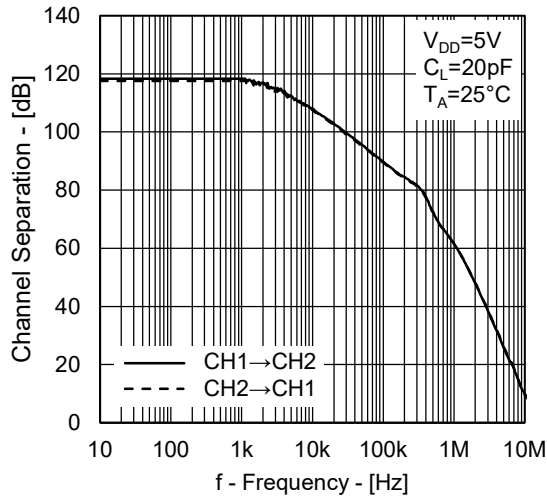
CMRR vs. f



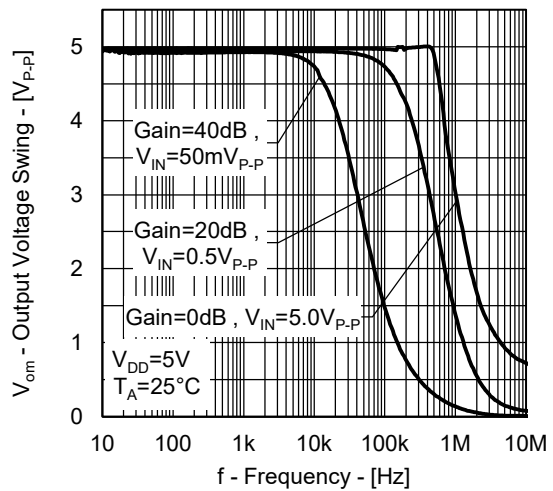
SVRR vs. f



Channel Separation vs. f



V_{om} vs. f

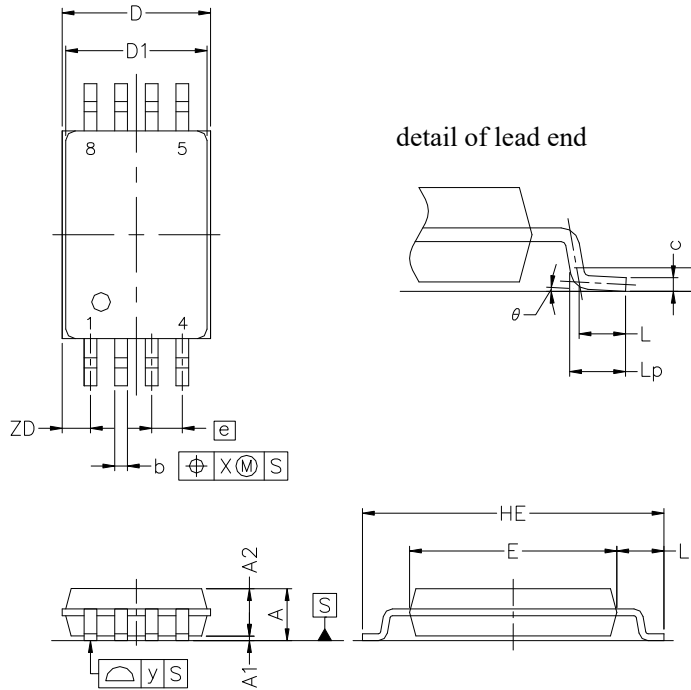


Package Dimensions

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	—

Unit:mm



ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} _{-0.05}
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.60

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

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