READ2304G
High Drivability & High Slew Rate, Input Output Full Range, CMOS Dual Operational Amplifier

Description
The READ2304G is input and output full range dual CMOS Operational Amplifier realizing high drivability and high slew rate. This IC can be used in minimum operating supply voltage from 2.5V, and in wide ambient temperature range from -40˚C to +105˚C.

Features
- Low voltage single supply operation  $V_{DD} = 2.5V$ to $5.5V$
- Low input offset voltage  $V_{IO} \leq \pm 6.0mV$
- Low input bias current  $I_{B} \leq (1pA)$.
- Wide output voltage range  $V_{OUT}: V_{SS}+0.1V$ to $V_{DD}-0.1V(@I_{O}=5mA)$
- Supply current (per channel)  $I_{DD} = 0.75mA$ Typ.
- High slew rate  $SR = 8V/\mu s$ Typ.

( ) reference value of design

Product Line-up

<table>
<thead>
<tr>
<th>Type name</th>
<th>Product type quality level</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ2304GSP</td>
<td>High slew rate with Normal quality level</td>
<td>8 pins plastic TSSOP</td>
</tr>
<tr>
<td>READ2304GSN</td>
<td>High slew rate with Normal quality level</td>
<td>8 pins plastic MSOP</td>
</tr>
</tbody>
</table>

Pin Arrangement

```
V_{OUT1} 1
V_{IN1(-)} 2
V_{IN1(+)} 3
V_{SS} 4
8 V_{DD}
7 V_{OUT2}
6 V_{IN2(-)}
5 V_{IN2(+)}
```
Equivalent Circuit (per one channel)

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VDD</td>
<td>-0.3 to +6.5</td>
<td>V</td>
</tr>
<tr>
<td>Differential input voltage</td>
<td>V_ID</td>
<td>-VDD to +VDD</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>V_I</td>
<td>-0.3 to VDD+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>I_O</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>P_T</td>
<td>440</td>
<td>mW</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>T_J</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating temp. range</td>
<td>T_A</td>
<td>-40 to +105</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temp. range</td>
<td>T_STG</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of GND-0.3V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm x 100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern).

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

READ2304GSP: Derate at -5.5 mW/°C when T_A > 69 °C
(Junction – ambient thermal resistance R_th(J-A) = 183 °C/W)

READ2304GSN: Derate at -4.8 mW/°C when T_A > 58 °C
(Junction – ambient thermal resistance R_th(J-A) = 208 °C/W)
## Electrical Characteristics

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$V_{DD} - V_{SS}$</td>
<td>2.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>$V_{IO}$</td>
<td>±6.0</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input offset current</td>
<td>$I_{IO}$</td>
<td>(1)</td>
<td>pA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input bias current</td>
<td>$I_{IB}$</td>
<td>(1)</td>
<td>pA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output high voltage</td>
<td>$V_{OH}$</td>
<td>$V_{DD} - 0.2$</td>
<td>V</td>
<td>$I_L = 10mA$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output low voltage</td>
<td>$V_{OL}$</td>
<td>$V_{SS} + 0.2$</td>
<td>V</td>
<td>$I_L = 10mA$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage gain</td>
<td>$A_V$</td>
<td>60</td>
<td>90</td>
<td>dB</td>
<td></td>
<td>$R_L = \infty$, $I_O = 0$</td>
</tr>
<tr>
<td>Channel supply current</td>
<td>$I_{DSS/ch}$</td>
<td>0.75</td>
<td>1.5</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common mode rejection ratio</td>
<td>CMRR</td>
<td>60</td>
<td>80</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage rejection ratio</td>
<td>SVRR</td>
<td>60</td>
<td>80</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common mode input voltage range</td>
<td>$V_{ICM}$</td>
<td>$V_{SS}$</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain bandwidth product</td>
<td>GBW</td>
<td>6</td>
<td>MHz</td>
<td>$C_L = 20pF$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew rate</td>
<td>SR</td>
<td>8</td>
<td>V/us</td>
<td>$C_L = 20pF$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

( ) reference value of design

### Notes

Output terminal: The over-current protection feature is not built in the output terminal of this product.

Therefore, please insert resistance to output port.

Input offset voltage: The amplifier circuit of the first block of operational amplifier.

A circuit suitable for operation near GND, and a circuit suitable for operation near +power supply. In case of input voltage of overlap point output port has a minute voltage shift or distortion.
Electrical Characteristics

$I_{DD}/ch$ vs. $V_{DD}$

$T_A=25^\circ C$
$V_{IN}=1/2V_{DD}$

$I_{DD}$ - Channel Supply Current - [mA]
$V_{DD}$ - Supply Voltage - [V]

$V_{IO}$ vs. $V_{DD}$

$T_A=25^\circ C$
$V_{IN}=1/2V_{DD}$

each 5 samples data

$V_{IO}$ - Input Offset Voltage - [mV]
$V_{DD}$ - Supply Voltage - [V]

$I_B$ vs. $V_{IN}$

$T_A=25^\circ C$
$V_{DD}=5V$

$I_B$ - Input Bias Current - [pA]
$V_{IN}$ - Input Voltage - [V]

$I_B$ vs. $T_A$

$V_{DD}=5V$

$I_B$ - Input Bias Current - [pA]
$T_A$ - Operating Temp. Range - [°C]
SR vs. $T_A$ (Output Rise Time)

SR - Slew Rate - [V/μs]

$T_A$ - Operating Temp. Range - [°C]

SR vs. $T_A$ (Output Fall Time)

SR - Slew Rate - [V/μs]

$T_A$ - Operating Temp. Range - [°C]

Pulse Response

Voltage 2V/div

(Voltage 50mV/div)

(Time 10μs/div)

$t$ - Time - [μs]

$V_{DD}=5.5V$

$V_{DD}=5V$

$V_{DD}=2.5V$

$C_L=20pF$

$V_{DD}=5V$

$V_{DD}=2.5V$

$C_L=20pF$

$V_{DD}=5V$

$V_{DD}=2.5V$

$C_L=20pF$

$T_A=25°C$

$V_O=100mV$

$C_L=20pF$

$V_{IN}=2V/div$

$V_{O}-Output Voltage - [mV]$

$V_{IN}=100mV$

$C_L=20pF$

$V_{O}=4.8V$

$C_L=20pF$

$V_{IN}=2V/div$

$V_{O}-Output Voltage - [mV]$

$V_{IN}=100mV$

$C_L=20pF$

$V_{O}=4.8V$

$C_L=20pF$

$V_{IN}=2V/div$

$V_{O}-Output Voltage - [mV]$

$V_{IN}=100mV$

$C_L=20pF$
A\_v, \phi vs. f

CMRR vs. f

SVRR vs. f

Channel Separation vs. f

V\_om vs. f

\(V_{DD}=5V\)
\(C_i=20pF\)
\(T_A=25^\circ C\)

\(A\_v\) - Voltage Gain - [dB]

\(\phi\) - Phase Margin - [deg.]

CMRR - Common Mode Rejection Ratio - [dB]

SVRR - Supply Voltage Rejection Ratio - [dB]

Channel Separation - [dB]

V\_om - Output Voltage Swing - [V\_P-P]

\(V_{DD}=5V\)
\(C_i=20pF\)
\(T_A=25^\circ C\)

Gain=40dB , \(V_{IN}=50mV_{P-P}\)
Gain=20dB , \(V_{IN}=0.5V_{P-P}\)
Gain=0dB , \(V_{IN}=5.0V_{P-P}\)

Gain=0dB , \(V_{IN}=5.0V_{P-P}\)

\(V_{DD}=5V\)
\(T_A=25^\circ C\)

CH1→CH2
CH2→CH1

\(V_{DD}=5V\)
\(C_i=20pF\)
\(T_A=25^\circ C\)

\(V_{DD}=5V\)
\(C_i=20pF\)
\(T_A=25^\circ C\)
# Package Dimensions

## 8-PIN PLASTIC TSSOP

<table>
<thead>
<tr>
<th>JEITA Package code</th>
<th>RENESAS code</th>
<th>Previous code</th>
<th>MASS (TYP.) [g]</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-TSSOP8-0225-0.65</td>
<td>PTSP0008JD-A</td>
<td>P8GR-65-9LG</td>
<td>—</td>
</tr>
</tbody>
</table>

**Unit:** mm

**NOTE**
Each lead centerline is located within 0.10 mm of its true position at maximum material condition.
**8-PIN PLASTIC MSOP**

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS (TYP.) [g]</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-TSSOP8-2.8x2.9-0.65</td>
<td>PTSP0008JF-A</td>
<td>P8MP-65-KAA-1</td>
<td>0.02</td>
</tr>
</tbody>
</table>

**NOTE**

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.
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