READ2302G
High Drivability & High Slew Rate, Input Output Full Range, CMOS Dual Operational Amplifier

$V_{\text{IO}} \leq \pm 6\text{mV}$, $SR = 8\text{V/\mu s}$, $GBW = 6\text{MHz}$

Description
The READ2302G is input and output full range dual CMOS Operational Amplifier realizing high drivability and high slew rate. This IC can be used in minimum operating supply voltage from 2.5V, and in wide ambient temperature range from -40°C to +105°C.

Available in ultra-small 8 pins TSSOP packages.

Features
- Low voltage single supply operation $V_{\text{DD}} = 2.5\text{V to 5.5V}$
- Low input offset voltage $V_{\text{IO}} \leq \pm 6.0\text{mV}$
- Low input bias current $I_{B} \leq (1\text{pA})$.
- Wide output voltage range $V_{\text{OUT}}: V_{SS}+0.1\text{V to } V_{DD}-0.1\text{V(@Io=5mA)}$
- Supply current (per channel) $I_{DD} = 0.75\text{mA Typ.}$
- High slew rate $SR = 8\text{V/\mu s Typ.}$

(Product reference value of design)

Product Line-up

<table>
<thead>
<tr>
<th>Type name</th>
<th>Product type quality level</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ2302GSP</td>
<td>High slew rate with Normal quality level</td>
<td>8 pins plastic TSSOP</td>
</tr>
</tbody>
</table>


## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage ^Note.1</td>
<td>VDD</td>
<td>-0.3 to +6.5</td>
<td>V</td>
</tr>
<tr>
<td>Differential input voltage</td>
<td>V_ID</td>
<td>-V_DD to +V_DD</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage ^Note.2</td>
<td>V_I</td>
<td>-0.3 to V_DD +0.3</td>
<td>V</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>I_O</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Power dissipation ^Note.3</td>
<td>P_T</td>
<td>440</td>
<td>mW</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>T_J</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating temp. range</td>
<td>T_A</td>
<td>-40 to +105</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temp. range</td>
<td>T_STG</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

*Note 1.* Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of GND-0.3V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm×100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern). Please take note that every package has derating rate’s restriction reception.
### Electrical Characteristics  
\(<V_{DD}=5V, \ T_A=25^\circ C>\)

<table>
<thead>
<tr>
<th>Items</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>(V_{DD}-V_{SS})</td>
<td>2.5</td>
<td></td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>(V_{IO})</td>
<td></td>
<td>(\pm 6.0)</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Input offset current</td>
<td>(I_{IO})</td>
<td></td>
<td>(1)</td>
<td></td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Input bias current</td>
<td>(I_{IB})</td>
<td></td>
<td>(1)</td>
<td></td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Output high voltage</td>
<td>(V_{OH})</td>
<td></td>
<td>(V_{DD}-0.2)</td>
<td></td>
<td>V</td>
<td>(I_L = 10mA)</td>
</tr>
<tr>
<td>Output low voltage</td>
<td>(V_{OL})</td>
<td></td>
<td>(V_{SS}+0.2)</td>
<td></td>
<td>V</td>
<td>(I_L = 10mA)</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>(A_V)</td>
<td>60</td>
<td>90</td>
<td></td>
<td>dB</td>
<td>(R_L\geq 100k\Omega)</td>
</tr>
<tr>
<td>Channel supply current</td>
<td>(I_{DD/ch})</td>
<td>0.75</td>
<td>1.5</td>
<td></td>
<td>mA</td>
<td>(R_L=\infty, \ I_O=0)</td>
</tr>
<tr>
<td>Common mode rejection ratio</td>
<td>(CMRR)</td>
<td>60</td>
<td>80</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Supply voltage rejection ratio</td>
<td>(SVRR)</td>
<td>60</td>
<td>80</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Common mode input voltage range</td>
<td>(V_{ICM})</td>
<td>(V_{SS})</td>
<td>(V_{DD})</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Gain bandwidth product</td>
<td>(GBW)</td>
<td>6</td>
<td></td>
<td></td>
<td>MHz</td>
<td>(C_L=20pF)</td>
</tr>
<tr>
<td>Slew rate</td>
<td>(SR)</td>
<td>8</td>
<td></td>
<td></td>
<td>V/\mu s</td>
<td>(C_L=20pF)</td>
</tr>
</tbody>
</table>

( ) reference value of design

**Notes**

Output terminal: The over-current protection feature is not built in the output terminal of this product. Therefore, please insert resistance to output port.

Input offset voltage: the amplifier circuit of the first block of operational amplifier.

A circuit suitable for operation near GND, and a circuit suitable for operation near +power supply.

In case of input voltage of overlap point output port has a minute voltage shift or distortion.
Electrical Characteristics

- **$I_{DD}/ch$ vs. $V_{DD}$**
  - $T_A = 25^\circ C$
  - $V_{IN} = 1/2V_{DD}$
  - $V_{DD} = 2.5V$
  - $V_{DD} = 5V$
  - $V_{DD} = 5.5V$

- **$I_{DD}/ch$ vs. $T_A$**
  - $V_{DD} = 2.5V$
  - $V_{DD} = 5V$
  - $V_{DD} = 5.5V$

- **$V_{IO}$ vs. $V_{DD}$**
  - $T_A = 25^\circ C$
  - $V_{IN} = 1/2V_{DD}$
  - each 3 samples data

- **$V_{IO}$ vs. $T_A$**
  - $V_{DD} = 5V$

- **$I_B$ vs. $V_{IN}$**
  - $T_A = 25^\circ C$
  - $V_{DD} = 5V$

- **$I_B$ vs. $T_A$**
  - $V_{DD} = 5V$
SR vs. $T_A$ (Output rise time)

$T_A$ - Operating temp. range - °C

$V_{DD}=2.5V$

$V_{DD}=5V$

$V_{DD}=5.5V$

$V_{DD}=2.5V$

$C_L=20pF$

SR - Slew rate - V/μs

SR vs. $T_A$ (Output fall time)

$T_A$ - Operating temp. range - °C

$V_{DD}=2.5V$

$V_{DD}=5V$

$V_{DD}=5.5V$

$V_{DD}=2.5V$

$C_L=20pF$

SR - Slew rate - V/μs

Pulse response

$T_A=25°C$

$V_{DD}=5V$

$V_{IN}=4.8V$

$C_L=20pF$

Input voltage - mV

Output voltage - mV

Pulse response

$T_A=25°C$

$V_{DD}=5V$

$V_{IN}=100mV$

$C_L=20pF$

Input voltage - V

Output voltage - V

V - Output voltage - mV

$V_{DD} - 2V/div$

$V_{DD} - 50mV/div$

$t$ - Time - μs

(time 10μs/div)
$A_V, \phi$ vs. $f$

$A_V$ - Voltage gain - dB

$\phi$ - Phase margin - deg.

$AV, \phi$ vs. $f$

$V_{DD}=5V$

$C_L=20pF$

$T_A=25^\circ C$

CMRR vs. $f$

CMRR - Common mode rejection ratio - dB

$CMRR$ vs. $f$

$V_{DD}=5V$

$C_L=20pF$

$T_A=25^\circ C$

SVRR vs. $f$

SVRR - Supply voltage rejection ratio - dB

$SVRR$ vs. $f$

$CL=20pF$

$TA=25^\circ C$

Channel separation vs. $f$

Channel separation - dB

Channel separation vs. $f$

$V_{om}$ vs. $f$

$V_{om}$ - Output voltage swing - $V_{P-P}$

$V_{om}$ vs. $f$

$V_{DD}=5V$

$T_A=25^\circ C$

Gain=40dB , $V_{in}=50mV_{P-P}$

Gain=20dB , $V_{in}=0.5V_{P-P}$

Gain=0dB , $V_{in}=5.0V_{P-P}$
Package Dimensions

8-PIN PLASTIC TSSOP

<table>
<thead>
<tr>
<th>JEITA Package code</th>
<th>RENESAS code</th>
<th>Previous code</th>
<th>MASS(TYP.)[g]</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-TSSOP8-0225-0.65</td>
<td>PTSP0008JD-A</td>
<td>P8GR-65-9LG</td>
<td>-</td>
</tr>
</tbody>
</table>

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

<table>
<thead>
<tr>
<th>ITEM</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>3.15 ±0.15</td>
</tr>
<tr>
<td>D1</td>
<td>3.00 ±0.10</td>
</tr>
<tr>
<td>E</td>
<td>4.40 ±0.10</td>
</tr>
<tr>
<td>HE</td>
<td>6.40 ±0.20</td>
</tr>
<tr>
<td>A</td>
<td>1.20 MAX.</td>
</tr>
<tr>
<td>A1</td>
<td>0.10 ±0.05</td>
</tr>
<tr>
<td>A2</td>
<td>1.00 ±0.05</td>
</tr>
<tr>
<td>A3</td>
<td>0.25</td>
</tr>
<tr>
<td>b</td>
<td>0.24 +0.06  -0.05</td>
</tr>
<tr>
<td>c</td>
<td>0.145 ±0.055</td>
</tr>
<tr>
<td>L</td>
<td>0.5</td>
</tr>
<tr>
<td>Lp</td>
<td>0.60 ±0.15</td>
</tr>
<tr>
<td>L1</td>
<td>1.00 ±0.20</td>
</tr>
<tr>
<td>θ</td>
<td>3° +5°      -3°</td>
</tr>
<tr>
<td>e</td>
<td>0.65</td>
</tr>
<tr>
<td>x</td>
<td>0.10</td>
</tr>
<tr>
<td>y</td>
<td>0.10</td>
</tr>
<tr>
<td>ZD</td>
<td>0.60</td>
</tr>
</tbody>
</table>
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