RC32012A-001

RC32012A-001 Custom Configuration

This datasheet addendum is to be used in conjunction with the overall RC32012A datasheet. This addendum indicates the register settings that are pre-configured in the internal One-Time Programmable (OTP) memory of the device by Renesas. These register settings represent the default values the registers will take on power-up or reset. Values may be changed at any time afterwards over the serial port, but any such changes will be lost when the device is reset or power-cycled unless programmed into OTP as an additional or replacement configuration.

In addition, there are several other pieces of documentation that describe specific functions or details not covered this document. Table 1 shows related documents.

Table 1. Related Documentation for RC32012A-001

Document Title	Document Description
RC32012A Datasheet	Contains a functional overview of the device and hardware-design related details including pinouts, AC and DC specifications and applications information related to power filtering and terminations.
RC32012A-001 Datasheet Addendum (this document)	Indicated pre-programmed power-up / reset configurations of this specific dash code part number.
8A3xxxx Family Programming Guide	Contains detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.
Evaluation Board Reference Manual	Describes the evaluation board. Evaluation boards are available for the 8A34001 (144BGA) or 8A34002 (72QFN) devices. These devices contain a superset of the functionality available in all other members of the 8A3xxxx family. They can serve as evaluation tools for any of the less fully-featured family members.
Timing Commander Personality User Manual	Detailed description of how to use Renesas' Timing Commander configuration tool. At this time, a personality file is only available for 8A34001. This personality contains a superset of the functionality available in all other members of the 8A3xxxx family. Since all members of the 8A3xxxx family share register locations and resource numbering, configurations generated using the 8A34001 personality can be used in any member of the 8A3xxxx family. Functionality that is not available on the other family members will of course not respond to any configuration of it that is made.

Device Information Block Contents

GPIO Usage at Reset

GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO9
OTP configuration select	OTP configuration select	OTP configuration select	OTP configuration select	Unused	Synthesizer mode (EEPROM load disable)	Unused

Analog Voltage Used on VDDA_BG_LC and VDDA_PDCP_XTAL

Voltage Level used on VDDA_BG_LC Supply[1]	Voltage Level used on VDDA_PDCP_XTAL[1]
3.3V	3.3V

1. Used during device reset period to set regulator parameters for fastest startup time. Can be changed later via register accesses or in configuration data, but that will result in extended startup time while re-calibration occurs.

Device Initial Configuration Information for Configuration 0

Present as blank configuration.

Device Initial Configuration Information for Configuration 1

Present as blank configuration.

Device Initial Configuration Information for Configuration 2

Present as blank configuration.

Device Initial Configuration Information for Configuration 3

Present as blank configuration.

Device Initial Configuration Information for Configuration 4

Present as blank configuration.

Device Initial Configuration Information for Configuration 5

Present as blank configuration.

Device Initial Configuration Information for Configuration 6

Present as blank configuration.

Device Initial Configuration Information for Configuration 7

Present as blank configuration.

Device Initial Configuration Information for Configuration 8

Present as blank configuration.

Device Initial Configuration Information for Configuration 9

Present as blank configuration.

Device Initial Configuration Information for Configuration 10

Present as blank configuration.

Device Initial Configuration Information for Configuration 11

Present as blank configuration.

Device Initial Configuration Information for Configuration 12

Present as blank configuration.

Device Initial Configuration Information for Configuration 13

Present as blank configuration.

Device Initial Configuration Information for Configuration 14

Present as blank configuration.

Device Initial Configuration Information for Configuration 15

Serial Port Mode Main	Serial Port Aux Main
Selected by GPIO9 (7b base I2C address) High: I2C (1011 A2* A1* A0*) Low: SPI	Selected by GPIO9 (7b base I2C address) High: SPI Low: I2C (1011 A2* A1* A0*)

* Hardware pins latched at power-up reset.

Inputs

Crystal Frequency (MHz)	XO_DPLL Input (MHz)	CLK0 (MHz)	CLK1 (MHz)	CLK8 (MHz)	CLK9 (MHz)	CLK13 (MHz)	CLK14 (MHz)	CLK15 (MHz)
49.152	10	156.25	125	—	—	—	—	—

Outputs

Output	Frequency (MHz)	Type	Enable	Source	Divider	VDDO_Q
Q0	322.2656	LVPECL 2.5V	Enabled	DPLL0	2	2.5V
Q1	322.2656	LVPECL 2.5V	Enabled	DPLL0	2	2.5V
Q2	125	LVPECL 2.5V	Enabled	DPLL5	5	2.5V
Q3	156.25	LVPECL 2.5V	Enabled	DPLL5	4	2.5V
Q4	184.32	LVPECL 2.5V	Enabled	DPLL2	5	2.5V
Q5	153.6	LVPECL 2.5V	Enabled	DPLL2	6	2.5V
Q6	153.6	LVPECL 2.5V	Enabled	DPLL2	6	2.5V
Q7	156.25	LVPECL 2.5V	Enabled	DPLL7	4	1.8V
Q8	125	LVPECL 2.5V	Enabled	DPLL5	5	2.5V
Q9	156.25	LVDS	Enabled	DPLL5	4	1.8V
Q10	184.32	LVPECL 2.5V	Enabled	DPLL2	5	2.5V
Q11	125	CMOS	Enabled	DPLL7	5	1.8V

PLL Channel Configuration

Channel	Mode	Frequency (MHz)	LockBW	Dampening Factor	Primary Source	Reference Selection
System APLL	Synthesizer	13762.56	—	—	Crystal (doubled)	—
System DPLL	Disabled	—	—	—	—	—
DPLL0	Jitter Attenuator	644.53125	25Hz	Overdamp	0	Manual
DPLL2	Synthesizer	921.6	0µHz	Overdamp	—	Automatic
DPLL5	Synthesizer	625	0µHz	Overdamp	—	Automatic
DPLL7	Synthesizer	625	0µHz	Overdamp	—	Automatic

GPIOs

	GPIO0	GPIO1	GPIO2	GPIO3
Enabled	False	False	False	False
Mode	User control	User control	User control	User control
Function	Used as input for CLK13	User control (direction: input)	User control (direction: input)	Used as input for CLK15

	GPIO4	GPIO5	GPIO9
Enabled	False	False	False
Mode	User control	User control	User control
Function	User control (direction: input)	User control (direction: input)	Used as input for CLK14

Ordering Information and Marking Diagram

Refer to the RC32012A page for product options. Download the datasheet for ordering information and marking diagram.

Revision History

Revision	Date	Description
1.00	Aug 27, 2021	Initial release of the RC32012A-001 Datasheet Addendum.

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