RBA160N04AHPF-4UA01

40V – 160A – N-channel Power MOS FET

Application: Automotive

Description
The RBA160N04AHPF-4UA01 is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features
- Super low on-state resistance
  \( R_{DS(on)} = 1.25 \, \text{m}\Omega \, \text{MAX.} \) (\( V_{GS} = 10 \, \text{V}, I_D = 80 \, \text{A} \))
- Low input capacitance
  \( Ciss = 8800 \, \text{pF TYP.} \) (\( V_{DS} = 25 \, \text{V} \))
- Designed for automotive application and AEC-Q101 qualified
- Pb-free (This product does not contain Pb in the external electrode)

Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Quantity</th>
<th>Shipping container</th>
</tr>
</thead>
<tbody>
<tr>
<td>RBA160N04AHPF-4UA01#GB0</td>
<td>800pcs/reel</td>
<td>Taping</td>
</tr>
</tbody>
</table>

Outline

1. Gate
2. Drain
3, 4, 5, 6, 7. Source
8. Drain (Fin)

TO-263-7pin-SHL* (MP-25ZU)
* Short Head & Lead

Equivalent circuit

Remark
Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to Source Voltage (VGS = 0 V)</td>
<td>VDSS</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Gate to Source Voltage (VDS = 0 V)</td>
<td>VGSS</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current (DC) (Tc = 25 °C)</td>
<td>ID(0°C)</td>
<td>±160</td>
<td>A</td>
</tr>
<tr>
<td>Drain Current (pulse) Note1</td>
<td>ID(pulse)</td>
<td>±640</td>
<td>A</td>
</tr>
<tr>
<td>Total Power Dissipation (Tc = 25 °C)</td>
<td>PT1</td>
<td>250</td>
<td>W</td>
</tr>
<tr>
<td>Total Power Dissipation (TA = 25 °C)</td>
<td>PT2</td>
<td>1.8</td>
<td>W</td>
</tr>
<tr>
<td>Channel Temperature</td>
<td>Tch</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-55 to 175</td>
<td>°C</td>
</tr>
<tr>
<td>Repetitive Avalanche Current Note2</td>
<td>IAR</td>
<td>55</td>
<td>A</td>
</tr>
<tr>
<td>Repetitive Avalanche Energy Note3</td>
<td>EAR</td>
<td>303</td>
<td>mJ</td>
</tr>
</tbody>
</table>

Note 1. Pd ≤ 10 μs, Duty Cycle ≤ 1%
2. VGS = 20 → 0V, RG = 25 Ω
3. L = 100μH, VDD = 20V, VGS = 20 → 0V, RG = 25 Ω

Thermal Resistance

Channel to Case Thermal Resistance | RH(ch-c) | 0.60 | °C/W |
Channel to Ambient Thermal Resistance | RH(ch-A) | 83.3 | °C/W |

Electrical Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IGS</td>
<td>1</td>
<td>μA</td>
<td>83.3</td>
<td>VDD = 40 V, VGS = 0 V</td>
<td></td>
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<tr>
<td>Gate Leakage Current</td>
<td>IDSS</td>
<td>±100</td>
<td>nA</td>
<td>250</td>
<td>VGS = ±20 V, VDS = 0 V</td>
<td></td>
</tr>
<tr>
<td>Gate to Source Threshold Voltage</td>
<td>VGSSH</td>
<td>2.0</td>
<td>3.0</td>
<td>4.0</td>
<td>V</td>
<td>VGS = VGS, IG = 250 μA</td>
</tr>
<tr>
<td>Drain to Source On-state Resistance</td>
<td>RD(on)</td>
<td>1.05</td>
<td>1.25</td>
<td>mΩ</td>
<td>VGS = 10 V, IG = 80 A</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Ciss</td>
<td>8800</td>
<td>13200</td>
<td>pF</td>
<td>VGS = 25 V</td>
<td></td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>Coss</td>
<td>980</td>
<td>1470</td>
<td>pF</td>
<td>VGS = 0 V</td>
<td></td>
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<tr>
<td>Reverse Transfer Capacitance</td>
<td>CRSS</td>
<td>530</td>
<td>960</td>
<td>pF</td>
<td>f = 1 MHz</td>
<td></td>
</tr>
<tr>
<td>Turn-on Delay Time</td>
<td>tD(on)</td>
<td>32</td>
<td>64</td>
<td>ns</td>
<td>VDD = 20 V, IG = 80 μA</td>
<td></td>
</tr>
<tr>
<td>Rise Time</td>
<td>tR</td>
<td>22</td>
<td>53</td>
<td>ns</td>
<td>VGS = 10 V</td>
<td></td>
</tr>
<tr>
<td>Turn-off Delay Time</td>
<td>tD(off)</td>
<td>97</td>
<td>194</td>
<td>ns</td>
<td>RG = 0 Ω</td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>tF</td>
<td>22</td>
<td>53</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>QG</td>
<td>157</td>
<td>236</td>
<td>nC</td>
<td>VDD = 32 V</td>
<td></td>
</tr>
<tr>
<td>Gate to Source Charge</td>
<td>Qgs</td>
<td>37</td>
<td>nC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate to Drain Charge</td>
<td>QGD</td>
<td>40</td>
<td>nC</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Body Diode Forward Voltage</td>
<td>VFB</td>
<td>0.9</td>
<td>1.5</td>
<td>V</td>
<td>IR = 160 A, VGS = 0 V</td>
<td></td>
</tr>
<tr>
<td>Reverse Recovery Time</td>
<td>tRR</td>
<td>71</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Recovery Charge</td>
<td>QRR</td>
<td>92</td>
<td>nC</td>
<td></td>
<td></td>
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</tbody>
</table>

Note 4. Pulse test
Note 5. Refer value
Test Circuit

Avalanche Test Circuit

\[ I_{as} = \frac{1}{2} \cdot L \cdot I_{as}^2 \cdot \frac{V_{oss}}{V_{oss} - V_{dd}} \]

Switching Time Test Circuit

Waveform

\[ V_{oss} \]

\[ V_{dd} \]

\[ I_{in} \]

\[ V_{oss} \]

\[ 0 \]

\[ 0 \]

\[ E_{as} \]

\[ V_{oss} \]

\[ V_{dd} \]

\[ I_{as} \]
Typical Characteristics (TA = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

FORWARD BIAS SAFE OPERATING AREA

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

DYNAMIC INPUT/OUTPUT CHARACTERISTICS

SOURCE TO DRAIN DIODE FORWARD VOLTAGE
Package Dimensions

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASS (Typ) [g]</th>
<th>Package Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>PRSS0008DC-A</td>
<td>—</td>
<td>1.39</td>
<td>MP-25ZU</td>
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</tbody>
</table>

Unit: mm
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