RAA223881

700V Off-line Flyback Regulator

The RAA223881, an off-line flyback regulator with an integrated 700V power MOSFET, provides a cost-effective solution for high-input voltage applications such as appliances, air conditioners, and general-purpose isolated power supplies.

The flyback regulator operates with a constant switching frequency of 65kHz and employs current mode control. At light loads, it operates in burst mode to reduce power consumption and uses secondary-side feedback to provide excellent output voltage regulation.

The RAA223881 features an integrated high-voltage (HV) startup for a low system-component count. It also provides frequency dithering to simplify EMI filter design. The device comes in a 7 Ld PDIP package.

Features

- Integrated with 700V 5Ω MOSFET
- Constant frequency PWM operation with current mode control
- Burst mode operation at light load
- Protections:
  - Short-circuit protection (SCP)
  - Overload protection (OLP)
  - Input undervoltage protection (V_{IN}UV)
  - V_{CC} overvoltage protection (V_{CC}OV)
  - Output open-loop protection (OLP)
  - Short-winding protection (SWP)
  - Over-temperature protection (OTP)

Applications

- Large appliances
- Air conditioners
- Auxiliary power supply for TV, set-top box, or LCD/LED monitor
- Industry equipment

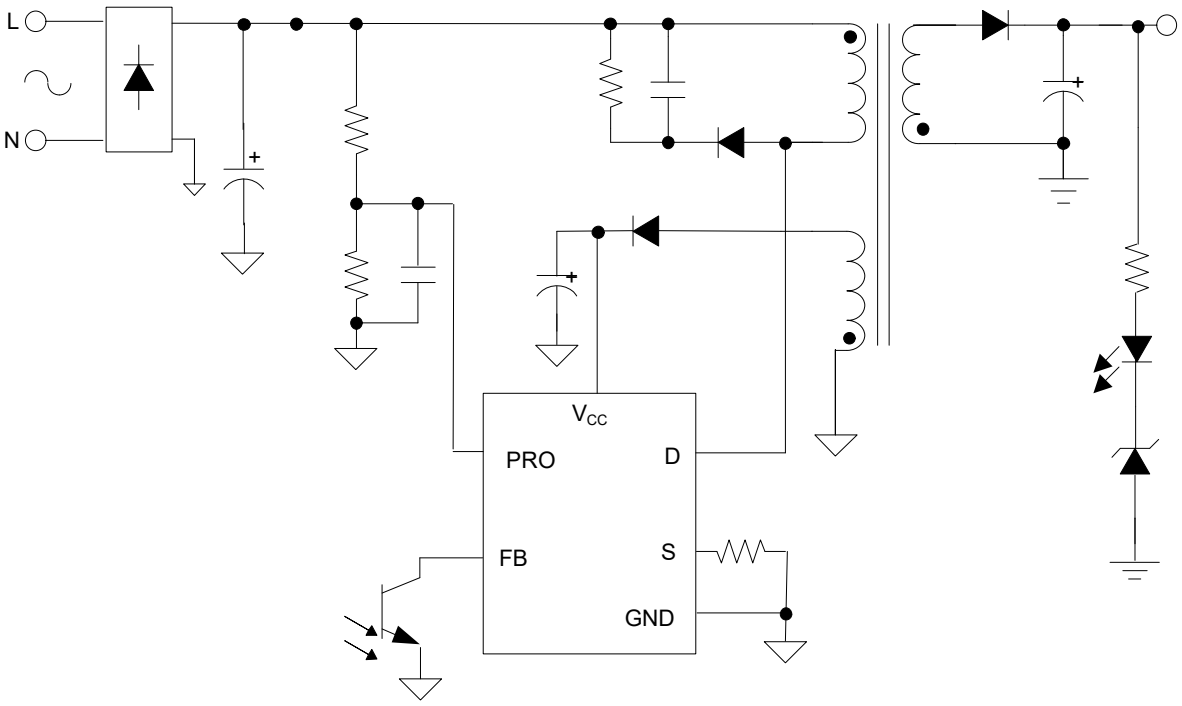

Figure 1. Typical Flyback Circuit

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1. Overview

1.1 Block Diagram

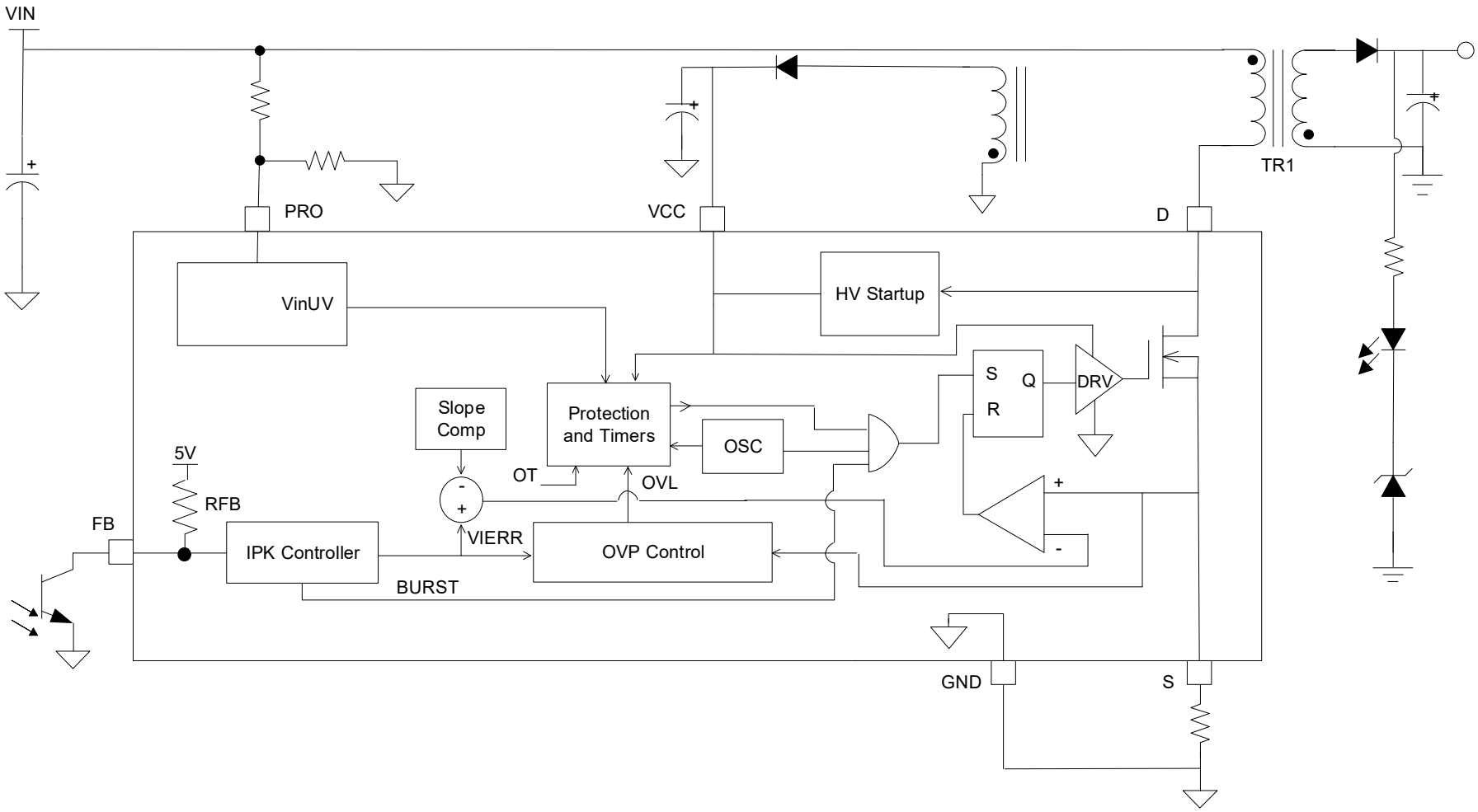


Figure 2. Block Diagram of RAA223881

2. Pin Information

2.1 Pin Assignments

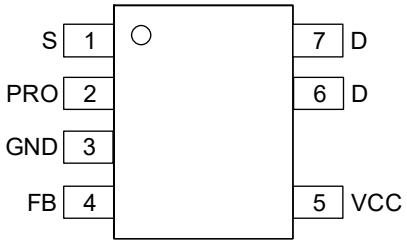


Figure 3. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	S	Source of power FET
2	PRO	Input voltage sense
3	GND	IC ground
4	FB	Feedback signal input
5	VCC	IC supply voltage
6	D	Drain of power FET
7	D	Drain of power FET

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC	-0.3	+30	V
VFB	-0.3	+5	V
PRO	-0.3	+5	V
D (to S)	- 0.3	+700V	V
Continuous Power Dissipation (T_A = +25°C)	-	1.8	W
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V_{CC}	10	25	V
Ambient Temperature	-40	+125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	7 Ld PDIP	θ_{JA}[1]	Junction to ambient	70	°C/W
		θ_{JC}[2]	Junction to case	11.4	°C/W

1. θ_{JA} is measured on a FR4 1oz PCB with copper size of 150mm^2 on pin 6, 7, and 1 at 25°C ambient.
2. θ_{JC} is measured from the center of pin 6 and 7 and close to the plastic body.

3.4 Electrical Specifications

Typical operating conditions at 25°C, V_{DRAIN} = 375V, V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Startup and Power FET						
Internal V_{CC} Startup Current	I_{VCC_START}	V_{CC} = 8, V_{DRAIN} = 100V	-	3.6	-	mA
Drain Leakage Current	I_{D_LEAK}	V_{CC} = 0, V_D = 375V, V_{FB} = 0V	-	1	-	µA
Drain Bias	I_{D_BIAS}	V_{CC} = 12, V_{DRAIN} = 375V	-	-	10	µA
Power FET Breakdown Voltage	$V_{(BR)DSS}$	T_J = 25°C	700	-	-	V

Typical operating conditions at 25°C, V_{DRAIN} = 375V, V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Power FET On-Resistance	$r_{DS(ON)}$	T_J = 25°C, V_{CC} = 12V, I_{DS} = 300mA	-	5	7	Ω
		T_J = 125°C	-	10	12.5	Ω
Power FET Output Capacitance	C_{OSS}	V_{DS} = 25V, V_{GS} = 0V	-	30	-	pF
V_{CC} Supply						
V_{CC} Start (Rising)/HV Regulator Off	V_{CC_START}	V_{HV} = 100V	10.7	12	13	V
V_{CC} (Falling) /HV Regulator On	V_{CC_HVON}	V_{HV} = 100V	9	10	11	V
HV Regulator On/Off Hysteresis	V_{VCC_HYS}	-	-	1.7	-	V
V_{CC} Undervoltage Threshold (Falling)	V_{CC_UVLO}	IC stop switching	7.4	8	8.6	V
V_{CC} OV Clamping Threshold	V_{CC_CLP}	-	20.5	23	24.7	V
V_{CC} OV Latch Threshold	V_{CC_OVL}	-	24.7	27	30	V
V_{CC} Quiescent Current	I_{VCC_Q}	V_{FB} = 0V, no switching	-	620	877	µA
V_{CC} Current During Switching	I_{VCC}	V_{FB} > 0.7V, f_{SW} = 65kHz, D = 0.4	-	1	1.38	mA
Current Sense						
Max Peak Current Sensing Voltage	V_{CS_MAX}	V_{FB} = 2.5V	860	970	1084	mV
SCP/SWP Threshold	V_{CS_SC}	Rs ≥ 0.55Ω	1370	1630	1990	mV
Minimum Peak Current Sensing Voltage	V_{CS_MIN}	V_{FB} = V_{BURH} when exiting burst mode	-	250	-	mV
Leading Edge Blank Time	t_{LEB}	-	248	305	372	ns
Feedback						
Transconductance	GM	V_{FB} to V_{CS}	-	0.46	-	V/V
FB Pin Pull-up Resistor	R_{FB}	-	14.5	19	-	kΩ
FB Threshold Entering Burst Mode	V_{BURL}	-	-	1.3	-	V
FB Threshold Exiting Burst Mode	V_{BURH}	-	-	1.56	-	V
FB Threshold For Overload Protection	V_{FB_OLP}	-	3.5	4.0	-	V
FB Internal Pull-up Voltage	V_{FB_MAX}	-	-	4.9	-	V
Input Undervoltage Protection (Brown-In/Brown-Out)						
PRO Pin UV Rising Threshold	$V_{PRO\_UV\_R}$	-	2.4	2.6	2.9	V
PRO Pin UV Falling Threshold	$V_{PRO\_UV\_F}$	-	2.2	2.5	2.8	V
PRO Pin Clamp Threshold	V_{PRO_CLP}	-	3.1	3.5	3.9	V
Frequency						
Oscillator Frequency	f_{SW}	-	57.2	65	68	kHz
Dithering	-	Percent frequency	-5	-	5	%
Timing						
Maximum Duty Cycle	D_{MAX}	f_{SW} = 65kHz	76	77	79	%
Startup Timer	T_{ST}	2048 cycles, 65kHz	-	31	-	ms
Hiccup Restart Delay	T_{HICC}	32768 cycles, 65kHz	-	504	-	ms

Typical operating conditions at 25°C, V_{DRAIN} = 375V, V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
OLP/OCP Delay Timer	T_{OLP}	4096 cycles, f_{SW} = 65kHz, V_{FB} > 4.5V	-	63	-	ms
V_{IN}UV Delay Timer	T_{VINUV}	4096 cycles, f_{SW} = 65kHz	-	63	-	ms
Thermal						
Over-Temperature Threshold	OTP_{TH}	-	-	150	-	°C
Over-Temperature Hysteresis	OTP_{HYS}	-	-	30	-	°C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Performance Graphs

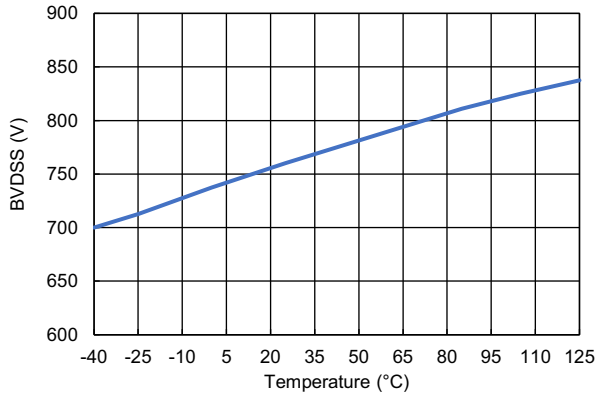


Figure 4. Breakdown Voltage vs Temperature

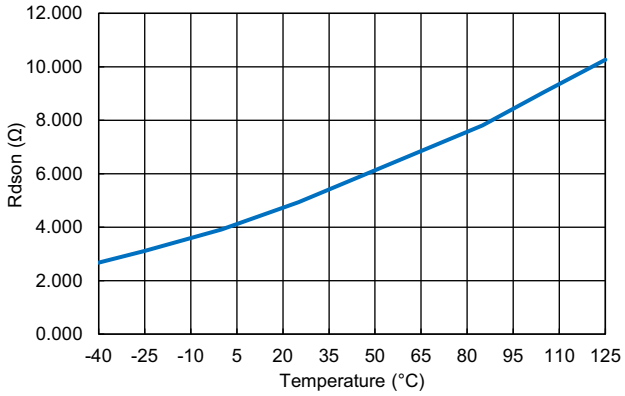


Figure 5. $r_{DS(ON)}$ vs Temperature

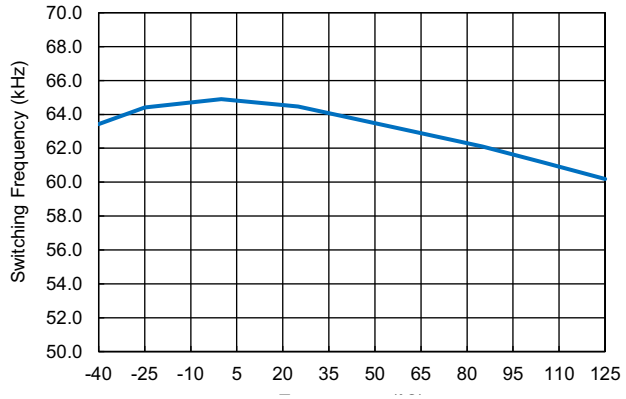


Figure 6. Switching Frequency vs Temperature

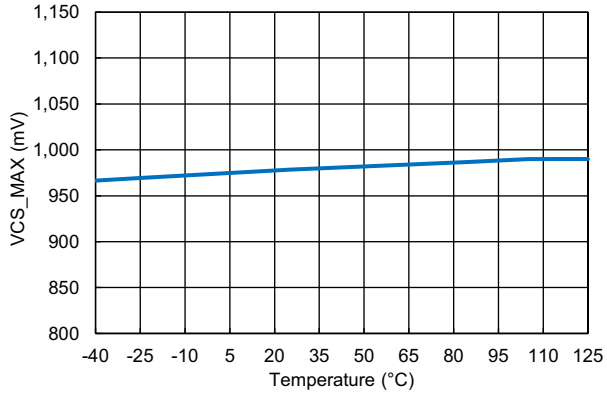


Figure 7. Maximum Current Sensing Threshold vs Temperature

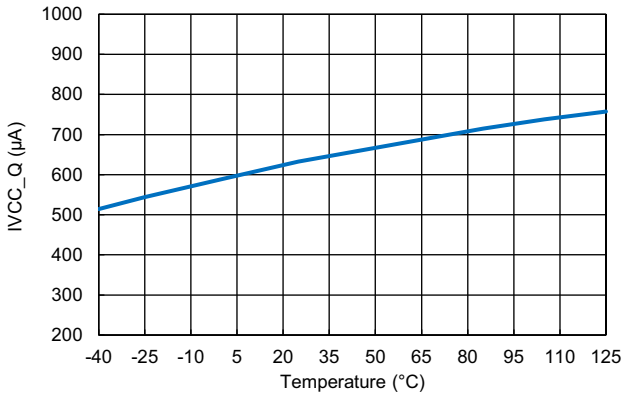


Figure 8. V_{CC} Quiescent Current vs Temperature

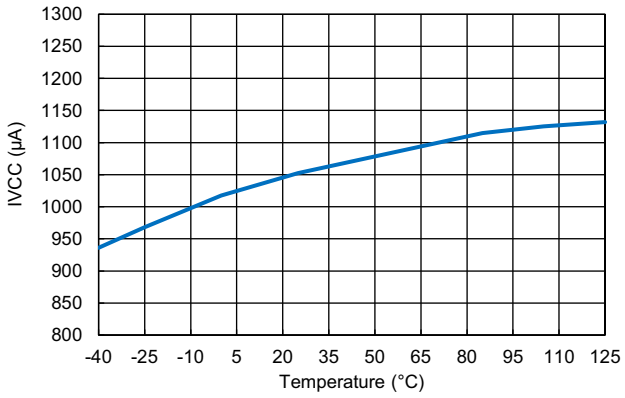


Figure 9. V_{CC} Supply Current in Switching vs Temperature

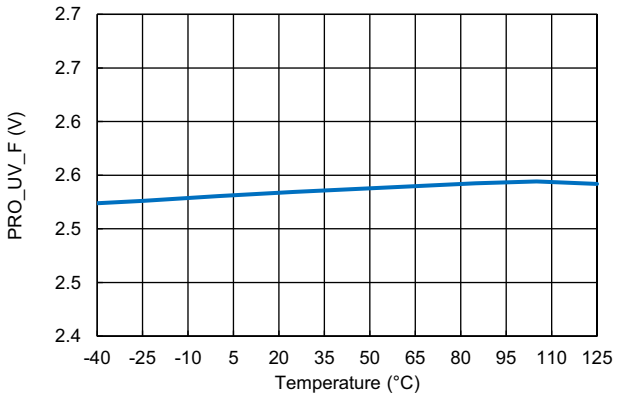


Figure 10. Input Undervoltage Threshold (Falling) vs Temperature

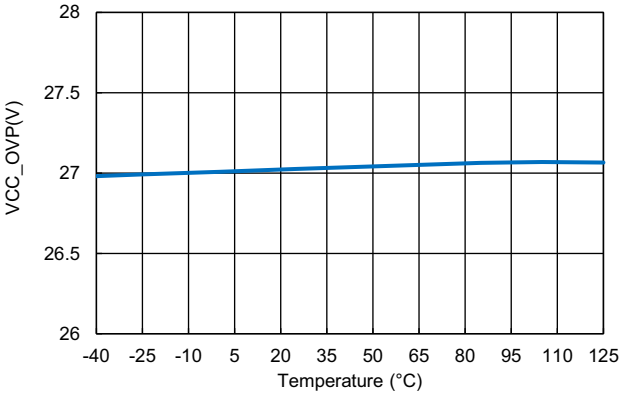


Figure 11. V_{CC} Overvoltage Protection Threshold vs Temperature

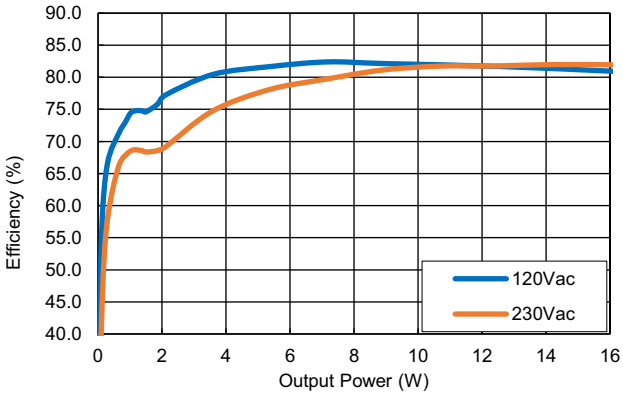


Figure 12. Efficiency

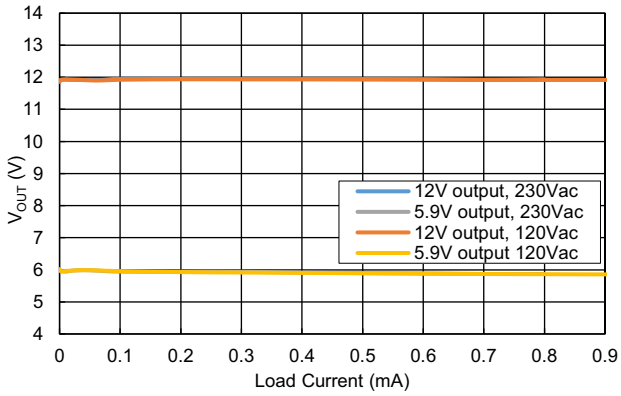


Figure 13. Load Regulation

Typical Waveforms (V_{IN} = 230Vac, V_{O1} = 12V, V_{O2} = 5.9V, I_{O1} = I_{O2} = 0.9A, T_A = 25°C, Figure 26, L_{PRI} = 750µH, C_{O1} = 1000µF)

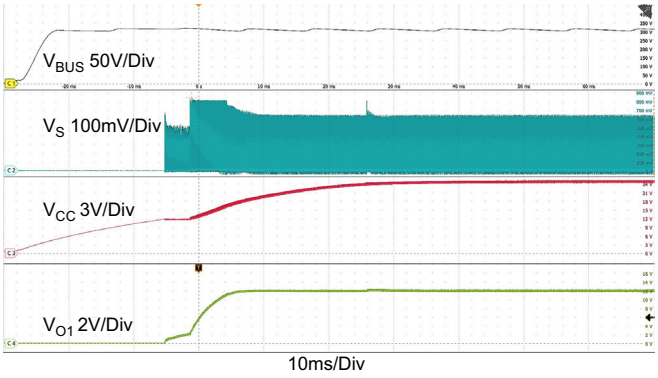


Figure 14. Startup

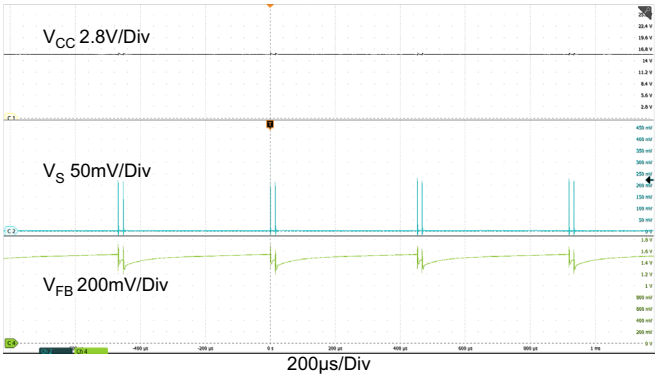


Figure 15. Light Load Operation

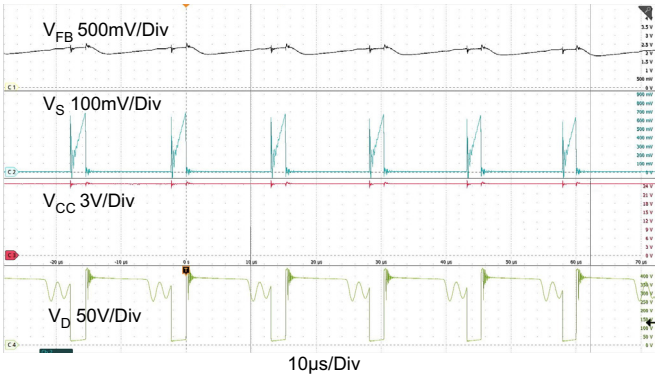


Figure 16. Full Load Operation

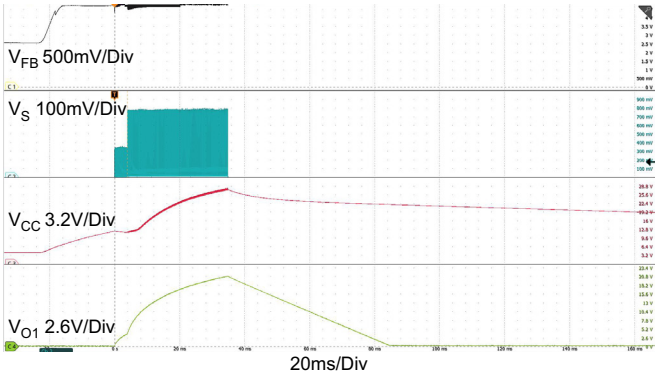


Figure 17. Feedback Open-Loop Protection

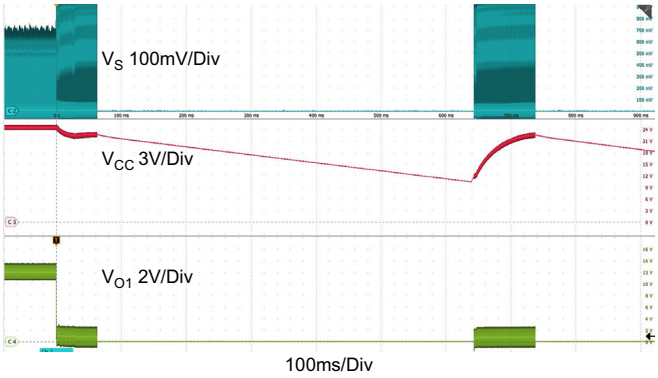


Figure 18. Short-Circuit Protection

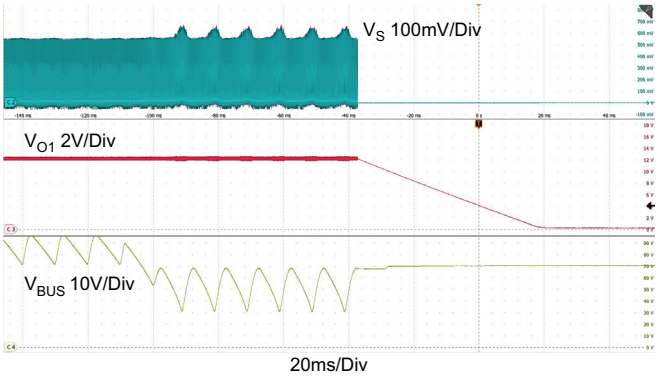


Figure 19. Input Undervoltage Protection (70Vac - 50Vac)

Typical Waveforms (V_{IN} = 230Vac, V_{O1} = 12V, V_{O2} = 5.9V, I_{O1} = I_{O2} = 0.9A, T_A = 25°C, Figure 26, L_{PRI} = 750µH, C_{O1} = 1000µF) (Cont.)

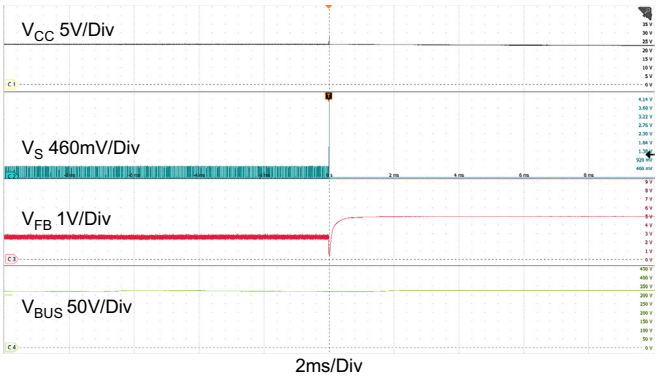


Figure 20. Short-Winding Protection

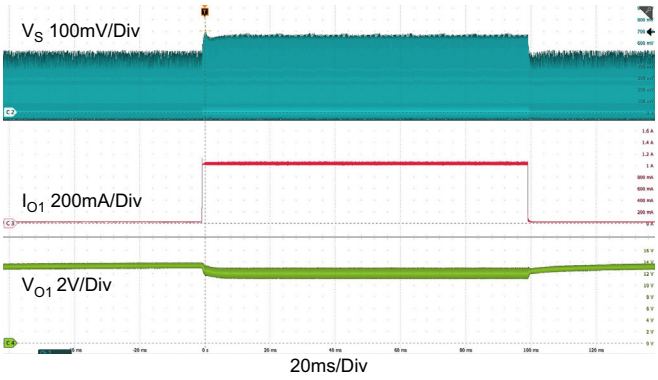


Figure 21. Step Load Response (I_{O1} = 10mA - 1A)

5. Functional Description

The RAA223881 can be configured as a constant frequency PWM flyback converter with secondary-side regulation (see Figure 22).

- Constant Frequency PWM Mode – At full load, the IC regulates the output voltage with a secondary-side error amplifier (TL431). The error signal is sent to the FB pin through an optocoupler. The FB voltage level controls the peak current in every switching cycle. The turn-on point is set by the internal fixed frequency oscillator.
- Burst Mode – At light load, the regulator transitions into the burst mode operation to save IC power consumption. While the load decreases, the FB voltage reduces. When the load drops below V_{BURL}, the part enters burst mode operation, and the IC stops switching. When FB voltage rises back to V_{BURH}, the IC resumes switching until FB voltage falls back to V_{BURL}. In Burst mode, the peak current is typically not more than V_{CS_MIN}/R_S excluding the overshoot, and the burst frequency is below 3kHz, which effectively minimizes the audible noises. See the Burst mode operation in Figure 23.

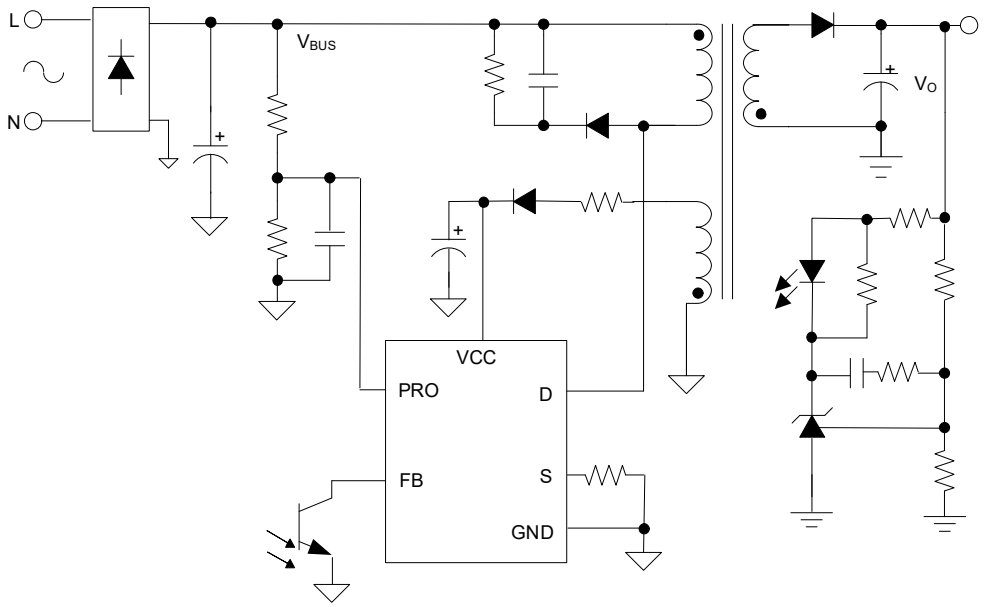


Figure 22. Flyback Application Circuit

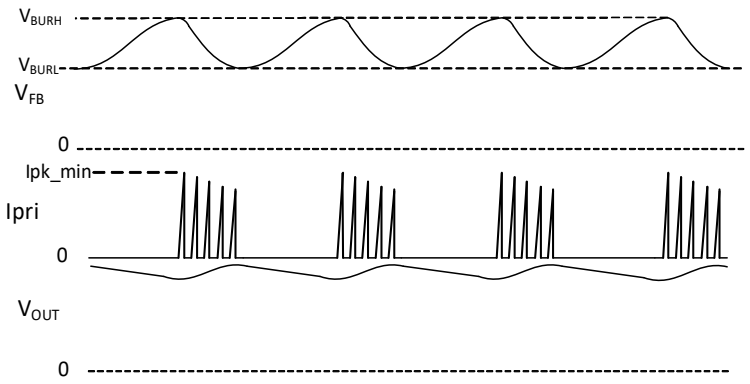


Figure 23. Burst Mode Operation at Light Load

5.1 Soft Start-Up

When the input voltage (rectified bus) is higher than the input undervoltage setpoint programmed by the PRO pin resistors, V_{CC} charges up by an internal HV current source. When V_{CC} reaches V_{CC_START}, the IC begins switching, and a startup timer begins (~31ms). The internal HV current source turns off until V_{CC} drops below V_{CC_HVON} where it turns on again. During the startup, the IC enables two steps of peak current limits so that the output gradually charges and implements a soft startup. The SCP disables during the startup blanking time. With V_{OUT} established, the auxiliary winding supplies V_{CC}, and the internal HV current source disables to keep power consumption low. See the startup process in Figure 24.

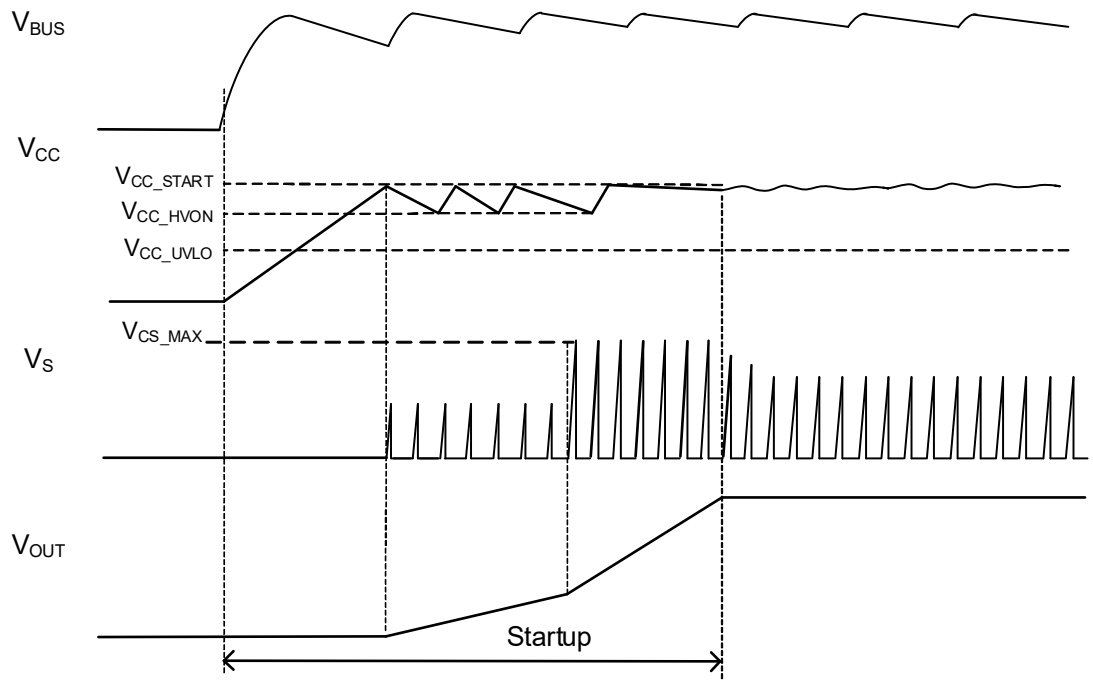


Figure 24. Start-Up Diagram

5.2 Brown-In and Brown-Out Protection

Brown-in and brown-out protection each stop the IC switching when the input voltage is too low; as a result, this protection prevents the input current from going too high. The IC detects low input voltage using the PRO pin when it is connected to a resistor divider from the rectified DC bus (see Figure 22).

When a low input voltage is applied and the PRO pin voltage is less than $V_{PRO\_UV\_R}$, the IC does not switch until the input voltage is increased so that the PRO pin voltage exceeds $V_{PRO\_UV\_R}$. The IC starts switching if V_{CC} is equal or above V_{CC_START}.

When the AC input voltage decreases and the PRO pin voltage drops below $V_{PRO\_UV\_F}$, after a V_{IN}UV delay time of 63ms, the IC stops switching. When the AC input voltage increases and the PRO pin voltage rises above $V_{PRO\_UV\_R}$, IC switching is enabled. *Note:* To have an effective brown-out when AC voltage is low, a small capacitor with a sufficient value is required to filter out the ripple voltage so that the brown-out protection is not defeated by the ripple peak by the end of the delay time.

With a normal input voltage, the PRO pin voltage is internally clamped at a voltage between 3.5V and 5V, determined by the values of the PRO pin resistor divider.

5.3 Overload and Short-Circuit Protection

When an overload or a short-circuit occurs, V_{FB} increases. When V_{FB} reaches V_{FB_OLP}, a fault delay timer starts. If V_{FB} is still greater than V_{FB_OLP} after the timer expires (~63ms), the IC stops switching for a hiccup time of approximately 504ms. Next, the IC attempts a normal soft-start sequence after the hiccup timer expires. The logic sequence appears in Figure 25.

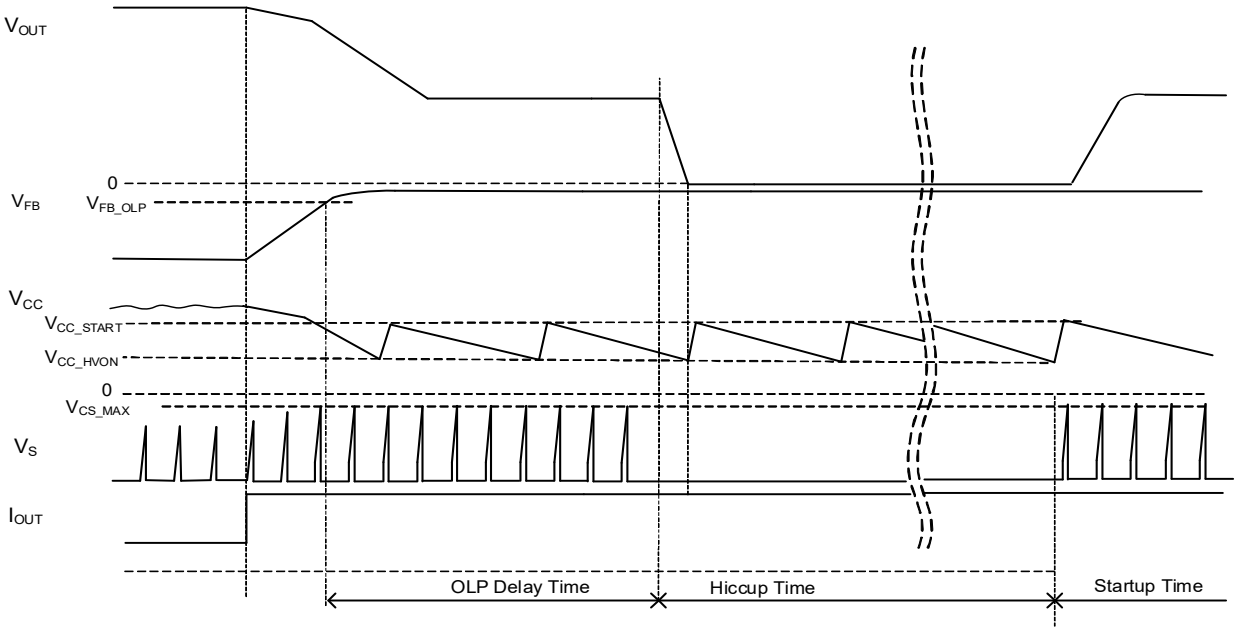


Figure 25. Overload Protection Diagram

5.4 Short-Winding Protection

The short-winding protection protects the IC from a catastrophic failure resulting from either an accidental transformer winding short or a secondary-side diode short; when these shorts occur, the primary side current quickly rises to a dangerous level within a short time that is usually within the normal blanking time. The IC detects it when the sensed voltage on the S pin reaches to V_{CS_SC}. Finally, the IC quickly turns off the power FET and latches off (the whole IC) until the V_{CC} drops below V_{CC_UVLO} or the input is recycled.

5.5 V_{CC} Overvoltage Protection and Open-Loop Protection

When V_{CC} increases to V_{CC_CLP}, an internal clamp (~5mA) is activated, preventing V_{CC} from going higher. If V_{CC} continues to increase up to V_{CC_OVL}, the IC is latched off, unless V_{CC} drops below V_{CC_UVLO} or the input is recycled.

When the feedback loop is open, V_{FB} rises up to the maximum, demanding the maximum peak current. As a result, V_{OUT} goes beyond the regulation point. This is detected by the auxiliary winding. With a proper turns ratio of auxiliary winding to the output winding, V_{CC} rises up to the V_{CC_OVL} when V_{OUT} surpasses the regulation point, and IC is latched off. The latch-off releases when V_{CC} drops below V_{CC_UVLO} or the input is recycled.

6. Application Topologies

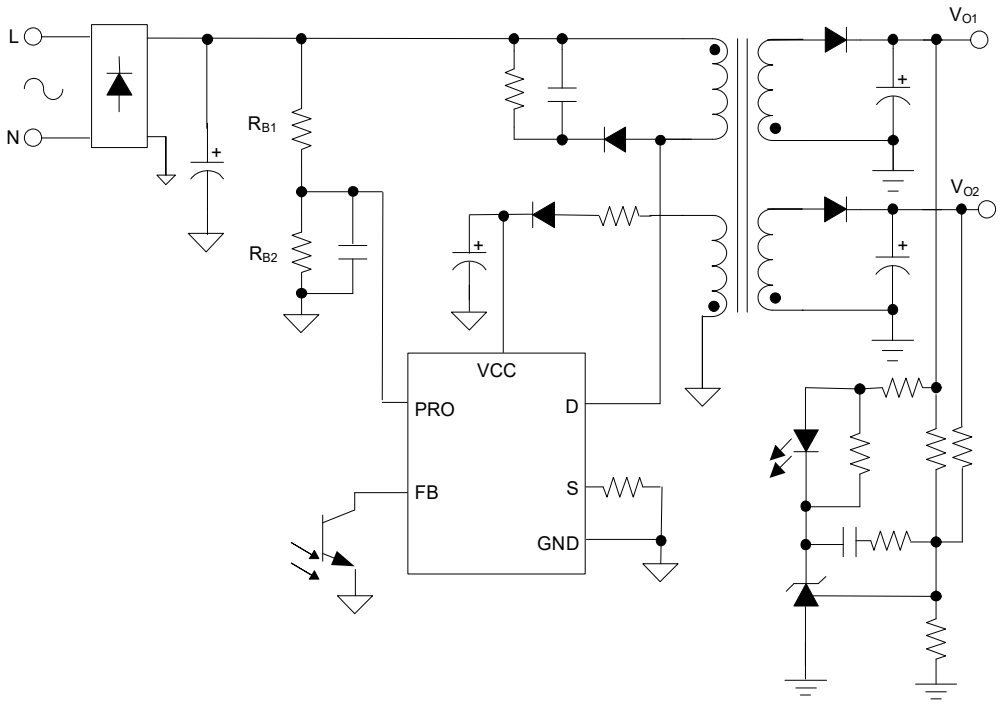


Figure 26. Dual-Output Flyback with Input Brown-In/Brown-Out Protection

7. Design Guidance

7.1 Input Bulk Capacitor

The input bulk capacitor (C_{IN} in Figure 26) provides a DC voltage with some ripple voltage for the flyback. The lowest bus voltage determines that the power flyback can deliver. Equation 1 calculates the required minimum bus valley voltage for the target output power level. To keep the bus valley above this value, the bulk capacitor value must be high enough to support maximum output power at the lowest expected input voltage. The required capacitance is calculated by using Equation 2, where I_{PKMAX} is the max peak current required for full load operation. The value η is the assumed full load efficiency at the minimum AC line input voltage.

(EQ. 1)
$$V_{busmin} = \frac{2P_{OUT}}{\eta I_{PKMAX} D_{MAX}}$$

(EQ. 2)
$$C_{in} = \frac{P_{OUT}\left(0.25 + \frac{1}{2\pi}\operatorname{asin}\frac{\sqrt{2}V_{acmin} - V_{busmin}}{\sqrt{2}V_{acmin}}\right)}{\eta V_{acmin}(\sqrt{2}V_{acmin} - 70)f_{LINE}}$$

7.2 Transformer Primary Inductance and Turns Ratio

The primary inductance must be small enough so that inductor current can hit the required peak current at the bus voltage valley for full load operation at the minimum input voltage. The primary inductance also needs to be big enough to maintain a CCM operation at full load when the bus voltage is at lowest point in the valley. Use Equation 3 and Equation 4 to select the inductor value. Renesas recommends choosing a maximum duty cycle that is smaller than the controller's DMAX value. To ensure a stable operation without subharmonics and power limiting, Renesas recommends using a maximum duty cycle between 0.5 to 0.6 in applications.

(EQ. 3)
$$L_P > \frac{\eta D^2_{MAX} V^2_{busmin}}{2 f_{SW} P_{OUT}}$$

(EQ. 4)
$$L_P < \frac{D_{MAX} V_{busmin}}{f_{SW} I_{PKFL}}$$

Use Equation 5 to calculate the transformer turns ratio. Because the bus voltage can be as low as V_{busmin}, Renesas recommends using a D_{max} value of 0.5~0.6 to avoid an excessively high duty cycle.

(EQ. 5)
$$N \le \frac{V_{busmin}}{V_F + V_o} \bullet \frac{D_{max}}{1 - D_{max}}$$

Alternately, the turns ratio should not be too small either; select a high turns ratio according to Equation 5 to minimize the voltage rating of the secondary diodes, which also maximizes efficiency.

7.3 Current Sensing Resistor

The peak current is sensed through R_{SENSE} on the S pin. The voltage on the S pin is compared with the internal current command voltage. When the sensed voltage reaches the current command voltage level, the MOSFET turns off. The internal current sense voltage limit, V_{CS_MAX} determines maximum peak current in the primary

winding. The value of R_{SENSE} is calculated by Equation 6. *Note*: R_{SENSE} must be evaluated for proper power capability.

(EQ. 6) $$R_{SENSE} = \frac{V_{CSMAX}}{I_{PKMAX}} - 0.1$$

7.4 PRO Pin Resistors

The resistor divider must be calculated to ensure that V_{IN} UV protection engages at the appropriate bus voltage. To limit the resistor power loss <10mW, Renesas recommends that $R_{B1} \geq 10M\Omega$. Therefore, R_{B2} is calculated with Equation 7.

(EQ. 7) $$R_{B2} = \frac{V_{PRO\_UV\_F}}{V_{VINUV} - V_{PRO\_UV\_F}} \bullet R_{B1}$$

Where V_{IN}UV is the required minimum bus voltage to allow switching, and is usually chosen slightly below the minimum bus valley voltage for a chosen C_{IN}. Because the UV detection has a time delay longer half line cycle, a small ceramic cap of 3.3nF~6.8nF in parallel to R_{B2} should be enough to filter out most ripple voltage.

7.5 Output Capacitance

The minimum output capacitance is chosen by considering allowable switching ripple, step load response requirements, and in some applications, the required output hold-time when the input shuts off.

Use the RAA223881 calculation tool to determine all these values.

7.6 PCB Layout Guidance

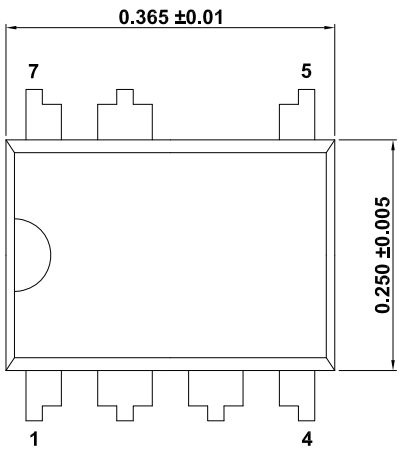
Proper layout is important to ensure a stable operation, good thermal behavior, EMI performance, and reliable operation for various operating environments. Follow these layout recommendations for an optimal design.

1. Leave proper spacing (recommend minimum 1.5mm) between high voltage (max 400V) traces and low voltage traces.
2. Keep a small loop from the input filter capacitor to the transformer primary winding, IC D pin, and IC S pin to the ground of the input capacitor. On the output side, maintain a small loop from the transformer secondary winding, output diode, and output capacitor to the return terminal of the secondary winding.
3. Keep sufficient copper area on the IC drain pin (not less than $150mm^2$ for 17W output power) for a better thermal performance.
4. Place the V_{CC} decoupling cap close to the pin.

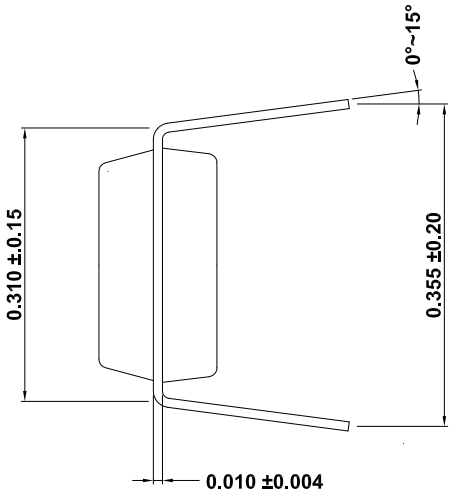
8. Package Outline Drawing

For the most recent package outline drawing, see E7.3.

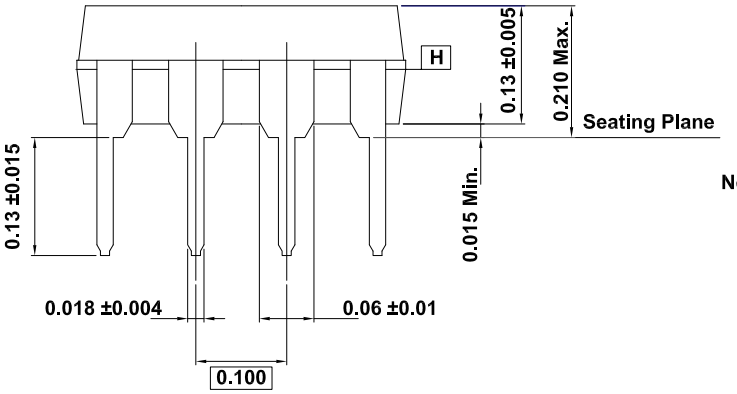
E7.3
7 Lead Plastic Dual Inline Package (PDIP)
Rev 1, 4/2022



Top View



Side View



Side View

Notes:

1. Jedec outline: N/A.
2. D, E1 Dimensions do not include mold flash or protrustions. Mold flash or protrusions exceed 0.010 inch.
3. eB is measured at the lead tips with the leads unconstrained.
4. Pointed or rounded lead tips are with preferred to ease insertion.
5. Distance between leads including dam bar protrusions are 0.005 inch minimum.
6. Datum plane H coincident with the bottom of lead, where lead exits body.

9. Ordering Information

Part Number[1]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type	Temp. Range
RAA2238814GSP#AA1	223881	7 Ld PDIP	E7.3	Tube	-40 to +150°C
RTKA223881DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations).

10. Revision History

Revision	Date	Description
1.00	Apr 1, 2024	Initial release.

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