The RAA223012 is a universal input AC/DC switching buck regulator with ultra-low standby power that features a 700V integrated MOSFET capable of delivering up to 2.5W output power (Table 1). It supports output voltage as low as 3.3V.

The RAA223012 combines constant off-time control for heavy load and Pulse Frequency Modulation (PFM) for light-load operation. Constant off-time controls switching frequency above the audible frequency of approximately 50kHz. PFM eliminates any potential audible noises while offering superior light-load efficiency and ultra-low power consumption (<10mW at no load). Efficiency is achieved up to 75%. The built-in frequency dithering further reduces the EMI noise spectrum.

The RAA223012 also features input brownout protection that prevents input circuitry from the overcurrent at low input voltage, and hiccup protections for output fault conditions such as short-circuit, overload, and open feedback.

The RAA223012 is available in a small 5 Ld TSOT23 and 8 Ld SOIC packages.

### Features
- Ultra low standby power (<10mW)
- No audible noise
- Low quiescent current (<100µA)
- Output voltage as low as 3.3V
- Low EMI with frequency dithering
- 5 Ld TSOT23 and 8 Ld SOIC package options
- Programmable PFM allows optimization of C\text{OUT} for various standby power requirements
- Protection features: Short-Circuit Protection (SCP), Overload Protection (OLP), Open Feedback Protection, and Over-Temperature Protection (OTP).

### Applications
- Home appliances
- Home automation, IoT, and sensors
- Metering and Industry control
- Bias power

#### Table 1. Maximum Output Current (Max. Ambient 85°C)

<table>
<thead>
<tr>
<th>V_{OUT} (V)</th>
<th>120V_{AC}</th>
<th>230V_{AC}</th>
<th>85V_{AC}~265V_{AC}</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>100mA</td>
<td>100mA</td>
<td>100mA</td>
</tr>
<tr>
<td>12</td>
<td>140mA</td>
<td>140mA</td>
<td>140mA</td>
</tr>
<tr>
<td>5</td>
<td>185mA</td>
<td>195mA</td>
<td>170mA</td>
</tr>
<tr>
<td>3.3</td>
<td>190mA</td>
<td>190mA</td>
<td>190mA</td>
</tr>
</tbody>
</table>

#### Figure 1. Typical RAA223012 Buck Application Circuit
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1. Overview

1.1 Block Diagram

Figure 2. Block Diagram of RAA223012
2. Pin Information

2.1 Pin Assignments

![Pin Assignments Diagram]

2.2 Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 VCC</td>
<td>IC supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>2 FB</td>
<td>Feedback pin, 2.5V ±4%</td>
</tr>
<tr>
<td>3</td>
<td>3 GND</td>
<td>IC ground, externally connected to the SOURCE pin</td>
</tr>
<tr>
<td>4</td>
<td>4 SOURCE</td>
<td>Internal power MOSFET source</td>
</tr>
<tr>
<td>5</td>
<td>7 DRAIN</td>
<td>Internal power MOSFET drain</td>
</tr>
<tr>
<td>5, 6, 8</td>
<td>N/C</td>
<td>Not connected</td>
</tr>
</tbody>
</table>

3. Specifications

3.1 Absolute Maximum Ratings

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>-0.3</td>
<td>+6.5</td>
<td>V</td>
</tr>
<tr>
<td>VFB</td>
<td>-0.3</td>
<td>+6.5</td>
<td>V</td>
</tr>
<tr>
<td>DRAIN (to SOURCE)</td>
<td>- 0.3</td>
<td>700</td>
<td>V</td>
</tr>
<tr>
<td>Continuous Power Dissipation (T_A = +25°C)</td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>ESD Rating</td>
<td>Value</td>
<td></td>
<td>Unit</td>
</tr>
<tr>
<td>Human Body Model (Tested per JS-001-2017)</td>
<td>1.2</td>
<td></td>
<td>kV</td>
</tr>
<tr>
<td>Charged Device Model (Tested per JS-002-2014)</td>
<td>1</td>
<td></td>
<td>kV</td>
</tr>
<tr>
<td>Latch-Up (Tested per JESD78E; Class 2, Level A)</td>
<td>100</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>
3.2 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Resistance (Typical)</th>
<th>$\theta_{JA} ,(\degree C/W)[1]$</th>
<th>$\theta_{JC} ,(\degree C/W)[2]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Ld TSOT23</td>
<td>80</td>
<td>71</td>
</tr>
<tr>
<td>8 Ld SOIC</td>
<td>86</td>
<td>57</td>
</tr>
</tbody>
</table>

1. $\theta_{JA}$ is measured on single layer 1oz evaluation PCB with 218mm² thermal copper connected to the SOURCE and DRAIN pins, in free air.
2. For $\theta_{JC}$, the case temperature location is taken at the package top center.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Junction Temperature</td>
<td></td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum Storage Temperature Range</td>
<td>-60</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Pb-Free Reflow Profile</td>
<td></td>
<td>See TB493</td>
<td></td>
</tr>
</tbody>
</table>

3.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, V_DRAIN</td>
<td></td>
<td>375</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>3.3</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

3.4 Electrical Specifications

Typical operating conditions at 25°C, V_DRAIN = 100V, V_CC = 5.6V, T_J = -40 to +125°C, unless otherwise specified.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Startup and Power FET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal V_CC Startup Current</td>
<td>$I_{VCC_START}$</td>
<td>$V_{CC} = 4V$</td>
<td>1.6</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Drain Leakage Current</td>
<td>$I_{D_LEAK}$</td>
<td>$V_{CC} = 0V, V_{DRAIN} = 375V, V_{FB} = 2.6V$</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{D_BIAS}$</td>
<td>$I_{D_BIAS}$</td>
<td>$V_{CC} = 5.9V, V_{DRAIN} = 375V$</td>
<td>5</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Power FET Breakdown Voltage</td>
<td>$V_{DS(\text{BR})}$</td>
<td>$T_J = 25°C$</td>
<td>700</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Power FET On-Resistance</td>
<td>$r_{DS(\text{ON})}$</td>
<td>$T_J = 25°C, V_{CC} = 5.8V, I_{DS} = 200mA$</td>
<td>14.5</td>
<td>17</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = 125°C$</td>
<td></td>
<td></td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td>V_CC Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_CC Start (Rising)</td>
<td>$V_{CC_START}$</td>
<td></td>
<td>5.5</td>
<td>5.9</td>
<td>6.3</td>
<td>V</td>
</tr>
<tr>
<td>V_CC when Internal Regulator Off</td>
<td>$V_{CC_OFF}$</td>
<td></td>
<td>5.5</td>
<td>5.9</td>
<td>6.3</td>
<td>V</td>
</tr>
<tr>
<td>V_CC (Falling) Regulator On at Startup</td>
<td>$V_{CC_ON}$</td>
<td></td>
<td>5.2</td>
<td>5.55</td>
<td>5.9</td>
<td>V</td>
</tr>
<tr>
<td>Internal V_CC On/Off Hysteresis</td>
<td>$V_{CC_HYS}$</td>
<td></td>
<td>0.3</td>
<td>0.35</td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>V_CC (Falling) Regulator On after Startup</td>
<td>$V_{CC_ON_SS}$</td>
<td></td>
<td>4.25</td>
<td>4.5</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td>V_CC Undervoltage Threshold (Falling)</td>
<td>$V_{CC_UVLO}$</td>
<td>IC stop switching</td>
<td>3.15</td>
<td>3.4</td>
<td>3.55</td>
<td>V</td>
</tr>
<tr>
<td>V_CC Shunt Regulator On (Rise)</td>
<td>$V_{CC_SON}$</td>
<td>External V_CC supply, internal shunt on</td>
<td>6.15</td>
<td>6.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_CC Shunt Regulator Off (Fall)</td>
<td>$V_{CC_SOFF}$</td>
<td></td>
<td>6.1</td>
<td>6.4</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
Typical operating conditions at 25°C, \( V_{\text{DRAIN}} = 100\text{V}, V_{\text{CC}} = 5.6\text{V}, T_J = -40\) to +125°C, unless otherwise specified. (Cont.)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{CC}} ) Quiescent Current</td>
<td>( I_{\text{VCC_Q}} )</td>
<td>( V_{FB} &gt; 2.5\text{V}, ) no switching, ( V_{\text{CC}} = 5.6\text{V} )</td>
<td>70</td>
<td>103</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{CC}} ) Current During Switching</td>
<td>( I_{\text{VCC}} )</td>
<td>( V_{FB} &lt; 2.5\text{V}, ) switching frequency = 50kHz, ( D = 0.15, ) ( V_{\text{CC}} = V_{\text{CC_ON}} + 0.1\text{V} )</td>
<td>130</td>
<td>200</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{CC}} ) Discharging Current Hiccup Timing</td>
<td>( I_{\text{QVCC3}} )</td>
<td>( V_{\text{CC}} ) discharge current for timing of fault hiccup delay</td>
<td>19</td>
<td>30</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td><strong>Current Sense</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Current Limit</td>
<td>( I_{\text{PK}} )</td>
<td>( V_{FB} &lt; 2.5\text{V}, ) ( \text{di/dt} = 0.5\text{A/µs}, V_{\text{CC}} = 5.8\text{V} )</td>
<td>260</td>
<td>335</td>
<td>400</td>
<td>mA</td>
</tr>
<tr>
<td>SCP Threshold</td>
<td>( I_{\text{SC_TH}} )</td>
<td></td>
<td>710</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Minimum Peak Current</td>
<td>( I_{\text{PKMIN}} )</td>
<td>( \text{di/di} = 0.5\text{A/µs}, V_{\text{CC}} = 5.8\text{V} )</td>
<td>150</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Leading Edge Blank Time</td>
<td>( t_{\text{LEB}} )</td>
<td></td>
<td>192</td>
<td>230</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>Feedback</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Feedback Voltage</td>
<td>( V_{FB} )</td>
<td></td>
<td>2.4</td>
<td>2.5</td>
<td>2.63</td>
<td>V</td>
</tr>
<tr>
<td>Transconductance</td>
<td>( G_{M} )</td>
<td>( I_{\text{PK}} ) ( G_{M}, V_{\text{CC}} = 5.8\text{V} )</td>
<td>7</td>
<td></td>
<td></td>
<td>mS</td>
</tr>
<tr>
<td>Feedback Undervoltage Threshold</td>
<td>( V_{\text{FB_UV}} )</td>
<td>( V_{\text{CC}} = 5.7\text{V} )</td>
<td>1.6</td>
<td>1.7</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>Feedback Threshold for Increased Off-Time</td>
<td>( V_{\text{FB_TOFFMIN}} )</td>
<td>( V_{\text{CC}} = 5.0\text{V} )</td>
<td>0.67</td>
<td>0.84</td>
<td>0.98</td>
<td>V</td>
</tr>
<tr>
<td>Feedback Overvoltage</td>
<td>( V_{\text{FB_OV}} )</td>
<td></td>
<td>2.75</td>
<td>3</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td><strong>Timing</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>( t_{\text{OFF_MIN}} )</td>
<td>( V_{\text{CC}} = 5.0\text{V} )</td>
<td>15</td>
<td>19</td>
<td>24</td>
<td>µs</td>
</tr>
<tr>
<td>Maximum On-Time</td>
<td>( t_{\text{ON_MIN}} )</td>
<td>( V_{\text{CC}} = 5.0\text{V} )</td>
<td>12</td>
<td>15</td>
<td>18</td>
<td>µs</td>
</tr>
<tr>
<td>Minimum Off-Time in Short-Circuit</td>
<td>( t_{\text{OFFMIN_SC}} )</td>
<td>( V_{\text{CC}} = 5.0\text{V} )</td>
<td>200</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Hiccup Restart Delay</td>
<td>( t_{\text{HICC}} )</td>
<td>( C_{\text{VCC}} = 1\mu\text{F} )</td>
<td>100</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Startup Blanking Time, OLP Time</td>
<td>( t_{\text{OLP}} )</td>
<td>( f_{\text{SW}} = 50\text{kHz}, V_{FB} &lt; 1.7\text{V}, V_{\text{CC}} = 5.0\text{V} )</td>
<td>1024</td>
<td></td>
<td></td>
<td>cycle</td>
</tr>
<tr>
<td><strong>Thermal</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over-Temperature Threshold</td>
<td>( O_{TP_TH} )</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Over-Temperature Hysteresis</td>
<td>( O_{TP_HYS} )</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
4. Typical Characterization Graphs

**Figure 3. Breakdown Voltage vs Temperature**

**Figure 4. On-Resistance vs Temperature**

**Figure 5. Peak Current Limit vs Temperature**

**Figure 6. \( V_{CC} \) Start/Upper Limit vs Temperature**

**Figure 7. \( V_{CC} \) Undervoltage Threshold vs Temperature**

**Figure 8. IC Quiescent Current vs temperature**
Figure 9. Minimum Off-Time vs Temperature

\[ t_{OFF\_MIN} \] vs Temperature (°C)

Figure 10. Feedback Voltage vs Temperature

\[ V_{FB} \] vs Temperature (°C)

\( V_{IN} = 230V_{AC}, V_{OUT} = 6.5V, I_{OUT} = 100mA, L = 680\mu H, C_o = 100\mu F, T_A = 25°C \)

Figure 11. Startup

Figure 12. Shutdown

Figure 13. Full Load Operation

Figure 14. Light-Load Operation
$V_{\text{IN}} = 230\text{VAC}, V_{\text{OUT}} = 6.5\text{V}, I_{\text{OUT}} = 100\text{mA}, L = 680\mu\text{H}, C_0 = 100\mu\text{F}, T_A = 25^\circ\text{C}$ (Cont.)

**Figure 15. Overload protection**

**Figure 16. Short-Circuit Protection**

**Figure 17. Input Brownout Protection**

**Figure 18. Load Transient (10mA to 100mA)**

**Figure 19. Efficiency ($V_{\text{OUT}} = 6.5\text{V}$)**

**Figure 20. Load Regulation ($V_{\text{OUT}} = 6.5\text{V}$)**
5. Detailed Description

The RAA223012 adopts the high-side float switching topology as Figure 1 shows. A floating VCC supplies IC operation. The output voltage is sensed on the FB pin from an RC sampling network connected to the output, and compared with the internal reference through an error amplifier that controls the peak current accordingly.

5.1 Constant Off-Time Mode

In heavy load, the power FET is turned on after a constant off-time. Because the on-time is comparably much smaller than the off-time, the IC operates with quasi-constant frequency. When the load current goes lower, the peak current becomes lower while still switching around 50kHz until it hits the minimum peak current limit. Because the switching frequency is always kept around 50kHz in the operation, no audible noises can be heard.

5.2 PFM Mode

When the load current decreases below a certain value (see, the peak current is kept at the minimum level, while the off-time is gradually increased to maintain the output regulation. As a result, the frequency reduces. The IC goes into Pulse Frequency Modulation (PFM) operation, as Figure 21 shows, so losses are reduced due to switching frequency reduction. During this mode, while the switching frequency is reduced below 1kHz at no load, the audible noise is minimized by keeping the peak current at the minimum level. In the meantime, due to the low IC biasing current and small peak current, the standby power can be achieved below 10mW. The above operation is illustrated in Figure 22 and Figure 23.

![Figure 21. PFM Operation in Light Load](image)

![Figure 22. Switching Frequency vs IOUT](image)

![Figure 23. Peak Current vs Switching Current](image)

5.3 Output Voltage Sampling

The RC sampling network samples the output voltage through a forward biased D3 when D2 is free-wheeling. When the D2 cathode goes high and D2 stops conducting current, the sampled voltage across CFB1 is discharged by RFB1 and RFB2. In constant off-time operation, the FB pin voltage is slightly below the internal reference. The power FET is set on after a constant off-time. In PFM mode, when the sampled voltage on FB pin drops to internal...
reference, the power FET is clocked on. In this way, the light-load switching is set by the \( C_{FB1} \), \( R_{FB1} \), and \( R_{FB2} \) for the corresponding load. Therefore, the required no-load standby power is achieved by choosing \( C_{FB1} \), allowing you the flexibility to design your circuit for various standby power requirements. For detailed design guidance, see Feedback Capacitor (\( C_{FB1} \)) Selection.

### 5.4 Soft Start-Up

The RAA223012 starts up with the \( V_{CC} \) capacitor charged by an internal HV current source. When the \( V_{CC} \) reaches up to 5.9V, the IC begins switching, the internal HV current source is turned off, and a start-up timer begins. When \( V_{CC} \) drops below 5.5V, the HV current source is on again, which is determined by the actual IC supply current. During the start-up, the output voltage ramps up gradually, which is controlled by a variable off-time set by the feedback voltage. After the timer expires (start-up is finished), the HV current source is on again only when \( V_{CC} \) drops to 4.5V. When \( V_{OUT} \) is established, \( V_{CC} \) can be supplied by \( V_{OUT} \) (optional) to save power consumption for high efficiency and low standby power, see Figure 24.

![Figure 24. RAA223012 Low Standby Power Buck Regulator](image)

Figure 25 shows the start-up diagram.

![Figure 25. RAA223012 Start-Up Diagram](image)
5.5 Overload Protection

With the fixed minimum off-time (when $V_{FB} \geq 0.84\text{V}$), the maximum load current that the RAA223012 allows is limited for a given output voltage and inductor, and therefore, is the maximum output power (<5W). However, when the output voltage continues to drop during the overload, the FET power losses increase and can cause potential IC overheating. Therefore, when $V_{FB}$ reaches 1.7V an internal comparator is triggered and starts an Overload Protection (OLP) timer. When the timer is expired, the overload situation is identified, and the IC is shut off. $V_{CC}$ is discharged by a 19µA internal current source to 3.4V, and charged up to 5.9V to resume switching (the interval without switching is the hiccup time). The overload protection time sequence is shown in Figure 26.

![Figure 26. RAA223012 Overload Protection Diagram](image)

5.6 Short-Circuit Protection

When the output is shorted, $V_{OUT} = 0$, $V_{FB}$ drops to zero because of the feedback network, introducing a delay. Before $V_{FB}$ drops to $V_{FB,TOFFMIN}$, the RAA223012 operates with $T_{ONMAX}$ and $T_{OFFMIN}$, which quickly builds up a high current (>IPK) because the inductor peak current does not get reset. When the current reaches $I_{SC,TH}$, a timer is started. If the inductor current reaches $I_{SC,TH}$ for four consecutive cycles, the RAA223012 determines that a short-circuit is present and immediately shuts off switching. The IC then quickly charges $V_{CC}$ up to 5.9V and discharges it with a 19µA current source to 3.4V. When $V_{CC}$ drops to 3.4V, a 1.6mA current source charges $V_{CC}$ back to 5.9V where the IC resumes switching.

When the RAA223012 resumes switching, assuming $V_{FB}$ drops to zero, the IC operates with the increased $T_{OFFMIN,MAX}$ so the inductor current can fully reset below the maximum peak limit. The RAA223012 operates in CCM with the inductor peak current being limited at IPK, with an average current around 240mA during the short. The part remains in hiccup mode until the short is removed. When the short is removed, $V_{OUT}$ returns to normal. This procedure is shown in Figure 27.
Figure 27. RAA223012 Short-Circuit Protection Diagram
6. Application Topologies

Figure 28. RAA223012 Buck with Enhanced Efficiency and Low Standby Power

Figure 29. RAA223012 Buck with Enhanced Efficiency

Figure 30. RAA223012 Buck with Low BOM Cost

Figure 31. RAA223012 Buck/Boost
7. Design Guidance

7.1 Feedback Resistor Selection

The output voltage is set by the resistor divider of \(R_{FB1}\) and \(R_{FB2}\). Because of the diode forward voltage mismatch between the feedback diode D3 and free-wheeling diode D2, an additional 0.4 offset is added in Equation 1 to calculate the resistor values of \(R_{FB1}\) and \(R_{FB2}\).

\[
\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT} + 0.4}{V_{FB}} - 1
\]

(EQ. 1)

7.2 Output Inductor Selection

Because the buck regulator is designed with a constant off-time of 19µs at full load, design the output inductor according to Equation 2:

\[
L \geq \frac{V_{OUT} T_{OFF,MIN}}{2(\frac{I_{PK}}{I_{O,MAX}} - 1)}
\]

(EQ. 2)

For example, if \(V_{OUT} = 6.5V\), if \(I_{O,MAX} = 150mA\),

\[
L \geq \frac{6.5 \times 19 \times 10^{-6}}{2 \times (0.335 - 0.15)} = 333 \mu H
\]

L is chosen with a fixed value 470µH.

7.3 Feedback Capacitor (\(C_{FB1}\)) Selection

The feedback capacitor, \(C_{FB1}\), determines the pulse frequency at no load condition. The corresponding inductor current is shown in Figure 32.

![Figure 32. The Inductor Current at No Load Operation](image_url)

The average output current is written as Equation 3.

\[
I_{OUT,MIN} = \frac{I_{PK,MIN}(T_{ON} + T_{OFF})}{2T_{stb}}
\]

(EQ. 3)

Because \(T_{ON} << T_{OFF}\), \(I_{OUT,MIN}\) can be written as:
Therefore:

\[
\frac{I_{PK,MIN}T_{OFF}}{2T_{stb}} = I_{OUT,MIN}, \text{ where } T_{OFF} = \frac{L}{V_{OUT}}
\]

To have the required input standby power, \(P_{IN,STBY}\), the power delivered to the output should satisfy Equation 5:

\[
V_{OUT}I_{OUT,MIN} = P_{IN,STBY}\eta
\]

where \(\eta\) is the light-load efficiency.

Replacing \(I_{OUT,MIN}\) with Equation 4 gives you Equation 6:

\[
V_{OUT}\left(\frac{L}{2V_{OUT}T_{stb}}\right)^2 = P_{IN,STBY}\eta
\]

The required time interval \(T\) is calculated using Equation 7:

\[
T_{stb} = \frac{L}{2P_{IN,STBY}\eta}
\]

Because the time interval \(T_{stb}\) is primarily determined by the sampling network discharging time, it is related to \(C_{FB1}\) in Equation 8:

\[
C_{FB1} = \frac{V_{OUT}T_{stb}}{\Delta V_{OUT}(R_{FB1} + R_{FB2})}
\]

where \(\Delta V_{OUT}\) is the output voltage increase above the nominal \(V_{OUT}\) at no load.

From Equation 8, it can be seen that a bigger sampling capacitor leads to a smaller \(\Delta V_{OUT}\), but \(C_{FB1}\) can not be too big as it calls for a huge \(C_{OUT}\). A small \(\Delta V_{OUT}\) can cause erratic logic function of the internal PFM comparator in mode transition. Therefore, choose \(\Delta V_{OUT}\) properly according to the highest \(V_{OUT}\) allowed in the applications. When \(\Delta V_{OUT}\) is picked, \(C_{FB1}\) is calculated using Equation 8.

### 7.4 Output Capacitor Selection

The output capacitor does not only need to meet the requirement of output ripple voltage and load transient response, but also needs to ensure the slew rate of the output voltage is slower than the discharging rate of the
sampling capacitor, $C_{FB1}$, in a defined step load transient, as shown in the Figure 33. Therefore, $C_{OUT}$ is first calculated according to $V_{OUT}$ discharging by Equation 9.

\[
C_{OUT} \geq \frac{C_{FB1} \Delta I_{OUT} (R_{FB1} + R_{FB2})}{V_{OUT}} \tag{EQ. 9}
\]

\[
C_{OUT} \geq \frac{\Delta I_{OUT} T}{0.07V_{OUT}} \tag{EQ. 10}
\]

where 7% voltage drop is used in this example.

### 7.5 Dummy Resistor Selection

At no load condition, the system standby power is determined by the IC quiescent current and the feedback resistor bleeding current. If the required standby power is not low, a dummy resistor can be added in parallel with the output capacitor to keep a no-load output voltage from getting too high. Its value is calculated using Equation 11.

\[
R_O = \frac{V_{OUT}}{P_{INSTBY} \eta \left( \frac{V_{OUT}}{I_q V_{FB}} - \frac{V_{FB}}{R_{FB2}} \right)} \text{, where } \eta = 0.4 \tag{EQ. 11}
\]

### 7.6 Power Capability

The maximum power the RAA223012 can deliver depends on the ambient temperature, output voltage, input voltage, and even PCB thermal design. In general, higher input voltage with lower ambient temperature allows a bit more power than low input voltage at higher ambient temperature. Also, it delivers more power at higher output voltage. Table 1 summarizes the maximum power the RAA223012 can deliver with ambient temperature up to 85°C. This table should be used as a reference and may vary because of the actual PCB thermal design.

### 7.7 PCB Layout Guidance

Proper layout is important to ensure a stable operation, good thermal behavior, EMI performance, and reliable operation for various operating environments. Pay attention to the following layout recommendations:

- Leave proper spacing between high voltage (maximum 400V) traces and low voltage traces (minimum 1.4mm)
- Keep a small loop from the input filter capacitor to the IC, switching inductor, output capacitor, and to the ground of the input capacitor, and a small loop consisting of a switching inductor, output capacitor, and free-wheeling diode.
- Keep sufficient copper area on the IC drain and/or source pin (not less than 140mm² for 2W to 3W output power) for better thermal performance
• Keep the switching inductor away from the input EMI inductor to avoid noise coupling, especially when an unshielded switching inductor is used.
• Place the $V_{CC}$ decoupling capacitor and FB pin decoupling capacitor close to the pins.

The PCB layout example is shown in Figure 34.

8. EMI Performance

Conducted and Radiated EMI compliance for EN55022/CISPR22 (5V/150mA output)
Figure 37. Neutral, 120V\textsubscript{AC}

Figure 38. Neutral, 230V\textsubscript{AC}

Figure 39. FCC Part15/CISPR22 Class B Radiated Emissions at 3 Meters, 120V\textsubscript{AC}, 60Hz (Peak Detector)

Figure 40. FCC Part15/CISPR22 Class B Radiated Emissions at 3 Meters, 230V\textsubscript{AC}, 50Hz (Peak Detector)
9. Package Outline Drawings

For the most recent package outline drawing, see P5.064B.

P5.064B
5 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 3, 2/2022

NOTE:
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.
For the most recent package outline drawing, see M8.15.

M8.15
8 Lead Narrow Body Small Outline Plastic Package
Rev 5, 4/2021

NOTES:
1. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.
10. Ordering Information

<table>
<thead>
<tr>
<th>Part Number[1][2]</th>
<th>Part Marking</th>
<th>Package Description (RoHS Compliant)</th>
<th>Pkg. Dwg. #</th>
<th>Carrier Type[3]</th>
<th>Junction Temp Range</th>
</tr>
</thead>
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<tr>
<td>RAA2230124GSP#AA0</td>
<td>223012</td>
<td>8 LD SOIC</td>
<td>M8.15</td>
<td>Tube</td>
<td>-40 to +125°C</td>
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<tr>
<td>RAA2230124GSP#MA0</td>
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<td></td>
<td></td>
<td>Reel, 250</td>
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<tr>
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<td></td>
<td>Reel, 2.5k</td>
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<tr>
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<td>012[4]</td>
<td>5 Ld TSOT23</td>
<td>P5.064B</td>
<td>Reel, 250</td>
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</tr>
<tr>
<td>RAA2230124GP#JA0</td>
<td></td>
<td></td>
<td></td>
<td>Reel, 3k</td>
<td></td>
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<tr>
<td>RTKA223012DR0010BU</td>
<td>Evaluation Board with RAA223012 in 8 LD SOIC package</td>
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<td>RTKA223012DR0020BU</td>
<td>Evaluation Board with RAA223012 in 5 Ld TSOT23 package</td>
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</table>

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

2. For Moisture Sensitivity Level (MSL), see the RAA223012 device page. For more information about MSL, see TB363.

3. See TB347 for details about reel specifications.

4. The part marking is located on the bottom of the part.

Table 2. Key Differences between Family of Parts

<table>
<thead>
<tr>
<th>Device</th>
<th>rDS(ON) (Ω)</th>
<th>IPK (mA)</th>
<th>tOFF_MIN (µs)</th>
<th>Package Options</th>
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<td>520</td>
<td>32</td>
<td>8 Ld SOIC, 5 Ld SOIC, 5 Ld TSOT</td>
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<tr>
<td>RAA223012</td>
<td>14.5</td>
<td>335</td>
<td>19</td>
<td>8 Ld SOIC, 5 Ld TSOT</td>
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<td>RAA223021</td>
<td>4</td>
<td>1100</td>
<td>23</td>
<td>7 Ld SOIC</td>
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</table>

11. Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
</table>
| 3.01  | Mar 3, 2022| Updated POD P5.064B to the latest revision, changes are as follows:  
- Corrected pin numbering to align with datasheet and actual unit.  
- In the End View, widened the lead thickness range to 0.08-0.2mm and removed Note 6. |
| 3.00  | Sep 2, 2021| Changed the Theta JC thermal value for the SOT23-5 package from 80 to 71. |
| 2.00  | Jun 3, 2021| Applied new template.  
Updated File Number to R16DS0139EU0200.  
Changed the SOIC Theta JA from 89 to 86.  
Changed TSOT23 Theta JC from 60 to 80.  
Updated Table 2.  
Updated POD M8.15 to latest revision:  
-Added the coplanarity specification. |
| 1.01  | Feb 25, 2021| Updated Figure 31. |
| 1.00  | Dec 16, 2020| Initial release |
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