The **RAA212422** is a dual output regulator combining a 1.1A synchronous buck regulator with an input range of 3V to 40V with a 1.5A synchronous buck regulator with an input voltage range of 2.7V to 5.5V. Because both high-side and low-side MOSFETs are integrated for both regulators, the RAA212422 provides an easy-to-use, high-efficiency, and low BOM-count solution for a variety of applications.

Both regulators feature internal and external compensation, thermal shutdown, and power-good functions. The wide \( V_{\text{IN}} \) buck regulator features a PFM mode for improved efficiency at light load. This feature can be disabled if forced PWM mode is desired. It switches at a default frequency of 500kHz; however, it can also be programmed using an external resistor from 300kHz to 2MHz. Other features include programmable soft-start and hiccup overcurrent protection.

The low \( V_{\text{IN}} \) buck regulator operates at 1MHz switching frequency, which provides fast load transient response allowing the use of small inductors. Because the high-side MOSFET of the low \( V_{\text{IN}} \) buck regulator is a PMOS, a boot capacitor is not needed, reducing the external component count. They operate at 100% duty cycle and in PWM mode only, reducing noise susceptibility and RF interference.

The RAA212422 is available in a small RoHS compliant 3mmx6mm TDFN plastic package with a full-range industrial temperature of \(-40^\circ\text{C}\) to \(+125^\circ\text{C}\).

**Related Literature**

For a full list of related documents, visit our website:

- [RAA212422 device page](#)

---

**Figure 1. Typical Application**

**Figure 2. Efficiency vs Load, \( V_{\text{OUT1}} = 5V, L_1 = 22\mu\text{H} \)**
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1. Overview

1.1 Typical Application Circuits

![Figure 3. Internal Default Parameter Selection](image-url)
### Table 1. Wide VIN Buck Regulator - External Component Selection

<table>
<thead>
<tr>
<th>VOUT1 (V)</th>
<th>L1 (µH)</th>
<th>COUT1 (µF)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>CFF1 (pF)</th>
<th>RFS (kΩ)</th>
<th>RCOMP1 (kΩ)</th>
<th>CCOMP1 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>33</td>
<td>2 x 22</td>
<td>90.9</td>
<td>4.75</td>
<td>4.7</td>
<td>115</td>
<td>200</td>
<td>470</td>
</tr>
<tr>
<td>5</td>
<td>22</td>
<td>47 + 22</td>
<td>90.9</td>
<td>12.4</td>
<td>22</td>
<td>DNP (Note 1)</td>
<td>130</td>
<td>470</td>
</tr>
<tr>
<td>3.3</td>
<td>22</td>
<td>47 + 22</td>
<td>90.9</td>
<td>20</td>
<td>22</td>
<td>DNP (Note 1)</td>
<td>120</td>
<td>470</td>
</tr>
<tr>
<td>2.5</td>
<td>22</td>
<td>47 + 22</td>
<td>90.9</td>
<td>28.7</td>
<td>22</td>
<td>DNP (Note 1)</td>
<td>110</td>
<td>470</td>
</tr>
<tr>
<td>1.8</td>
<td>10</td>
<td>47 + 22</td>
<td>90.9</td>
<td>45.5</td>
<td>22</td>
<td>DNP (Note 1)</td>
<td>90</td>
<td>470</td>
</tr>
</tbody>
</table>

**Note:**
1. Connect FS1 to VCC1.

### Table 2. Low VIN Buck Regulator - External Component Selection

<table>
<thead>
<tr>
<th>VOUT2 (V)</th>
<th>L1 (µH)</th>
<th>COUT2 (µF)</th>
<th>R3 (kΩ)</th>
<th>R4 (kΩ)</th>
<th>CFF2 (pF)</th>
<th>RCOMP1 (kΩ)</th>
<th>CCOMP1 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>1.5</td>
<td>2x22</td>
<td>33</td>
<td>100</td>
<td>47</td>
<td>40</td>
<td>270</td>
</tr>
<tr>
<td>1.2</td>
<td>2.2</td>
<td>2x22</td>
<td>100</td>
<td>100</td>
<td>22</td>
<td>60</td>
<td>270</td>
</tr>
<tr>
<td>1.8</td>
<td>2.2</td>
<td>2x22</td>
<td>200</td>
<td>100</td>
<td>15</td>
<td>80</td>
<td>330</td>
</tr>
<tr>
<td>2.5</td>
<td>2.2</td>
<td>2x22</td>
<td>316</td>
<td>100</td>
<td>8.2</td>
<td>100</td>
<td>330</td>
</tr>
<tr>
<td>3.3</td>
<td>2.2</td>
<td>2x22</td>
<td>450</td>
<td>100</td>
<td>6.8</td>
<td>120</td>
<td>330</td>
</tr>
</tbody>
</table>
1.2 Block Diagram

Figure 5. Functional Block Diagram
1.3 Ordering Information

<table>
<thead>
<tr>
<th>Part Number (Notes 3, 4)</th>
<th>Part Marking</th>
<th>Temp Range (°C)</th>
<th>Tape and Reel (Units) (Note 2)</th>
<th>Package (RoHS Compliant)</th>
<th>Pkg. Dwg. #</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAA2124224GNP#AA0</td>
<td>RAA212422</td>
<td>-40 to +125</td>
<td>-</td>
<td>22 Ld QFN</td>
<td>L22.3x6</td>
</tr>
<tr>
<td>RAA2124224GNP#HA0</td>
<td>RAA212422</td>
<td>-40 to +125</td>
<td>6k</td>
<td>22 Ld QFN</td>
<td>L22.3x6</td>
</tr>
<tr>
<td>RAA2124224GNP#MA0</td>
<td>RAA212422</td>
<td>-40 to +125</td>
<td>250</td>
<td>22 Ld QFN</td>
<td>L22.3x6</td>
</tr>
</tbody>
</table>

Notes:
2. See TB347 for details about reel specifications
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the RAA212422 device page. For more information about MSL, see TB363.

1.4 Pin Configurations

![22 Ld 3x6 TQFN Top View](image)

1.5 Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN2</td>
<td>Input supply for the power stage of the low ( V_{IN} ) PWM regulator and the source for the internal linear regulator that provides bias for the low ( V_{IN} ) buck regulator. Place a minimum of 10µF ceramic capacitance from VIN2 to GND and as close as possible to the IC for decoupling. The input voltage range is 2.7V to 5.5V.</td>
</tr>
<tr>
<td>2</td>
<td>EN2</td>
<td>Device enable input for the low ( V_{IN} ) buck regulator. When the input voltage on this pin rises above 1.4V, the device is enabled. The device is disabled when the pin is pulled to ground. A 100Ω resistor discharges the output through the LX2 pin when the device is disabled. See Figure 5 on page 5 for details.</td>
</tr>
<tr>
<td>3</td>
<td>VIN3</td>
<td>Connect VIN3 to VIN2.</td>
</tr>
<tr>
<td>4</td>
<td>PG2</td>
<td>Power-good output of the low ( V_{IN} ) buck regulator. PG2 is pulled to ground during the soft-start interval and when the output voltage is below regulation limits. An internal 5MΩ pull-up resistor is on this pin.</td>
</tr>
<tr>
<td>5</td>
<td>SS1</td>
<td>Controls the soft-start ramp time for the output of the wide ( V_{IN} ) buck regulator. A single capacitor from the SS1 pin to ground determines the output ramp rate. See &quot;Soft-Start (Wide ( V_{IN} ) and Low ( V_{IN} ) Buck)&quot; on page 21 for soft-start details. If the SS1 pin is tied to VCC1, an internal soft-start of 2ms is used.</td>
</tr>
</tbody>
</table>
**RAA212422 1. Overview**

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>SYNC1</td>
<td>Synchronization and light load operational mode selection input. Connect to logic high or VCC for PWM mode. Connect to logic low or ground for PFM mode. Logic ground enables the IC to automatically choose PFM or PWM operation. Connect to an external clock source for synchronization with positive edge trigger. Sync source must be higher than the programmed IC frequency. There is an internal 5MΩ pull-down resistor to prevent an undefined logic state if SYNC is left floating.</td>
</tr>
<tr>
<td>7</td>
<td>BOOT1</td>
<td>Floating bootstrap supply pin for the power MOSFET gate driver for the wide VIN buck regulator. The bootstrap capacitor provides the necessary charge to turn on the internal N-channel MOSFET. Connect an external 100nF capacitor from this pin to LX1.</td>
</tr>
<tr>
<td>8</td>
<td>VIN1</td>
<td>The input supply for the power stage of the wide VIN buck regulator and the source for the internal linear bias regulator. Place a minimum of 4.7µF ceramic capacitance from VIN1 to GND1 and close to the IC for decoupling. The input voltage range is 3V to 40V.</td>
</tr>
<tr>
<td>9</td>
<td>LX1</td>
<td>Switch node output. It connects the switching FETs with the external output inductor.</td>
</tr>
<tr>
<td>10</td>
<td>GND1</td>
<td>Power ground connection. Connect directly to the system GND plane.</td>
</tr>
<tr>
<td>11</td>
<td>NC1</td>
<td>No connect</td>
</tr>
<tr>
<td>12</td>
<td>NC2</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>EN1</td>
<td>Wide VIN buck regulator enable input. The regulator and bias LDO are held off when the pin is pulled to ground. When the voltage on this pin rises above 1V, the chip is enabled. Connect this pin to VIN1 for automatic start-up. Do not connect the EN1 pin to VCC1 because the LDO is controlled by EN1 voltage.</td>
</tr>
<tr>
<td>14</td>
<td>PG1</td>
<td>Open-drain, power-good output that is pulled to ground when the output voltage of the wide VIN buck regulator is below regulation limits or during the soft-start interval. An internal 5MΩ pull-up resistor is on this pin.</td>
</tr>
<tr>
<td>15</td>
<td>VCC1</td>
<td>Output of the wide VIN buck regulator’s internal 5V linear bias regulator. Decouple to GND with a 1µF ceramic capacitor at the pin.</td>
</tr>
<tr>
<td>16</td>
<td>FB1</td>
<td>Feedback pin for the wide VIN buck regulator. FB1 is the inverting input to the voltage loop error amplifier. COMP1 is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB1. In addition, the PWM regulator’s power-good and UVLO circuits use FB1 to monitor the regulator output voltage.</td>
</tr>
<tr>
<td>17</td>
<td>COMP1</td>
<td>Error amplifier output. When this pin is tied to VCC1, internal compensation is used. When only an RC network is connected from COMP1 to GND1, external compensation is used. See &quot;Loop Compensation Design&quot; on page 28 for more details.</td>
</tr>
<tr>
<td>18</td>
<td>FS1</td>
<td>Frequency selection pin for the wide VIN buck regulator. Tie to VCC1 for 500kHz switching frequency. Connect a resistor to GND1 for adjustable frequency from 300kHz to 2MHz.</td>
</tr>
<tr>
<td>19</td>
<td>COMP2</td>
<td>Low VIN buck regulator error amplifier. When COMP2 is tied high to VIN2, internal compensation is used. When COMP2 is connected with a series resistor and capacitor to GND, external compensation is used. See &quot;Loop Compensation Design&quot; on page 28 for more details.</td>
</tr>
<tr>
<td>20</td>
<td>FB2</td>
<td>Feedback pin for the low VIN buck regulator. FB2 is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB2. In addition, the power-good PWM regulator’s power-good and undervoltage protection circuits use FB2 to monitor the output voltage.</td>
</tr>
<tr>
<td>21</td>
<td>GND2</td>
<td>Power ground for low VIN buck regulator. Connect directly to the system ground plane.</td>
</tr>
<tr>
<td>22</td>
<td>LX2</td>
<td>Power stage switching node for output voltage regulation of the low VIN buck regulator. Connect to the output inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See Figure 5 on page 5 for details.</td>
</tr>
<tr>
<td></td>
<td>EPAD</td>
<td>Ground connection. Connect to the application board GND plane with at least five vias. All voltage levels are measured with respect to this pin. The EPAD MUST NOT float.</td>
</tr>
</tbody>
</table>
2. Specifications

2.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN1 to GND</td>
<td>-0.3</td>
<td>+43</td>
<td>V</td>
</tr>
<tr>
<td>LX1 to GND (DC)</td>
<td>-0.3</td>
<td>V_{IN1} + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>LX1 to GND (20ns)</td>
<td>-2.0</td>
<td>+44</td>
<td>V</td>
</tr>
<tr>
<td>EN1 to GND</td>
<td>-0.3</td>
<td>+43</td>
<td>V</td>
</tr>
<tr>
<td>BOOT1 to LX1</td>
<td>-0.3</td>
<td>+5.5</td>
<td>V</td>
</tr>
<tr>
<td>COMP1, FS1, PG1, SYNC1, SS1, VCC1 to GND</td>
<td>-0.3</td>
<td>+5.9</td>
<td>V</td>
</tr>
<tr>
<td>FB1 to GND</td>
<td>-0.3</td>
<td>+2.95</td>
<td>V</td>
</tr>
<tr>
<td>VIN2 to GND (DC)</td>
<td>-0.3</td>
<td>+6</td>
<td>V</td>
</tr>
<tr>
<td>VIN2 to GND (20ms)</td>
<td>-0.3</td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td>LX2 to GND (DC)</td>
<td>-0.3</td>
<td>+6</td>
<td>V</td>
</tr>
<tr>
<td>LX2 to GND (100ns)</td>
<td>-1.5</td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td>EN2, COMP2, PG2, MODE2</td>
<td>-0.3</td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td>FB2</td>
<td>-0.3</td>
<td>+2.7</td>
<td>V</td>
</tr>
</tbody>
</table>

**ESD Rating**

<table>
<thead>
<tr>
<th>Rating</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human Body Model (Tested per JS-001-2017)</td>
<td>2</td>
<td>kV</td>
</tr>
<tr>
<td>Charged Device Model (Tested per JS-002-2014)</td>
<td>1</td>
<td>kV</td>
</tr>
<tr>
<td>Latch-Up (Tested per JESD78E; Class 2, Level A)</td>
<td>100</td>
<td>mA</td>
</tr>
</tbody>
</table>

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Resistance (Typical)</th>
<th>$\theta_JA$ (°C/W)</th>
<th>$\theta_JC$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22 Ld 3x6 QFN Package (Notes 5, 6)</td>
<td>31.3</td>
<td>2.3</td>
</tr>
</tbody>
</table>

Notes:

5. $\theta_JA$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.

6. For $\theta_JC$, the "case temp" location is the center of the exposed metal pad on the package underside.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Junction Temperature</td>
<td></td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum Storage Temperature Range</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Ambient Temperature Range</td>
<td>-40</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>Pb-Free Reflow Profile</td>
<td></td>
<td>Refer to TB493</td>
<td></td>
</tr>
</tbody>
</table>
### 2.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{\text{IN1}}$</td>
<td>3</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage, $V_{\text{IN2}}$</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>-40</td>
<td>+125</td>
<td>°C</td>
</tr>
</tbody>
</table>

### 2.4 Electrical Specifications

$V_{\text{IN1}}$ = 3V to 40V, unless otherwise noted. Typical values are at $T_A = +25^\circ$C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min (Note 9)</th>
<th>Typ</th>
<th>Max (Note 9)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Wide VIN Buck Regulator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>$V_{\text{IN1}}$</td>
<td>Voltage Range</td>
<td>3</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IN1}}$ Quiescent Supply Current</td>
<td>$I_Q1$</td>
<td>$V_{FB1} = 0.7V, \text{SYNC1} = V_{CC1}$</td>
<td>8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IN1}}$ Shutdown Supply Current</td>
<td>$I_{SD1}$</td>
<td>EN1 = 0V, $V_{\text{IN1}} = 40V$ (Note 7)</td>
<td>2</td>
<td>6</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$V_{CC1}$ Voltage</td>
<td>$V_{CC1}$</td>
<td>$V_{\text{IN1}} = 6V, I_{OUT} = 0$ to 10mA</td>
<td>4.5</td>
<td>5.1</td>
<td>5.7</td>
<td>V</td>
</tr>
<tr>
<td><strong>Power-On Reset</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC1}$ POR Threshold</td>
<td></td>
<td>Rising edge</td>
<td>2.75</td>
<td>2.95</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling edge</td>
<td>2.35</td>
<td>2.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>Oscillator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal Switching Frequency</td>
<td>$f_{SW1}$</td>
<td>$FS1$ pin = $V_{CC1}$</td>
<td>430</td>
<td>500</td>
<td>570</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Resistor from the FS1 pin to GND = 340kΩ</td>
<td>240</td>
<td>300</td>
<td>360</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Resistor from the FS1 pin to GND = 32.4kΩ</td>
<td>2000</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>$t_{\text{MIN_OFF}}$</td>
<td>$V_{\text{IN1}} = 3V$</td>
<td>150</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>$t_{\text{MIN_ON}}$ (Note 10)</td>
<td>$V_{\text{IN1}} = 3V$</td>
<td>90</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>FS1 Voltage</td>
<td>$V_{FS1}$</td>
<td>$R_{FS1} = 100kΩ$</td>
<td>0.39</td>
<td>0.4</td>
<td>0.41</td>
<td>V</td>
</tr>
<tr>
<td>Synchronization Frequency</td>
<td>SYNC1</td>
<td></td>
<td>300</td>
<td>2000</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>SYNC1 Pulse-Width</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td><strong>Error Amplifier</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error Amplifier Transconductance Gain</td>
<td>$g_m1$</td>
<td>External compensation</td>
<td>165</td>
<td>230</td>
<td>295</td>
<td>µA/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal compensation</td>
<td>50</td>
<td></td>
<td>µA/V</td>
<td></td>
</tr>
<tr>
<td>FB1 Leakage Current</td>
<td>$V_{FB1} = 0.6V$</td>
<td></td>
<td>1</td>
<td>150</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Current Sense Amplifier Gain</td>
<td>$R_{T1}$</td>
<td></td>
<td>0.44</td>
<td>0.5</td>
<td>0.55</td>
<td>V/A</td>
</tr>
<tr>
<td>FB1 Voltage</td>
<td>$T_A = -40^\circ$ to $+125^\circ$</td>
<td></td>
<td>0.590</td>
<td>0.599</td>
<td>0.607</td>
<td>V</td>
</tr>
<tr>
<td><strong>Power-Good</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lower PG1 Threshold - VFB1 Rising</td>
<td></td>
<td></td>
<td>90</td>
<td>94</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Lower PG1 Threshold - VFB1 Falling</td>
<td></td>
<td></td>
<td>82.5</td>
<td>86</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Upper PG1 Threshold - VFB1 Rising</td>
<td></td>
<td></td>
<td>116.5</td>
<td>120</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Upper PG1 Threshold - VFB1 Falling</td>
<td></td>
<td></td>
<td>107</td>
<td>112</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>PG1 Propagation Delay</td>
<td></td>
<td>Percentage of the soft-start time</td>
<td>10</td>
<td></td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>
### 2. Specifications

V\textsubscript{IN1} = 3V to 40V, unless otherwise noted. Typical values are at T\textsubscript{A} = +25°C. (Continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min (Note 9)</th>
<th>Typ</th>
<th>Max (Note 9)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG1 Low Voltage</td>
<td>I\textsubscript{SINK}</td>
<td>EN1 = V\textsubscript{CC}, VFB1 = 0V</td>
<td>0.05</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

#### Tracking and Soft-Start (SS1)

- Soft-Start Charging Current: I\textsubscript{SS1} = 4.2 5.5 6.7 µA
- Internal Soft-Start Ramp Time: EN1/SS1 = V\textsubscript{CC1} = 1.5 2.4 3.4 ms

#### Fault Protection

- Thermal Shutdown Temperature: T\textsubscript{SD} = Rising threshold 150 °C
- Current Limit Blanking Time: T\textsubscript{HYG} = Hysteresis 25 °C
- Overcurrent and Auto Restart Period: t\textsubscript{OCOFF} = 17 Clock pulses
- Positive Peak Current Limit: I\textsubscript{PLIMIT} (Note 8) = 1.3 1.6 1.8 A
- PFM Peak Current Limit: I\textsubscript{PK,PFM} (Note 8) = 0.34 0.4 0.5 A
- Zero Cross Threshold: 15 mA
- Power MOSFET

- High-Side: R\textsubscript{HDS} = I\textsubscript{LX1} = 100mA, V\textsubscript{CC} = 5V = 312 mΩ
- Low-Side: R\textsubscript{LDS} = I\textsubscript{LX1} = 100mA, V\textsubscript{CC} = 5V = 173.8 mΩ
- PHASE Leakage Current: EN1 = LX1 = 0V = 300 nA
- PHASE Rise Time: t\textsubscript{RISE} = VIN1 = 40V = 10 ns

#### EN1/SYNC1

- Input Threshold: Falling edge, logic low = 0.4 1 V
- Rising edge, logic high = 1.2 1.4 V
- EN1 Logic Input Leakage Current: EN1 = 0V/40V = -0.65 0.65 µA
- SYNC1 Logic Input Leakage Current: SYNC1 = 0V = 10 100 nA
- SYNC1 = 5V = 1.0 1.55 µA

#### Low VIN Buck Regulator

- Input Supply

- V\textsubscript{IN2} Undervoltage Lockout Threshold: V\textsubscript{UVLO2} = Rising, no load = 2.5 2.7 V
- Failing, no load = 2.2 2.4 V
- Quiescent Supply Current: I\textsubscript{VIN2} = f\textsubscript{SW} = 1MHz, no load at the output = 7 15 mA
- Shut Down Supply Current: I\textsubscript{SD2} = VIN2 = 5.5V, EN2 = low = 5 10 µA

#### Output Regulation

- Feedback Voltage: V\textsubscript{FB2} = T\textsubscript{J} = +25°C = 0.595 0.600 0.605 V
- T\textsubscript{J} = -40°C to +125°C = 0.582 0.605 V
- V\textsubscript{FB2} Bias Current: I\textsubscript{VFB2} = V\textsubscript{FB2} = 2.7V, T\textsubscript{J} = -40°C to +125°C = -120 50 350 nA
- Line Regulation: V\textsubscript{IN2} = V\textsubscript{O} = 0.5V to 5.5V (minimal 2.7V) = -0.2 -0.05 0.1 %/V
- Load Regulation: See Note 11 \(< -0.2\) %/A
- Soft-Start Ramp Time Cycle: See Note 11 1 ms
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min (Note 9)</th>
<th>Typ</th>
<th>Max (Note 9)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Protections</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Peak Current Limit</td>
<td>I_PLIMIT</td>
<td>1.5A application</td>
<td>2.1</td>
<td>2.5</td>
<td>2.9</td>
<td>A</td>
</tr>
<tr>
<td>Zero Cross Threshold</td>
<td></td>
<td></td>
<td>-170</td>
<td>-70</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>Negative Current Limit</td>
<td>I_NLIMIT</td>
<td></td>
<td>-2.3</td>
<td>-1.75</td>
<td>-1</td>
<td>A</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td></td>
<td>Temperature rising</td>
<td>150</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td></td>
<td>Temperature falling</td>
<td>25</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compensation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error Amplifier Transconductance</td>
<td>COMP2</td>
<td>tied VIN2</td>
<td>40</td>
<td></td>
<td></td>
<td>µA/V</td>
</tr>
<tr>
<td>Transresistance</td>
<td>RT</td>
<td></td>
<td>0.24</td>
<td>0.3</td>
<td>0.40</td>
<td>Ω</td>
</tr>
<tr>
<td>Power MOSFETs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P-Channel MOSFET ON-Resistance</td>
<td>V_IN2 = 5V, I_O2 = 200mA</td>
<td></td>
<td>117</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>N-Channel MOSFET ON-Resistance</td>
<td>V_IN2 = 5V, I_O2 = 200mA</td>
<td></td>
<td>86</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>LX2 Maximum Duty Cycle</td>
<td></td>
<td></td>
<td>100</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LX2 Minimum On-Time</td>
<td>(Note 10)</td>
<td></td>
<td>60</td>
<td>85</td>
<td>85</td>
<td>ns</td>
</tr>
<tr>
<td>Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal Switching Frequency</td>
<td>f_SW2</td>
<td></td>
<td>850</td>
<td>1000</td>
<td>1150</td>
<td>kHz</td>
</tr>
<tr>
<td>Power-Good</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td></td>
<td>1mA sinking current</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Delay Time (Rising Edge)</td>
<td></td>
<td></td>
<td>0.5</td>
<td>1</td>
<td>2</td>
<td>ms</td>
</tr>
<tr>
<td>PGOOD Delay Time (Falling Edge)</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>PG2 Pin Leakage Current</td>
<td>PG2 = V_IN2</td>
<td></td>
<td>0.01</td>
<td>0.1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>OVP PG2 Rising Threshold</td>
<td></td>
<td></td>
<td>110</td>
<td>119</td>
<td>122</td>
<td>%</td>
</tr>
<tr>
<td>OVP PG2 Hysteresis</td>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>UVP PG2 Rising Threshold</td>
<td></td>
<td></td>
<td>80</td>
<td>85</td>
<td>90</td>
<td>%</td>
</tr>
<tr>
<td>UVP PG2 Hysteresis</td>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Enable Logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Input Low</td>
<td></td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Input High</td>
<td></td>
<td></td>
<td>1.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Leakage Current</td>
<td>I_MODE2</td>
<td>Pulled up to 5.5V</td>
<td>5.5</td>
<td>8</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

Notes:
7. Test conditions: V_IN1 = 40V, FB1 forced above regulation point (0.6V), switching and power MOSFET gate charging current not included.
8. Established by both current sense amplifier gain test and current sense amplifier output test at I_L = 0A.
9. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Minimum On-Time required to maintain loop stability.
11. Not tested in production. Characterized using evaluation board. See load regulation diagrams (Figures 16 through 19). +105°C T_A represents near worst case operating point.
3. Typical Performance Curves

3.1 Efficiency Curves

Wide VIN Buck f_{SW} = 500kHz, T_{A} = +25°C

Figure 6. Efficiency vs Load, PFM, V_{OUT1} = 5V, L_{1} = 22µH,

Figure 7. Efficiency vs Load, PWM, V_{OUT1} = 5V, L_{1} = 22µH,

Figure 8. Efficiency vs Load, PFM, V_{OUT1} = 3.3V, L_{1} = 22µH

Figure 9. Efficiency vs Load, PWM, V_{OUT1} = 3.3V, L_{1} = 22µH

Figure 10. V_{OUT} Regulation vs Load, PFM, V_{OUT1} = 5V

Figure 11. V_{OUT} Regulation vs Load, PWM, V_{OUT1} = 5V
3. Typical Performance Curves

Wide VIN Buck $f_{SW} = 500\text{kHz}$, $T_A = +25^\circ\text{C}$ (Continued)

Figure 12. $V_{OUT}$ Regulation vs Load, PFM, $V_{OUT1} = 3.3\text{V}$

Figure 13. $V_{OUT}$ Regulation vs Load, PWM, $V_{OUT1} = 3.3\text{V}$

Low VIN Buck $f_{SW} = 1\text{MHz}$, $T_A = +25^\circ\text{C}$

Figure 14. Efficiency vs Load, $V_{IN2} = 5\text{V}$

Figure 15. Efficiency vs Load, $V_{IN2} = 3.3\text{V}$

Figure 16. $V_{OUT}$ Regulation vs Load, $V_{OUT2} = 1.2\text{V}$

Figure 17. $V_{OUT}$ Regulation vs Load, $V_{OUT2} = 1.8\text{V}$,
3. Typical Performance Curves

Low $V_{IN}$ Buck $f_{SW} = 1$MHz, $T_A = +25^\circ$C (Continued)

Figure 18. $V_{OUT}$ Regulation vs Load, $V_{OUT2} = 2.5$V

Figure 19. $V_{OUT}$ Regulation vs Load, $V_{OUT2} = 3.3$V
### 3.2 Measurements

Wide VIN Buck Measurements \( f_{SW} = 500\text{kHz}, V_{IN1} = 24\text{V}, V_{OUT1} = 5\text{V}, T_A = +25^\circ\text{C} \)

- Figure 20. Start-Up at No Load, \( V_{OUT1} = 3.3\text{V}, \text{PFM} \)
- Figure 21. Start-Up at No Load, \( \text{PWM} \)
- Figure 22. Shutdown at No Load, \( V_{OUT1} = 3.3\text{V}, \text{PFM} \)
- Figure 23. Shutdown at No Load, \( \text{PWM} \)
- Figure 24. Start-Up at 1.1A, \( \text{PWM} \)
- Figure 25. Shutdown at 1.1A, \( \text{PWM} \)
3. Typical Performance Curves

Wide $V_{IN}$ Buck Measurements $f_{SW} = 500\text{kHz}, V_{IN1} = 24\text{V}, V_{OUT1} = 5\text{V}, T_A = +25^\circ\text{C}$ (Continued)

Figure 26. Steady State at No Load, PFM

Figure 27. Steady State at No Load, PWM

Figure 28. Light Load Operation at 20mA, PFM

Figure 29. Light Load Operation at 20mA, PWM

Figure 30. Steady State at 1.1A Load

Figure 31. Load Transient, PFM
Wide $V_{IN}$ Buck Measurements $f_{SW} = 500$kHz, $V_{IN1} = 24$V, $V_{OUT1} = 5$V, $T_A = +25^\circ$C (Continued)

**Figure 32. Load Transient, PWM**

**Figure 33. Overcurrent Protection**

**Figure 34. Overcurrent Protection Hiccup**

**Figure 35. Sync at 550kHz, 1.1A Load**

**Figure 36. Negative Current Limit**

**Figure 37. Negative Current Limit Recovery**
Low $V_{\text{IN}}$ Buck Measurements Unless otherwise noted: $V_{\text{IN2}} = 5\, \text{V}, V_{\text{OUT2}} = 1.2\, \text{V}, C_{\text{IN2}} = C_{\text{OUT2}} = 2 \times 22\, \mu\text{F}, T_J = +25^\circ\text{C}, I_{\text{LOAD}} = 0\, \text{A}$

Figure 38. Start-Up by Enable at No Load, $V_{\text{IN2}} = 5\, \text{V}, T_A = +25^\circ\text{C}$

Figure 39. Shutdown by Enable at No Load, $V_{\text{IN2}} = 5\, \text{V}, T_A = +25^\circ\text{C}$

Figure 40. Start-Up by Enable at 1.5A Load, $V_{\text{IN2}} = 5\, \text{V}, T_A = +25^\circ\text{C}$

Figure 41. Shutdown by Enable at 1.5A Load, $V_{\text{IN2}} = 5\, \text{V}, T_A = +25^\circ\text{C}$

Figure 42. Start-Up by $V_{\text{IN2}}$ at No Load, $V_{\text{IN2}} = 5\, \text{V}, T_A = +25^\circ\text{C}$
3. Typical Performance Curves

Low \( V_{\text{IN}} \) Buck Measurements

Unless otherwise noted: \( V_{\text{IN2}} = 5V, V_{\text{OUT2}} = 1.2V, C_{\text{IN2}} = C_{\text{OUT2}} = 2 \times 22\mu F, T_J = +25^\circ C, I_{\text{LOAD}} = 0A \)

- Figure 43. Start-Up by \( V_{\text{IN2}} \) at 1.5A Load, \( V_{\text{IN2}} = 5V \), \( T_A = +25^\circ C \)
- Figure 44. Shutdown by \( V_{\text{IN2}} \) at No Load, \( V_{\text{IN2}} = 5V \), \( T_A = +25^\circ C \)
- Figure 45. Shutdown by \( V_{\text{IN2}} \) at 1.5A Load, \( V_{\text{IN2}} = 5V \), \( T_A = +25^\circ C \)
- Figure 46. Steady State at No Load, \( V_{\text{IN2}} = 5V \), \( T_A = +25^\circ C \)
- Figure 47. Load Transient, \( V_{\text{IN2}} = 5V \), \( T_A = +25^\circ C \)
- Figure 48. Output Short-Circuit, \( V_{\text{IN2}} = 5V \), \( T_A = +25^\circ C \)
3. Typical Performance Curves

Low $V_{IN}$ Buck Measurements Unless otherwise noted: $V_{IN2} = 5V$, $V_{OUT2} = 1.2V$, $C_{IN2} = C_{OUT2} = 2x22\mu F$, $T_J = +25^\circ C$, $I_{LOAD} = 0A$

Figure 49. Overcurrent Protection, $V_{IN2} = 5V$, $T_A = +25^\circ C$

Figure 50. Overvoltage Protection, $V_{IN2} = 5V$, $T_A = +25^\circ C$

Figure 51. Over-Temperature Protection, $V_{IN2} = 5V$, $T_A = +160^\circ C$
4. Detailed Description

The RAA212422 consists of a constant frequency current mode wide $V_{IN}$ buck regulator and a low $V_{IN}$ buck regulator. The wide $V_{IN}$ buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +3V to +40V. An internal linear regulator provides bias to the low voltage portions of the wide $V_{IN}$ buck regulator. Peak current mode control simplifies feedback loop compensation and rejects input voltage variation. User-selectable internal feedback loop compensation further simplifies design. The buck regulator is equipped with an internal current sensing circuit and the peak current limit threshold is typically set at 1.6A.

The low $V_{IN}$ switching regulator operates at 1MHz switching frequency, which enables the use of smaller inductors resulting in small form factor while also providing excellent efficiency. The supply current is typically only 2µA when the regulator is shut down.

4.1 Power-On Reset /UVLO

The wide $V_{IN}$ buck regulator automatically initializes after receiving the input power supply and continually monitors the EN1 pin state. If EN1 is held below its logic rising threshold, the IC is held in shutdown and consumes typically 2µA from the VIN1 supply. If EN1 exceeds its logic rising threshold, the regulator enables the bias linear regulator and begins to monitor the VCC1 pin voltage. When the VCC1 pin voltage passes its rising POR threshold, the controller initializes the switching regulator circuits. If $V_{CC1}$ never passes the rising POR threshold, the controller does not allow the switching regulator to operate. If $V_{CC1}$ falls below its falling POR threshold while the switching regulator is operating, the switching regulator shuts down until $V_{CC1}$ returns.

When the low $V_{IN}$ buck regulator’s input voltage rises above a typical value of 2.5V, the regulator is allowed to turn on. When the input voltage falls below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.

4.2 Soft-Start (Wide $V_{IN}$ and Low $V_{IN}$ Buck)

Both the wide $V_{IN}$ and low $V_{IN}$ buck converters feature soft-start to avoid large inrush current. For the buck converters, $V_{OUT1}$ ($V_{OUT2}$) is slowly increased at start-up to its final regulated value.

For the wide $V_{IN}$ buck regulator, soft-start time is determined by the SS1 pin connection. If SS1 is pulled to VCC1, an internal 2ms timer is selected for soft-start. For other soft-start times, connect a capacitor from SS1 to GND. In this case, a 5.5µA current pulls up the SS1 voltage and the FB1 pin follows this ramp until it reaches the 600mV reference level. The wide $V_{IN}$ buck regulator soft-start time is described by Equation 1:

\[
\text{Time (ms)} = C(nF) \times 0.109
\]

For the low $V_{IN}$ buck regulator, when the VIN2 pin exceeds its rising POR trip point (nominal 2.5V), the device begins operation. If the EN2 pin is held low externally, nothing happens until this pin is released. When EN2 is released and is above the logic threshold, the internal default soft-start time is 1ms. The typical soft-start time for the low $V_{IN}$ buck regulator is 1ms.

4.3 Power-Good

PG1 is the open-drain output of a window comparator that continuously monitors the wide $V_{IN}$ buck regulator output voltage using the FB1 pin. PG1 is actively held low when EN1 is low and during the buck regulator soft-start period. After the soft-start period completes, PG1 becomes high impedance if the FB1 pin is within the range specified in the “Electrical Specifications” on page 9. If FB1 exits the specified window, PG1 is pulled low until FB1 returns. Over-temperature faults also force PG1 low until the fault condition is cleared by an attempt to soft-start. An internal 5MΩ pull-up resistor is on the PG1 pin.

The window comparator output, PG2, continuously monitors the low $V_{IN}$ buck regulator output voltage. PG2 is actively held low when EN2 is low and during the buck regulator soft-start period. After 1ms delay of the soft-start period, PG2 becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB2. When VFB2 drops 15% below or raises 15% above the nominal regulation voltage, the device pulls PG2 low. Any fault condition forces PG2 low until the fault condition is cleared by attempts to soft-start. An internal
5MΩ pull-up resistor is on the PG2 pin. You can add an external resistor from PG2 to VIN2 for more pull-up strength.

4.4 PWM Control Scheme (Wide VIN and Low VIN Buck)

Both the wide VIN and low VIN buck regulators employ peak current-mode Pulse-Width Modulation (PWM) control for fast transient response and pulse-by-pulse current limiting, as shown in Figure 5 on page 5. The current loop consists of the current-sensing circuit, slope compensation ramp, PWM comparator, oscillator, and latch. The current sense gain for the wide VIN buck regulator is typically 500mV/A and the slope compensation rate, Se1, is typically 450mV/T, where T is the switching cycle period. The current sense gain for the low VIN buck regulator is typically 300mV/A and the slope compensation rate, Se2, is typically 900mV/µs. The control reference for the current loop comes from the error amplifier’s output (VCOMP1 for wide VIN and VCOMP2 for low VIN buck regulator).

A PWM cycle begins when a clock pulse sets the PWM latch and the upper FET turns on. The current begins to ramp up in the upper FET and inductor. This current is sensed, converted to a voltage (VCSA), and summed with the slope compensation signal. This combined signal is compared to VCOMP1 (VCOMP2) and the latch is reset when the signal is equal to VCOMP1 (VCOMP2). Upon latch reset the upper FET turns off and the lower FET turns on, allowing current to ramp down in the inductor. The lower FET remains on until the clock initiates another PWM cycle. Figure 52 shows the typical operating waveforms during PWM operation. The dotted lines illustrate the sum of the current sense and slope compensation signal.

![Figure 52. PWM Operation Waveforms](image)

The output voltage is regulated as the error amplifier varies VCOMP1 (VCOMP2) and thus varies the output inductor current. The error amplifier is a transconductance type and its output (COMP1 or COMP2) is terminated with a series RC network to GND. This termination is internal (150kΩ/54pF) if the COMP1 pin is tied to VCC1 for the wide VIN buck. For the low VIN buck, the termination is a 200kΩ and 27pF series R-C network. In addition, the transconductance for COMP1 = VCC1 is 50µA/V vs 230µA/V for external R-C connection. Its non-inverting input is internally connected to a 600mV reference voltage and its inverting input is connected to the output voltage using the FB1 pin and its associated divider network. The maximum error amplifier voltage of the low VIN buck (COMP2) is clamped to 1.6V.

4.5 Light Load Operation

At light loads, converter efficiency can be improved by enabling Pulsed Frequency Modulation (PFM). Connecting the SYNC1 pin to GND allows the controller to choose PFM operation automatically when the load current is low. Figure 53 on page 23 shows the DCM operation. The IC enters the DCM mode of operation when eight consecutive cycles of inductor current crossing zero are detected. This corresponds to a load current equal to 1/2 the peak-to-peak inductor ripple current and set by Equation 2:

\[
I_{OUT} = \frac{V_{OUT}(1-D)}{2L_{SW}}
\]
where $D = \text{duty cycle}$, $f_{SW} = \text{switching frequency}$, $L = \text{inductor value}$, $I_{OUT} = \text{output loading current}$, and $V_{OUT} = \text{output voltage}$.

While operating in PFM mode, the regulator controls the output voltage with a simple comparator and pulsed FET current. A comparator signals the point where FB equals the 600mV reference, and the regulator begins providing pulses of current until FB moves above the 600mV reference by 1%. The current pulses are approximately 400mA and are issued at a frequency equal to the converter's programmed PWM operating frequency.

Due to the pulsed current nature of PFM mode, the converter can supply limited current to the load. If the load current rises beyond the limit, $V_{OUT}$ begins to decline. A second comparator signals an FB voltage 2% lower than the 600mV reference and forces the converter to return to PWM operation.

4.6 Output Voltage Selection

The regulator output voltage is easily programmed using an external resistor divider to scale $V_{OUT1}$ relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier; refer to Figure 54 for more information.

The output voltage programming resistor, $R_2$, depends on the value chosen for the feedback resistor, $R_1$, and the needed output voltage, $V_{OUT1}$, of the regulator. Equation 3 describes the relationship between $V_{OUT1}$ and the resistor values.

\[
R_2 = \frac{R_1 \cdot 0.6V}{V_{OUT1} - 0.6V}
\]

If the output voltage is 0.6V, $R_2$ is left unpopulated and $R_1$ is 0Ω.
Similarly, the output voltage of the low VIN buck can be set by an external resistor divider network. Calculate the values of resistors $R_3$ and $R_4$ using Equation 4.

\[
R_4 = \frac{R_3 \cdot 0.6V}{V_{OUT2} - 0.6V}
\]  

(EQ. 4)

If the target output voltage is 0.6V, $R_4$ is left unpopulated and $R_3$ is shorted. There is a leakage current from VIN2 to LX2. Renesas recommends preloading the output with 10µA minimum. For better performance, add a feedforward capacitor in parallel with $R_1$. Check loop analysis before use in an application.

4.7 Protection Features

The RAA212422 is protected from overcurrent, negative overcurrent, over-temperature, and boot undervoltage. The protection circuits operate automatically.

4.7.1 Overcurrent Protection

During PWM on-time of the wide VIN buck regulator, current through the upper FET is monitored and compared to a nominal 1.6A peak overcurrent limit. If the current reaches the limit, the upper FET turns off until the next switching cycle. In this way, FET peak current is always well limited.

If the overcurrent condition persists for typically 17 sequential clock cycles, the regulator begins its hiccup sequence. In this case, both FETs turn off and PG1 is pulled low. This condition is maintained for eight soft-start periods, after which the regulator attempts a normal soft-start.

If the output fault persists, the regulator repeats the hiccup sequence indefinitely. Output faults are not dangerous even if the output is shorted during soft-start.

If $V_{OUT1}$ is shorted very quickly, FB1 may collapse below 5/8 of its target value before the typical 17 cycles of overcurrent are detected. The RAA212422 recognizes this condition and begins to lower its switching frequency proportional to the FB1 pin voltage. This ensures that the current never runs away (even with $V_{OUT1}$ near 0V).

The low VIN buck regulator is protected from overcurrent by monitoring the CSA output with the OCP comparator, as shown in the Figure 5 on page 5. The current-sensing circuit has a gain of 300mV/A from the P-FET current to the CSA output. When the CSA output reaches a threshold, the OCP comparator is tripped to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET immediately turns off and does not turn on again until the next switching cycle. If the overcurrent condition stops, the output resumes back into regulation point.

4.7.2 Short-Circuit Protection (Low VIN Buck)

The low VIN buck regulator Short-Circuit Protection (SCP) comparator monitors the VFB2 pin voltage for output short-circuit faults. When the VFB2 voltage is lower than 0.3V, the SCP comparator forces the PWM oscillator frequency to drop below the normal operation value. This comparator is effective during startup or an output short-circuit event.

4.7.3 Negative Current Limit

For the wide VIN buck regulator, if an external source drives current into $V_{OUT1}$, the controller attempts to regulate $V_{OUT1}$ by reversing its inductor current to absorb the externally sourced current. If the external source is low impedance, the current may be reversed to unacceptable levels and the controller initiates its negative current limit protection. Similar to normal overcurrent, negative current protection is enabled by monitoring the current through the lower FET. When the valley point of the inductor current reaches negative current limit, the lower FET is turned off and the upper FET is forced on until current reaches the positive current limit or an internal clock signal is issued. At this point, the lower FET is allowed to operate. If the current is again pulled to the negative limit on the next cycle, the upper FET is forced on and the current is forced to 1/6 of the positive
current limit. At this point, the controller turns off both FETs and waits for COMP1 to indicate return to normal operation. During this time, the controller applies a 100Ω load from LX1 to PGND and attempt to discharge the output. Negative current limit is a pulse-by-pulse style operation and recovery is automatic.

For the low VIN buck regulator, similar to the overcurrent, the negative current protection is enabled by monitoring the current across the low-side N-FET, as shown in Figure 5 on page 5. When the valley point of the inductor current reaches -1.5A for two consecutive cycles, both P-FET and N-FET shut off. The 100Ω in parallel to the N-FET activates discharging the output into regulation. The control begins to switch when output is within regulation.

4.7.4 Over-Temperature Protection

Over-temperature protection limits the maximum junction temperature of both the wide VIN and low VIN buck regulators in the RAA212422. When the junction temperature (T_J) of the wide VIN buck converter exceeds +150°C, both FETs are turned off and the controller waits for the temperature to decrease by approximately 25°C. During this time PG1 is pulled low. When the temperature is within an acceptable range, the controller initiates a normal soft-start sequence. For continuous operation, do not exceed the +125°C junction temperature rating.

For the low VIN buck regulator, when the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops by 25°C, the device resumes operation by stepping through the soft-start.

4.7.5 Boot Undervoltage Protection (Wide VIN Buck)

During PWM operation near dropout (VIN1 near VOUT1), the regulator may hold the upper FET on for multiple clock cycles. To prevent the boot capacitor from discharging, the lower FET is forced on for approximately 200ns every 10 clock cycles.

If the boot capacitor voltage falls below 1.8V, the boot undervoltage protection circuit turns on the lower FET for 400ns to recharge the capacitor. This operation can arise during long periods of no switching, such as PFM no load situations.

4.8 Discharge Mode/Soft-Stop (Low VIN Buck)

When a transition to shutdown mode occurs or the VIN UVLO is set, the output discharges to GND through an internal 100Ω switch.

4.9 100% Duty Cycle (Low VIN Buck)

The RAA212422 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level at which the device can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty cycle operation is the product of the load current and the ON-resistance of the P-FET.

4.10 Power Derating Characteristics

To prevent the buck regulators from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 5:

\[ T_{RISE} = (PD)(\theta_{JA}) \]  

where PD is the power dissipated by the regulator and \( \theta_{JA} \) is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, \( T_J \), is given by Equation 6:

\[ T_J = (T_A + T_{RISE}) \]  

where \( T_A \) is the ambient temperature.

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.
5. Application Guidelines

5.1 Simplifying the Design

Although the wide VIN buck converter of RAA212422 offers user programmed options for most parameters, the easiest implementation with fewest components involves selecting internal settings for SS1, COMP1, and FS1.

The low VIN buck converter offers both internal and external compensation options. Tables 1 and 2 on page 4 provide component value selections for a variety of output voltages for the wide VIN and low VIN buck regulators and allow the designer to implement solutions with minimal effort. X5R or X7R ceramic capacitors are recommended for small solution size and low profile designs.

5.2 Operating Frequency (Wide VIN Buck)

The RAA212422 wide VIN buck converter operates at a default switching frequency of 500kHz if the FS1 pin is tied to VCC1. Tie a resistor from the FS1 pin to GND to program the switching frequency from 300kHz to 2MHz, as shown in Equation 7.

\[
R_{FS1}[\text{k}\Omega] = 108.75\text{k}\Omega \cdot \left( t - 0.2\mu s \right) / (1\mu s)
\]

where:

- \( t \) is the switching period in \( \mu s \)

Figure 55 shows the desired switching frequency and its corresponding \( R_{FS1} \).

5.3 Minimum On/Off-Time Limitation

Minimum on-time \( (t_{\text{MIN, ON}}) \) is the shortest duration of time that the HS FET can be turned on and minimum off time \( (t_{\text{MIN, OFF}}) \) is the shortest duration of time that the HS FET can be turned off. The typical \( t_{\text{MIN, ON}} \) is 90ns and the typical \( t_{\text{MIN, OFF}} \) is 150ns. For a given \( t_{\text{MIN, ON}} \) and \( t_{\text{MIN, OFF}} \), a higher switching frequency results in a narrower range of allowed duty cycle, which translates to a smaller allowed \( V_{\text{IN}} \) range.

For a given output voltage \( (V_{\text{OUT}}) \) and switching frequency \( (f_{\text{SW}}) \), the maximum allowed voltage is given by (Equation 8):

\[
V_{\text{IN(max)}} = \frac{V_{\text{OUT}}}{f_{\text{SW}} \times t_{\text{MIN, ON}}}
\]
5. Application Guidelines

The minimum allowed voltage is given by (Equation 9):

(EQ. 9) \[ V_{IN(min)} = \frac{V_{OUT}}{1 - f_{SW} \times t_{MIN\_OFF}} \]

Table 3 shows the recommended switching frequencies for the various V_{OUT} to operate up to the maximum V_{IN} (40V).

<table>
<thead>
<tr>
<th>V_{IN} (max) (V)</th>
<th>V_{OUT} (V)</th>
<th>f_{SW} (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>5</td>
<td>500</td>
</tr>
<tr>
<td>40</td>
<td>3.3</td>
<td>500</td>
</tr>
<tr>
<td>40</td>
<td>2.5</td>
<td>500</td>
</tr>
<tr>
<td>40</td>
<td>1.8</td>
<td>300</td>
</tr>
</tbody>
</table>

5.4 Synchronization Control (Wide V_{IN} Buck)

The wide V_{IN} buck converter operation frequency can be synchronized up to 2MHz by an external signal applied to the SYNC1 pin. The rising edge on the SYNC1 triggers the rising edge of LX1. To properly synchronize, the external source must be at least 10% greater than the programmed free running IC frequency.

5.5 Output Inductor Selection

The inductor value determines the converter’s ripple current. A reasonable starting point for choosing the ripple current, \( \Delta I \), is 30% of the total load current. You can calculate the inductor value using Equation 10:

(EQ. 10) \[ L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \]

As an example, using \( V_{IN1} = 24V \), \( V_{OUT1} = 5V \), \( f_{sw} = 500kHz \), \( I_{OUT1} = 1.1A \), and \( \Delta i/I_{OUT1} = 30\% \), the inductance is calculated as follows:

(EQ. 11) \[ L_1 = \frac{24V - 5V}{500kHz \times 0.3 \times 1.1A} \times \frac{5V}{24V} = 24\mu H \]

Choose a standard inductance value of 22\( \mu H \).

Increasing the inductance value reduces the ripple current and thus the ripple voltage. However, the larger inductance value may reduce the converter’s response time to a load transient. The inductor current rating should be such that it does not saturate in overcurrent conditions. For typical RAA212422 applications, inductor values are generally in the 10\( \mu H \) to 47\( \mu H \) range for the wide V_{IN} buck regulator and 1\( \mu H \) to 2.2\( \mu H \) for the low V_{IN} buck regulator. Generally, higher V_{OUT} requires higher inductance.

5.6 Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and a filtering function to prevent the switching current from flowing back to the battery rail. A good starting point for input capacitor selection is to use at least two 10\( \mu F \) for the wide V_{IN} buck regulator and at least two 22\( \mu F \) for the low V_{IN} buck regulator. X5R or X7R ceramic capacitors.

5.7 Output Capacitor Selection

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are two critical factors when considering an output capacitance choice. The current mode control loop allows the use of low ESR ceramic capacitors and enables small solution size on the PCB. You can also use electrolytic and polymer capacitors.
Although ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In DC/DC converter applications, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturer’s datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published. The result of these considerations may require an effective capacitance much lower than nominal and this value should be used in all design calculations. However, ceramic capacitors are a very good choice in many applications due to their reliability and extremely low ESR.

Use Equation 12 to calculate the required capacitance to meet the ripple voltage level. Additional capacitance can be used.

\[
V_{\text{OUT Ripple}} = \left( \frac{\Delta I}{8 \cdot f_{\text{SW}} \cdot C_{\text{OUT}}} + \Delta I \cdot ESR + \frac{ESL \cdot V_{\text{IN}}}{L} \right)
\]

where:
- \(\Delta I\) is the inductor’s peak-to-peak ripple current
- \(f_{\text{SW}}\) is the switching frequency
- \(C_{\text{OUT}}\) is the output capacitor
- \(ESR\) is the equivalent series resistance of the output capacitor
- \(ESL\) is the equivalent series inductance of the output capacitor
- \(L\) is the output filter inductance

### 5.8 Loop Compensation Design

When COMP1 is not connected to VCC1, the COMP1 pin is active for external loop compensation. The RAA212422 buck converter uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered a state variable because its peak current is constant and the system becomes a single order system. It is much easier to design a Type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. **Figure 56** shows the small signal model of the synchronous buck regulator.

![Figure 56. Small Signal Model of Synchronous Buck Regulator](image-url)
Figure 57 shows the Type II compensator and its transfer function is expressed as shown in Equation 13:

\[
A_v(S) = \frac{V_{COMP}}{V_{FB}} = \frac{GM \cdot R_2}{(C_6 + C_7) \cdot (R_1 + R_2)} \frac{1 + \frac{S}{\omega_{cz1}}}{1 + \frac{S}{\omega_{cz2}}} \frac{1 + \frac{S}{\omega_{cp1}}}{1 + \frac{S}{\omega_{cp2}}}
\]

where

\[
\omega_{cz1} = \frac{1}{R_6 C_6}, \quad \omega_{cz2} = \frac{1}{R_1 C_4}, \quad \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7}, \quad \omega_{cp2} = \frac{R_1 + R_2}{C_4 R_1 R_2}
\]

Compensator design goal:
- High DC gain
- Choose loop bandwidth $f_c$ less than 100kHz
- Gain margin: $>$10dB
- Phase margin: $>$40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of $f_c$ has a unity gain; therefore, the compensator resistance $R_6$ is determined by Equation 14.

\[
R_6 = \frac{2 \pi f_c V_o C_o R_{cs} k}{GM \cdot V_{FB}} = k_1 \cdot f_c V_o C_o
\]

where:
- $GM$ is the transconductance, $g_m$, of the voltage error amplifier in each phase
- $R_{cs}$ is the current sense trans-resistance
- $k$ is a constant to compensate for cross over frequency difference because the feed forward zero is placed at the vicinity of $f_c$
- $k_1$ is a constant that depends on the internal parameters of the buck converter. For the wide $V_{IN}$ buck regulator, $k_1$ is $16.1 \times 10^3$. For the low $V_{IN}$ buck regulator, $k_1$ is $13.9 \times 10^3$
Place the compensator zero in the vicinity of the power stage pole at full load. As an example, the compensator zero is placed at twice the frequency of the power stage pole at full load. Compensator capacitor $C_6$ is then given by Equation 15.

$$C_6 = \frac{R_6 C_o}{2R_6} = \frac{V_o C_o}{2I_o R_6}$$

An inherent integrator pole at DC by virtue of the compensation circuit helps to achieve high DC gain. Place another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower, in Equation 16. An optional zero can boost the phase margin. $\omega_{CZ2}$ is a zero due to $R_1$ and $C_4$.

$$C_7 = \max\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_{SW} R_6}\right)$$

Put feedforward zero at $f_{zff}$ to boost the phase at cross-over. The $f_{zff}$ can be chosen in the vicinity of $f_c$ depending on the amount of phase boost required.

$$C_4 = \frac{1}{2\pi f_{zff} R_1}$$

Example 1: If $V_{IN1} = 24V$, $V_{O1} = 5V$, $I_{O1} = 1.1A$, $f_{SW} = 500kHz$, $R_2 = 90.9k\Omega$, $C_{o1} = 32.1\mu F/5m\Omega$, $L_1 = 22\mu H$, and $f_c = 50kHz$, compensator resistance $R_6$:

$$R_6 = 16.1 \times 10^3 \cdot 50kHz \cdot 5V \cdot 32.1\mu F = 129.3k\Omega$$

Use $130k\Omega$ as the closest standard value for $R_6$.

$$C_6 = \frac{5V \cdot 32.1\mu F}{1.1A \cdot 130k\Omega \cdot 2} = 0.497nF$$

$$C_7 = \max\left(\frac{5m\Omega \cdot 32.1\mu F}{130k\Omega}, \frac{1}{\pi \cdot 500kHz \cdot 130k\Omega}\right) = (1.2pF, 4.9pF)$$

There is approximately 3pF parasitic capacitance from $V_{COMP1}$ to GND; Therefore, $C_7$ is optional. Use $C_6 = 470pF$ and $C_7 = \text{Open}$. Choose $f_{zff}$ to be $1.5 \times f_c$.

$$C_4 = \frac{1}{2\pi \cdot 50kHz \cdot 1.5 \cdot 90.9k\Omega} = 23.3pF$$

Use $C_4 = 22pF$. Figure 58 on page 31 shows the simulated voltage loop gain, which has a 44kHz loop bandwidth with an 84° phase margin and 21dB gain margin. In the above example, 22µF+47µF 1206 case size ceramic capacitors are used. The effective output capacitance after voltage derating is 32.1µF. In practice, ceramic capacitors have significant derating on voltage and temperature, depending on the type. Refer to the ceramic capacitor datasheet for more details.

The previous description is one of the methodologies to design the compensation network and can be used as a general guideline. However, it is not the only way to choose compensation components. The optimal compensation components may vary depending on your requirements.
Example 2: $V_{IN2} = 5V$, $V_{O2} = 1.2V$, $I_{O2} = 1.5A$, $f_{SW} = 1MHz$, $R_1 = R_2 = 100k\Omega$, $C_{o1} = 44.6\mu F/5m\Omega$, $L_1 = 2.2\mu H$, $f_c = 80kHz$, then compensator resistance $R_6$:

$$R_6 = 13.9 \times 10^3 \cdot 80kHz \cdot 1.2V \cdot 44.6\mu F = 59.5k\Omega$$

Use 60kΩ as the closest standard value for $R_6$.

$$C_6 = \frac{1.2V \cdot 44.6\mu F}{1.5A \cdot 60k\Omega} = 297pF$$

$$C_7 = \max\left(\frac{5m\Omega \cdot 44.6\mu F}{60k\Omega}, \frac{1}{\pi \cdot 1MHz \cdot 60k\Omega}\right) = (3.7pF, 5.3pF)$$

There is approximately 3pF parasitic capacitance from $V_{COMP1}$ to GND; Therefore, $C_7$ is optional. Use $C_6 = 270pF$ and $C_7 = OPEN$. Choose $f_{ZFB}$ to be at $f_c$.

$$C_4 = \frac{1}{2\pi \cdot 80kHz \cdot 100k\Omega} = 20pF$$

Use $C_4 = 22pF$. Figure 59 shows the simulated voltage loop gain. It shows that it has a 81kHz loop bandwidth with a 62° phase margin and 22dB gain margin.
6. Layout Suggestions

Proper layout of the power converter minimizes EMI and noise, and ensure first pass success of the design. Follow these layout guidelines to help optimize the design.

1. Place the input ceramic capacitors as close as possible to the IC VIN pin and power ground. Keep this loop (input ceramic capacitor, IC VIN pin, and power ground) as small as possible to reduce the trace parasitic inductance and hence reduce voltage spikes.

2. Place the input aluminum bulk capacitor close to the input ceramic capacitors.

3. Keep the phase node copper area small, but large enough to handle the load current.

4. Place the output capacitors close to the power stage components.

5. Place vias at the bottom pad of the IC. Place the bottom pad in a ground copper plane with an area as large as possible in multiple layers for better heat dissipation and removal.

6. One of the most critical connections is to connect the GND pin to the package GND pad. Use vias to directly connect the GND pad to the system GND plane. This connection ensures a low impedance path for all return current and an excellent thermal path to dissipate heat.

7. Place the 1µF ceramic decoupling capacitor at the VCC1 pin (the closest place to the IC). Place vias close to the ground pad of this capacitor.

8. Keep the bootstrap capacitor close to the IC.

9. Place the feedback divider close to the FB1 pin and do not route any feedback components near LX1 or BOOT1. If external components are used for SS1, COMP1, or FS1, the same advice applies.

10. Similarly, for the low VIN buck regulator, place the feedback divider close to the FB2 pin and do not route any feedback components near LX2. If external components are used for COMP2, the same advice applies.

11. Connect the EPAD to the ground plane with low-thermal resistance vias.

12. Connect GND1, GND2, and EPAD to the ground plane.
### 7. Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
</table>
| 1.00 | Jul 8, 2019 | Updated Title                  
                  Updated page 1 description. 
                  Updated Features section. 
                  Updated Figures 1, 2, and 5. 
                  Updated the title for Figures 12, 13, 20, and 22. 
                  Updated SYNC1 pin description. 
                  Added PFM Peak Current Limit spec on page 10. 
                  Updated “Typical Performance Curves”. 
                  Added “Light Load Operation” on page 22. 
                  Updated Boot Undervoltage Protection (Buck) section. 
                  Added Minimum On/Off-Time Limitation section. |
| 0.00 | Nov 9, 2018 | Initial release.                                                            |
8. Package Outline Drawing

L22.3x6
22 Lead Thin Dual Flat No-Lead Plastic Package (TDFN)
Rev 0, 3/18

For the most recent package outline drawing, see L22.3x6.

Notes:

1. Dimensions are in millimeters. Dimensions in ( ) for reference only.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metalized terminal and is measured between 0.20mm and 0.30mm from the terminal lip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
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