R9A06G150

ASSP for voice command and control based on RISC-V

R01DS0405EJ0100
Rev.1.00
Nov 18, 2022

Leading-performance 100 MHz RISC-V Andes D25F core, 256 KB code flash memory with background operation, 16 KB Data flash memory, and 128 KB SRAM with Parity. High-integration with Quad SPI.

Features

■ RISC-V Andes D25F Core

- RISC-V instruction-set architecture (RV32I)
- Maximum operating frequency: 100 MHz
- Andes Physical Memory Protection unit (Andes PMP) with 16 regions
- Debug and Trace: RISC-V External Debug Support
- Debug Port: JTAG

■ Memory

- 256-KB code flash memory
- 16-KB data flash memory (100,000 program/erase (P/E) cycles)
- 128-KB SRAM

■ Connectivity

- Serial Communications Interface (SCI) × 2
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding
- I3C bus interface (I3C)
- Serial Peripheral Interface (SPI)
- Quad Serial Peripheral Interface (QSPI)
- Serial Sound Interface Enhanced (SSIE) × 2
- PDM Interface × 2
- IrDA interface

■ Analog

- 12-bit A/D Converter (ADC12) with 2 sample-and-hold circuits
- 12-bit D/A Converter (DAC12) × 2
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 16-bit (GPT16) × 4
- Low Power Asynchronous General Purpose Timer (AGTW) × 4

■ System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL
- Clock out support

■ General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating Voltage

- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages

- Ta = -40°C to +85°C
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)
  - 24-pin QFN (4 mm × 4 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software-compatible Andes AndesCore™ D25F 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates a high-performance Andes AndesCore™ D25F core running up to 100 MHz with the following features:

- 256 KB code flash memory
- 128 KB SRAM
- Quad Serial Peripheral Interface (QSPI)
- Analog peripherals

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Andes AndesCore™-D25F	• Maximum operating frequency: up to 100 MHz • Andes AndesCore™ D25F: – Revision: 2.4.0 – AndeStar V5 instruction-set architecture (ISA) • RISC-V RV32I base integer instruction set • RISC-V C standard extension for compressed instructions • RISC-V M standard extension for integer multiplication and division • RISC-V A standard extension for atomic instructions • RISC-V F standard extensions for single-precision floating-point • AndeStar DSP extension • Andes performance extension • Andes CoDense extension – Physical memory protection (PMP), 16 regions – Performance monitors, cycle and instruction count control and status registers (CSRs) – Andes StackSafe™ hardware stack protection – Andes PowerBrake extension – Instruction and data local memory interface • Machine Timer • RISC-V external debug support – Debug module (DM) • 8 hardware breakpoint/watchpoint registers – Debug transport module (DTM) – JTAG debug port

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory.
Data flash memory	16 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with parity bit.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode
Resets	The MCU provides 12 resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	• Main clock oscillator (MOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL • Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Platform-Level Interrupt Controller (PLIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 External bus interface

Feature	Functional description
External bus	• QSPI area (EQBIU): Connected to the QSPI (external device interface)

Table 1.7 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16 × 4 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. The GPT can also be used as a general-purpose timer.
Low power Asynchronous General Purpose Timer (AGTW)	The low power Asynchronous General Purpose Timer (AGTW) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.

Table 1.7 Timers (2 of 2)

Feature	Functional description
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.8 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 2 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I3C bus interface (I3C)	The I3C bus interface (I3C) has 1 channel. The I3C module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions and MIPI I3C specification. Specific HDR Modes are not covered by conformance test suite (CTS). When CTS for HDR Modes is available, Renesas will confirm CTS tests.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 1 channel. The SPI provides high-speed full-duplex synchronous serial communications with processor and peripheral device.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) has 2 channels. The SSIE peripheral provides functionality to interface with digital audio devices for transmitting I2S/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver or transmitter to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission.
IrDA Interface (IrDA)	The IrDA (Infrared Data Association) interface sends and receives IrDA data communication waveforms in association with SCI0 based on the IrDA standard 1.0.
PDM Interface (PDM)	The PDM (Pulse Density Modulated) Interface has 2 channels that are connectable with up to 2 external microphones which outputs the pulse density modulated (PDM) signal. PDM Interface can filter and convert 1-bit digital data streams that were pulse density modulated at a high sampling rate into 20-bit or 16-bit digital data at a lower sampling rate.

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 6 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 32-bit data. When a selected condition applies, 32-bit data is compared and an interrupt can be generated.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

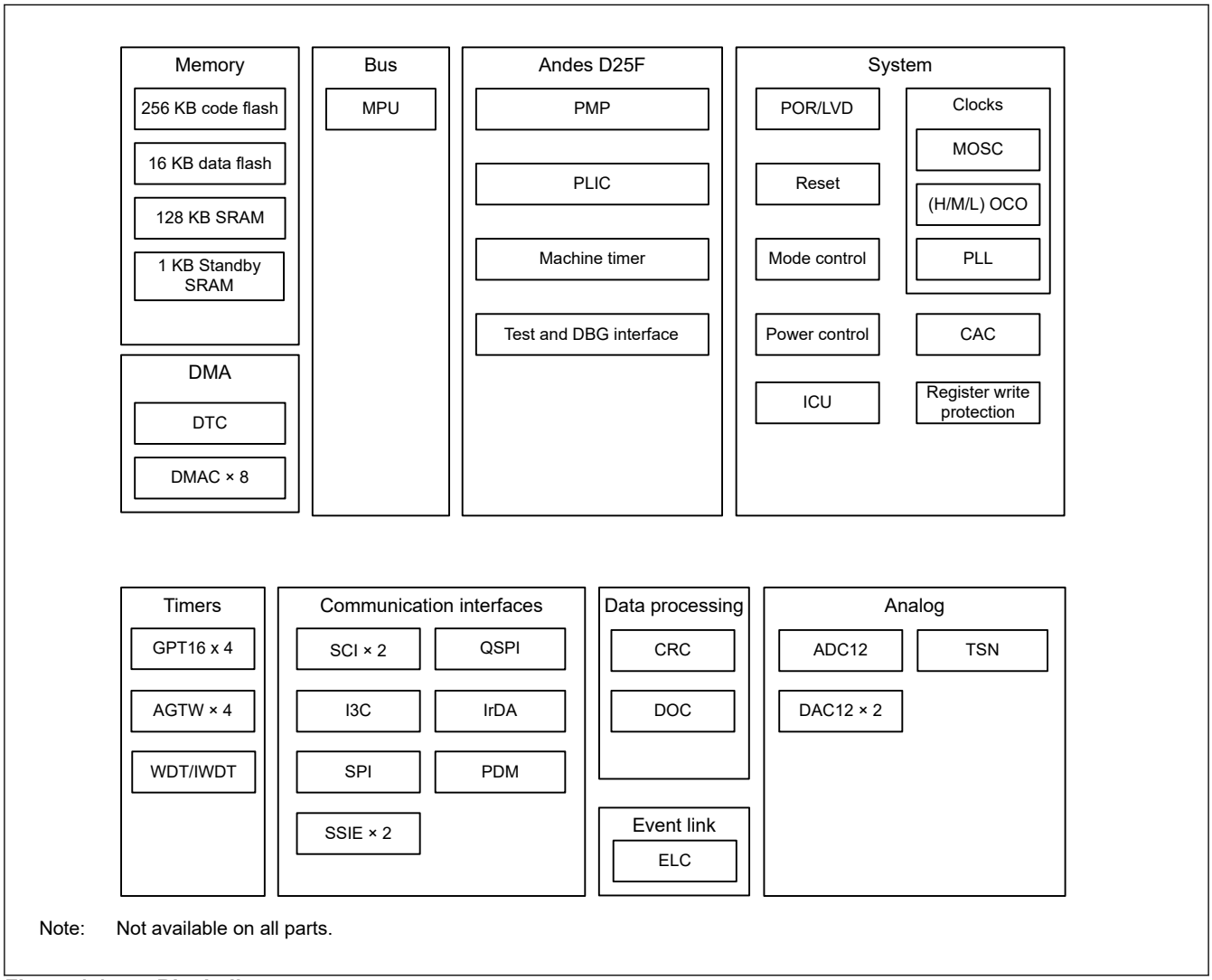


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.11 shows a list of products.

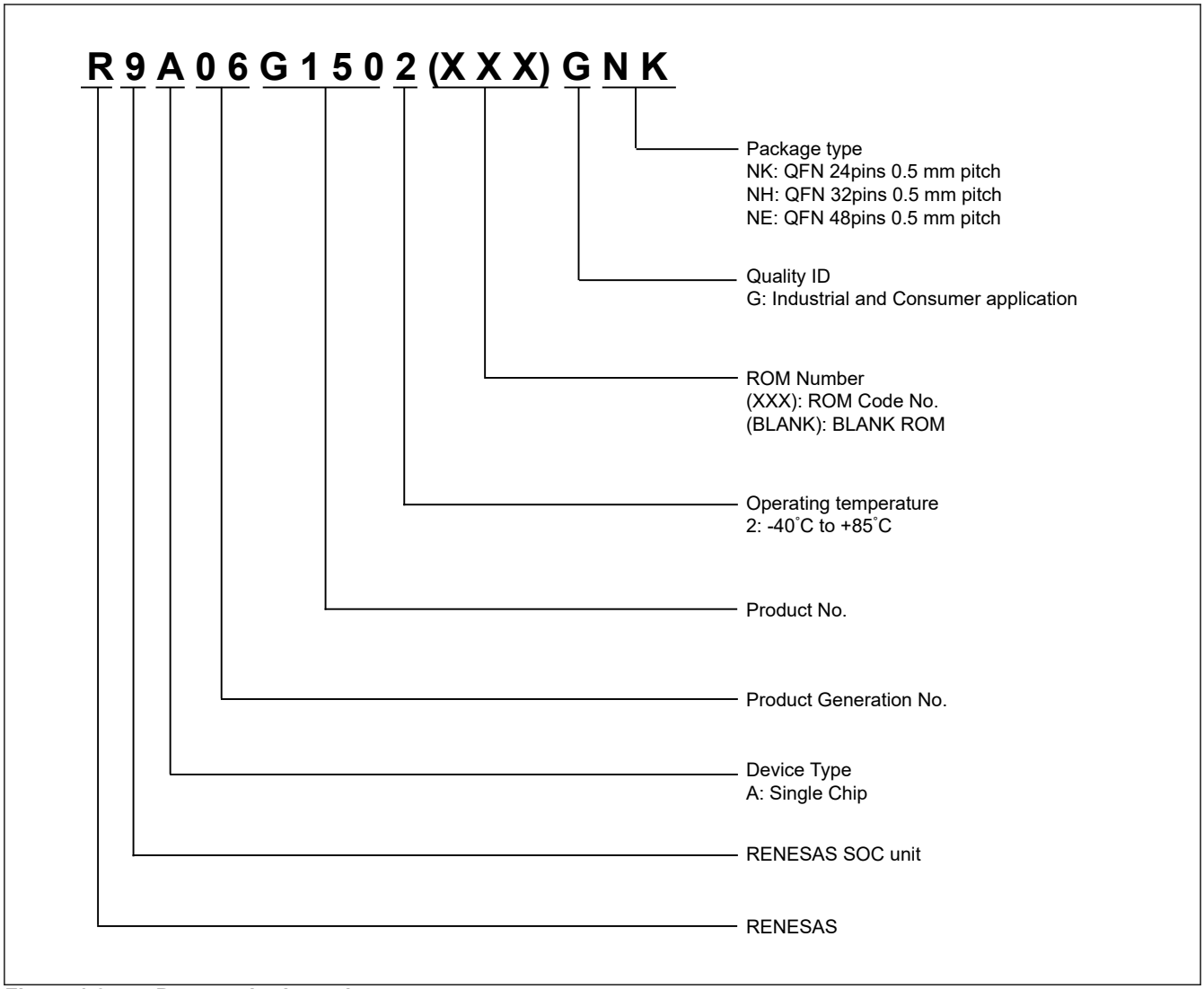


Figure 1.2 Part numbering scheme

Table 1.11 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R9A06G1502GNE	PWQN0048KC-A	256 KB	16 KB	128 KB	-40 to +85°C
R9A06G1502GNH	PWQN0032KE-A				
R9A06G1502GNK	PWQN0024KG-A				

1.4 Function Comparison

Table 1.12 Function Comparison

Parts number		R9A06G1502GNE	R9A06G1502GNH	R9A06G1502GNK
Pin count		48	32	24
Package		QFN		
Code flash memory		256KB		
Data flash memory		16 KB		
SRAM		128 KB		
	Parity	128 KB		
Standby SRAM		1 KB		
DMA	DTC	Yes		
	DMAC	8		
System	CPU clock	100 MHz (max.)		
	CPU clock sources	MOSC, HOCO, MOCO, LOCO, PLL		
	CAC	Yes		
	WDT/IWDT	Yes		
Communication	SCI	2		
	I3C	1		
	SPI	1		
	QSPI	1		0
	SSIE	2		
	IrDA	1		
	PDM	2		
Timers	GPT16*1	4		
	AGTW*1	4		
Analog	ADC12	Unit 0: 6	Unit 0: 4	
	DAC12	2		
	TSN	Yes		
Data processing	CRC	Yes		
	DOC	Yes		
Event control	ELC	Yes		

Note 1. Available pins depend on the Pin count, about details see section 1.7. Pin Lists.

1.5 Pin Functions

Table 1.13 Pin functions (1 of 2)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	TMS	I/O	On-chip emulator pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
GPT	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
AGTW	AGTWEEn	Input	External event input enable signals
	AGTWIOn	I/O	External event input and pulse output pins
	AGTWOn	Output	Pulse output pins
	AGTWOAn	Output	Output compare match A output pins
	AGTWOBn	Output	Output compare match B output pins
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low

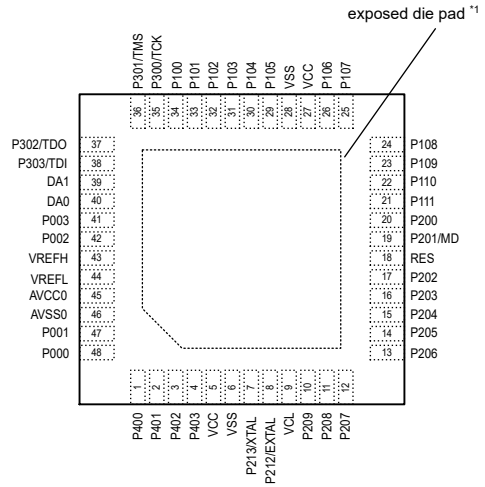
Table 1.13 Pin functions (2 of 2)

Function	Signal	I/O	Description
I3C	SCL	I/O	Input/output pins for the clock
	SDA	I/O	Input/output pins for data
SPI	RSPCK	I/O	Clock input/output pin
	MOSI	I/O	Input or output pins for data output from the master
	MISO	I/O	Input or output pins for data output from the slave
	SSLA0	I/O	Input or output pin for slave selection
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3
SSIE	SSIBCKn	I/O	SSIE serial bit clock pins
	SSILRCKn/SSIFSn	I/O	LR clock/frame synchronization pins
	SSIDATAn	Output	Serial data input/output pins
	AUDIO_CLKn	Input	External clock pin for audio (input oversampling clock)
IrDA	IRTXD0	Output	Data to be transmitted
	IRRXD0	Input	Received data
PDM	PDM_CLKn	Output	Output pins for clock
	PDM_DATAn	Input	Input pins for data
Analog power supply	AVCC0[*1]	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. This is also used as the analog reference voltage for DAC12. Supply this pin with the same voltage as the VCC pin.
	AVSS0[*2]	Input	Analog ground pin. This is used as the analog ground for the respective modules. This is also used as the analog reference ground voltage for DAC12. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12.
	VREFL	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12.[*3]
ADC12	AN0n	Input	Input pins for the analog signals to be processed by the A/D converter.
DAC12	DAn_A, DAn_B	Output	Output pins for the analog signals processed by the D/A converter.
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

Note 1. There is no AVCC0 pin for QFN32-pin and QFN24-pin. For QFN32-pin and QFN24-pin, the analog block supply voltage and the analog reference voltage of the DAC12 are supplied from the VCC pin.
Note 2. There is no AVSS0 pin for QFN32-pin and QFN24-pin. For QFN32-pin and QFN24-pin, the analog block ground voltage and the analog reference ground voltage of the DAC12 are supplied from the VSS pin.
Note 3. There is no VREFL pin for QFN32-pin and QFN24-pin.The reference ground voltage for the QFN32-pin and QFN24-pin is supplied from the VSS pin.

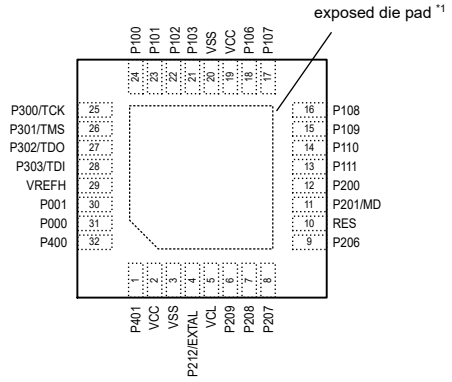
1.6 Pin Assignments

The following figures show the pin assignments from the top view.



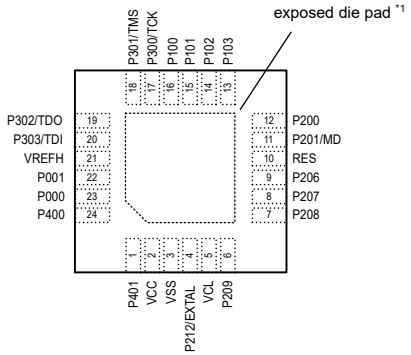
Note.1. Exposed die pad must be connected to VSS.

Figure 1.3 Pin assignment for QFN 48-pin



Note.1. Exposed die pad must be connected to VSS.

Figure 1.4 Pin assignment for QFN 32-pin



Note.1. Exposed die pad must be connected to VSS.

Figure 1.5 Pin assignment for QFN 24-pin

1.7 Pin Lists

Table 1.14 Pin list (1 of 2)

QFN48	QFN32	QFN24	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI (IrDA)/I3C/SPI/QSPI/SSIE/PDM	GPT/AGTW	ADC12/DAC12
1	32	24	CACREF	P400	IRQ4	SSILRCK0/SSIFS0/PDM_DATA0	AGTWEE2	—
2	1	1	—	P401	IRQ5	SSIBCK0/PDM_CLK0	AGTWIO2	—
3	—	—	—	P402	—	—	GTIOC4A_A/AGTWOA2	—
4	—	—	—	P403	—	—	GTIOC4B_A/AGTWOB2	—
5	2	2	VCC	—	—	—	—	—
6	3	3	VSS	—	—	—	—	—
7	—	—	XTAL	P213	—	—	—	—
8	4	4	EXTAL	P212	IRQ6	—	—	—
9	5	5	VCL	—	—	—	—	—
10	6	6	—	P209	—	SCK0/SCL/RSPCK_A	—	—
11	7	7	—	P208	—	RTS_CTS0/SDA/SSLA0_A	—	—
12	8	8	CACREF/CLKOUT	P207	IRQ0-DS	TXD0 (IRTXD0)/MOSI_A	GTIOC6B_A/AGTWEE1	—
13	9	9	—	P206	IRQ1-DS	RXD0 (IRRXD0)/MISO_A	GTIOC6A_A/AGTWIO1	—
14	—	—	—	P205	IRQ12-DS	—	AGTWEE3	—
15	—	—	—	P204	IRQ13-DS	—	AGTWIO3	—
16	—	—	—	P203	—	—	AGTWO3	—
17	—	—	—	P202	—	—	AGTWOA3	—
18	10	10	RES	—	—	—	—	—
19	11	11	MD	P201	—	—	—	—
20	12	12	—	P200	NMI	—	—	—
21	13	—	—	P111	—	QIO3	AGTWO2	—
22	14	—	—	P110	—	QIO2	AGTWOB0	—
23	15	—	—	P109	—	QIO1	GTIOC7B_B	—
24	16	—	—	P108	—	QIO0	GTIOC7A_B	—
25	17	—	—	P107	—	QSSL	GTIOC6B_B	—
26	18	—	—	P106	—	QSPCLK	GTIOC6A_B	—
27	19	—	VCC	—	—	—	—	—
28	20	—	VSS	—	—	—	—	—
29	—	—	—	P105	IRQ8	—	—	—
30	—	—	—	P104	IRQ9	—	AGTWOB3	—
31	21	13	CACREF/CLKOUT	P103	—	TXD9_B/MOSI_B/AUDIO_CLK1	GTIOC5A/AGTWEE0	
32	22	14	—	P102	—	RXD9_B/MISO_B/SSIBCK1	GTIOC5B/AGTWO0	—
33	23	15	—	P101	—	SCK9_B/RSPCK_B/SSIDATA1	GTIOC4A_B/AGTWOA0	—
34	24	16	—	P100	—	RTS_CTS9_B/SSLA0_B/SSILRCK1/SSIFS1	GTIOC4B_B/AGTWIO0	—
35	25	17	TCK	P300	—	SCK9_A	GTIOC7A_A	AN017
36	26	18	TMS	P301	—	RTS_CTS9_A	GTIOC7B_A	AN016
37	27	19	TDO/CLKOUT	P302	—	TXD9_A	—	DA1_B[*1]
38	28	20	TDI	P303	IRQ7	RXD9_A	—	DA0_B[*1]
39	—	—	—	—	—	—	—	DA1_A
40	—	—	—	—	—	—	—	DA0_A
41	—	—	—	P003	IRQ10	—	—	AN003

Table 1.14 Pin list (2 of 2)

QFN48	QFN32	QFN24	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI (IrDA)/I3C/SPI/QSPI/SSIE/PDM	GPT/AGTW	ADC12/DAC12
42	—	—	—	P002	IRQ11	—	—	AN002
43	29	21	VREFH	—	—	—	—	—
44	—	—	VREFL	—	—	—	—	—
45	—	—	AVCC0	—	—	—	—	—
46	—	—	AVSS0	—	—	—	—	—
47	30	22	—	P001	IRQ2	SSIDATA0/PDM_DATA1	—	AN001
48	31	23	—	P000	IRQ3	AUDIO_CLK0/PDM_CLK1	—	AN000

Note: Several pin names have the added suffix of _A, and _B. The suffix can be ignored when assigning functionality.
Note 1. These pins are not available for QFN48.

2. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = 2.7 to 3.6 V
- 2.7 ≤ VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL = 0 V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

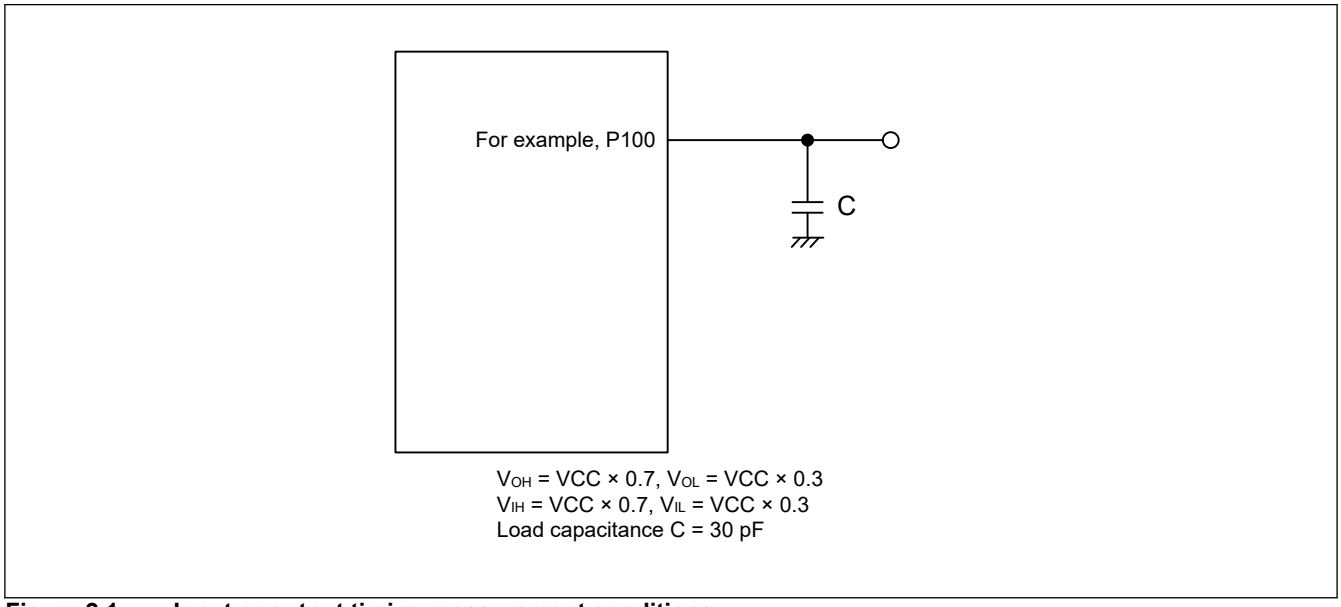


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.0	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature*3	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports P208, P209, P400 and P401 are 5 V tolerant.
Note 2. Connect AVCC0 to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1	—	VCC	—	V
	AVSS0	—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH, AVSS0, and VREFL pins open. Connect the AVCC0 and VREFH pins to VCC, and the AVSS0 and VREFL pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +85°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	
Schmitt trigger input voltage	Peripheral function pin	I3C (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*1 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*2	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*3 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
		Other input pins*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

Note 1. RES and peripheral function pins associated with Ports P208, P209, P400 and P401 (total 5 pins).

Note 2. All input pins except for the peripheral function pins already described in the table.
Note 3. Ports P208, P209, P400 and P401 (total 4 pins).
Note 4. All input pins except for the ports already described in the table.
Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL}

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000, P001, P002, P003, P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	I3C pin	Standard mode	I_{OL}	—	—	3	mA
		Fast mode	I_{OL}	—	—	6	mA
		Fast mode plus	I_{OL}	—	—	20	mA
		High speed mode	I_{OL}	—	—	3	mA
		I3C mode*5	I_{OH}	—	—	–3	mA
			I_{OL}	—	—	3	mA
	Other output pins*4	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
Permissible output current (max value per pin)	Ports P000, P001, P002, P003, P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	I3C pin	Standard mode	I_{OL}	—	—	3	mA
		Fast mode	I_{OL}	—	—	6	mA
		Fast mode plus	I_{OL}	—	—	20	mA
		High speed mode	I_{OL}	—	—	3	mA
		I3C mode*5	I_{OH}	—	—	–3	mA
			I_{OL}	—	—	3	mA
	Other output pins*4	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins		$\Sigma I_{OH\ (max)}$	—	—	–80	mA
			$\Sigma I_{OL\ (max)}$	—	—	80	mA

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. Except for P200, which is an input port.

Note 5. This is the value when I3C SDR or HDR mode is selected.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	I3C	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	I3C*1	V_{OH}	VCC – 0.27	—	—		I_{OH} = –3.0 mA (PRTS.PRTMD = 0)
		V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
		V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
		V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.HSME = 1)
		V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0)
	Ports P208, P209, P400, P401 (total 4 pins)*2	V_{OH}	VCC – 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
		V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\|I_{in}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P200		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	$\|I_{TSI}\|$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P200)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to P7	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Pull-up current serving as the SCL current source	I3C*3	ICS	2	—	12	mA	VCC = 3.0 to 3.6 V V_{in} = 0.3 × VCC to 0.7 × VCC
Input capacitance	All input pins	C_{in}	—	—	8		Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C

Note 1. SCL, SDA (total 2 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when IIC high speed mode is selected.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current[*1]	High-speed mode	Maximum[*2 *13]		I_{CC}[*3]	—	—	28.2	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz
		CoreMark®[*5 *6 *13]			—	12.6	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash[*4 *12]		—	16.2	—		
			All peripheral clocks disabled, while (1) code executing from flash[*5 *6 *12]		—	13	—		
		Sleep mode[*5]			—	4.1[*6*12]	13[*7*13]		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode[*5 *11]				—	0.6	—		ICLK = 1 MHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	6		—
			SNZCR.RXDREQEN = 0		—	0.4	—		—
	Deep Software Standby mode	Power supplied to Standby SRAM			—	16	93	μA	—
		Power not supplied to SRAM	Power-on reset circuit low power function disabled		—	11	25		—
			Power-on reset circuit low power function enabled		—	4	14		—
		Increase when AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		—	20	—		—
	Inrush current on returning from Deep Software Standby mode		Inrush current[*8]	I_{RUSH}	—	160	—	mA	
			Energy of inrush current[*8]	E_{RUSH}	—	1.0	—	μC	
Analog power supply current for QFN-48	During 12-bit A/D conversion			AI_{CC}	—	0.8	1.1	mA	—
	During 12-bit A/D conversion with S/H amp				—	1.8	2.5	mA	—
	Temperature sensor				—	0.1	0.2	mA	—
	During D/A conversion (per unit)		without AMP output		—	0.2	0.6	mA	—
			with AMP output		—	0.7	1.5	mA	—
	Waiting for A/D, D/A conversion (all units)				—	0.5	1.0	mA	—
	ADC12, DAC12 in standby modes (all units)[*10]				—	0.4	4.0	μA	—
Analog power supply current for QFN-32 and QFN-24	Increase during 12-bit A/D conversion			I_{CC}[*9]	—	1.0	1.3	mA	—
	Increase during 12-bit A/D conversion with S/H amp				—	2.0	2.7	mA	—
	Increase Temperature sensor operating				—	0.1	0.2	mA	—
	Increase during D/A conversion (per unit)		without AMP output		—	0.3	0.7	mA	—
			with AMP output		—	0.8	1.6	mA	—
	Increase waiting for A/D, D/A conversion (all units)				—	0.8	1.3	mA	—
Reference power supply current (VREFH)	During 12-bit A/D conversion			AI_{refh}	—	70	120	μA	—
	Waiting for 12-bit A/D conversion				—	0.07	0.5	μA	—
	ADC12 in standby modes				—	0.07	0.5	μA	—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.

I_{CC}Max. = 0.24 × f + 3.9 (max. operation in high-speed mode)
I_{CC} Typ. = 0.12 × f + 1.085 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.156 × f + 0.444 (low-speed mode)
I_{CC}Max. = 0.091 × f + 3.9 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.56MHz).
Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.12MHz).
Note 8. Reference value
Note 9. In QFN-32 and QFN-24, the current is added to ICC.
Note 10. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD20 (12-bit D/A converter module stop bit) are in the module-stop state.
Note 11. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6KHz).
Note 12. PLL output frequency = 100MHz.
Note 13. PLL output frequency = 200MHz.

Table 2.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark*2 *3		I_{CC}	126	µA/MHz	ICLK = 100MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1.56 MHz
	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*2 *3		130		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. PLL output frequency = 100MHz.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.9 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI boot mode*1		0.0084	—	20		—
VCC falling gradient		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 2.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r\ (VCC)} \leq$ VCC × 0.2
		—	—	1	MHz	Figure 2.2 $V_{r\ (VCC)} \leq$ VCC × 0.08
		—	—	10	MHz	Figure 2.2 $V_{r\ (VCC)} \leq$ VCC × 0.06
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

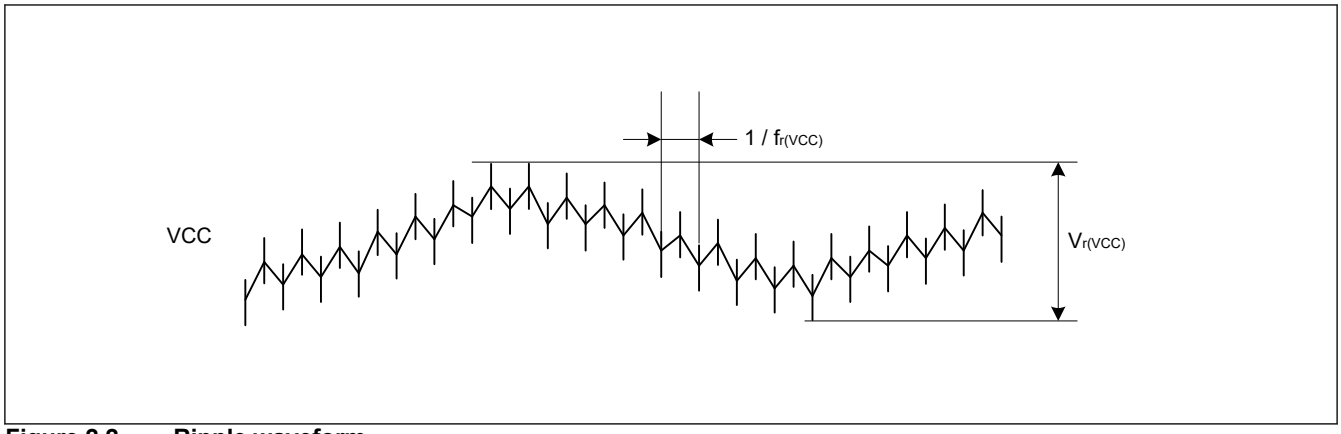


Figure 2.2 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of "section 2.2.1. Tj/Ta Definition".

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of Junction-to-Ambient (°C/W)
  - Ψjt : Thermal Resistance of Junction-to-Top Center Case (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, refer to Table 2.11.

Table 2.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	48-pin QFN (PWQN0048KC-A)	θja	29.1	°C/W	JEDEC standards
	32-pin QFN (PWQN0032KE-A)		29.5		
	24-pin QFN (PWQN0024KG-A)		39.2		
	48-pin QFN (PWQN0048KC-A)	Ψjt	0.15	°C/W	
	32-pin QFN (PWQN0032KE-A)		0.35		
	24-pin QFN (PWQN0024KG-A)		2.43		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.3 AC Characteristics

2.3.1 Frequency

Table 2.12 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLKA)		—	—	100	
	Peripheral module clock (PCLKB)		—	—	50	
	Peripheral module clock (PCLKC)		—*2	—	50	
	Peripheral module clock (PCLKD)		—	—	100	
	Flash interface clock (FCLK)		—*1	—	50	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.13 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKA)		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKC) *2		—*2	—	1	
	Peripheral module clock (PCLKD)		—	—	1	
	Flash interface clock (FCLK)*1		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

2.3.2 Clock Timing

Table 2.14 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 2.3
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time	t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time	t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency	f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1	$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.4
LOCO clock oscillation frequency	f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	60.4	µs	Figure 2.5
ILOCO clock oscillation frequency	f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency	F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time	t_{MOCOWT}	—	—	15.0	µs	—

Table 2.14 Clock timing (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency		f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 85°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	µs	—
HOCO period jitter		—	—	±85	—	ps	—
PLL clock frequency		f_{PLL}	100	—	200	MHz	—
PLL clock oscillation stabilization wait time		t_{PLLWT}	—	—	174.9	µs	Figure 2.6
PLL period jitter	f_{PLL} ≥ 120MHz	—	—	±100	—	ps	—
	f_{PLL} < 120MHz	—	—	±120	—	ps	—
PLL long term jitter		—	—	±300	—	ps	Term: 1µs, 10µs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

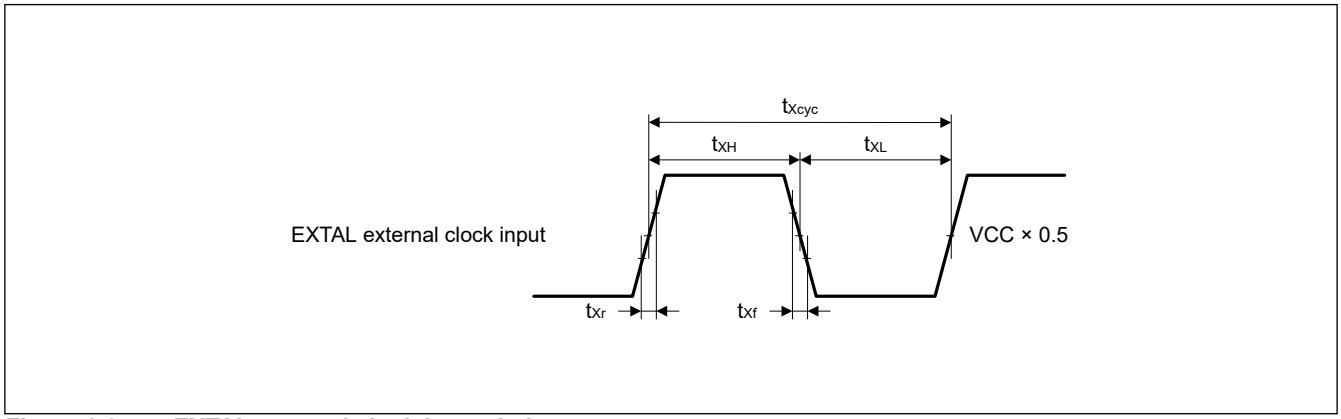


Figure 2.3 EXTAL external clock input timing

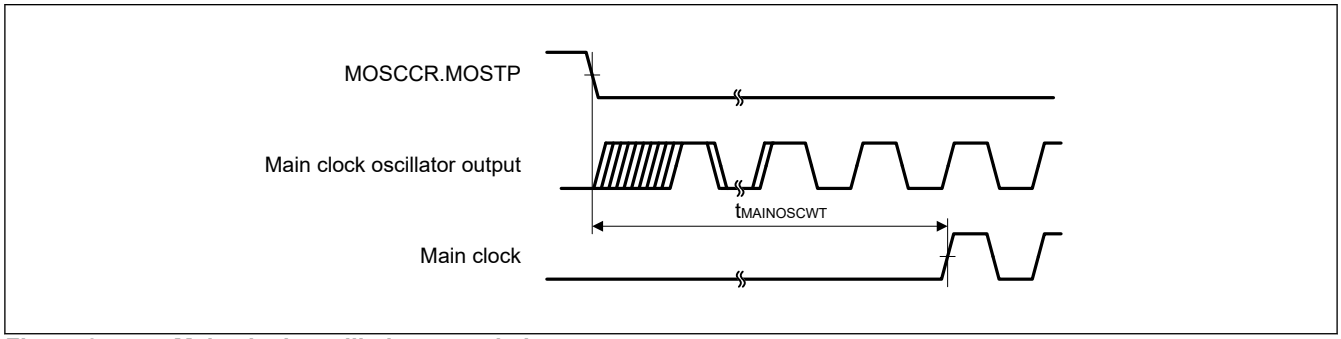


Figure 2.4 Main clock oscillation start timing

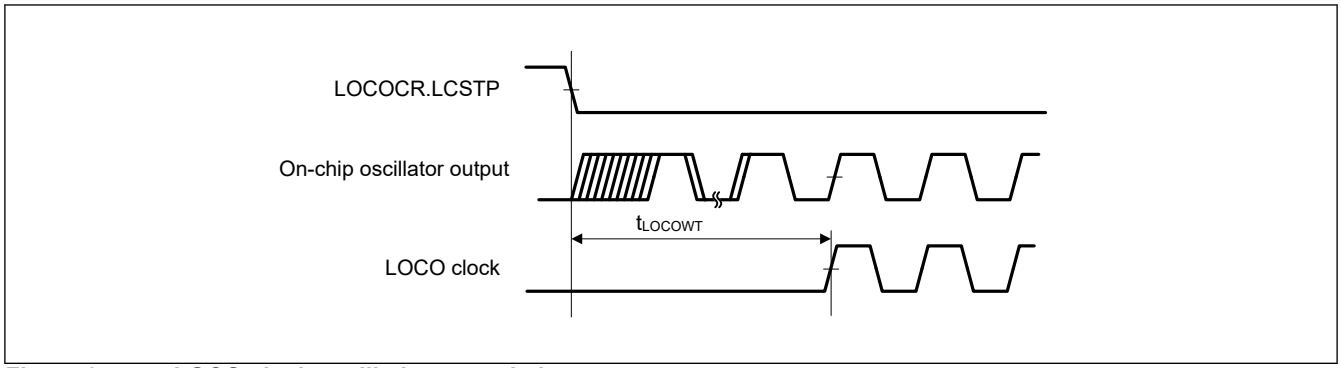


Figure 2.5 LOCO clock oscillation start timing

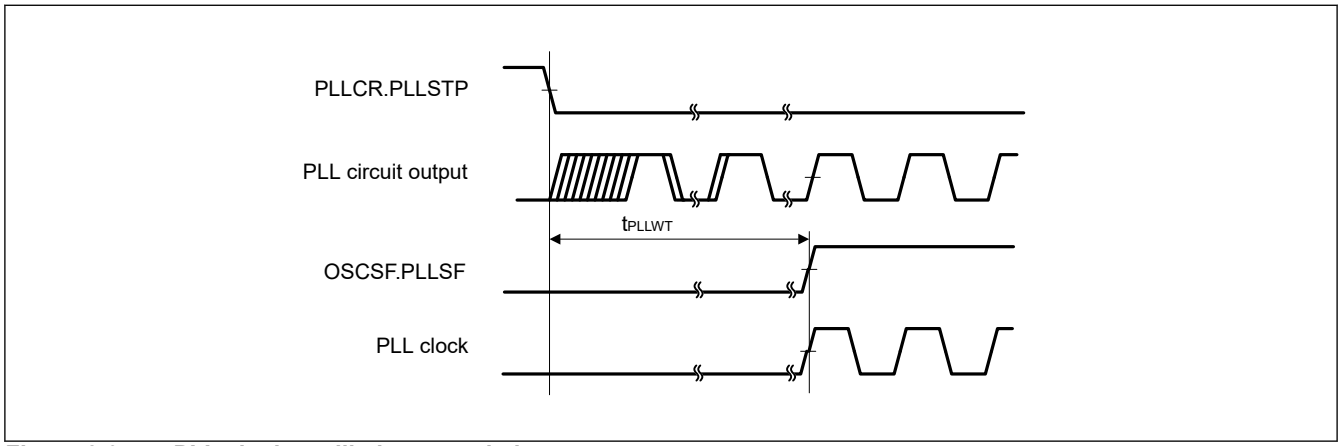


Figure 2.6 PLL clock oscillation start timing

2.3.3 Reset Timing

Table 2.15 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 2.7
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.8
	Software Standby mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	µs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	µs	Figure 2.7
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset)		t_{RESW2}	—	324	397.7	µs	—

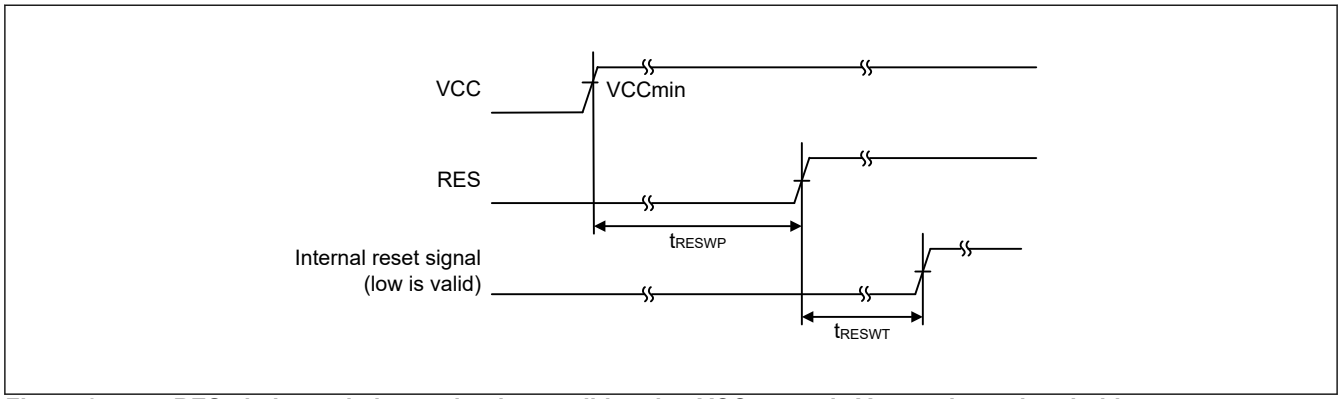


Figure 2.7 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

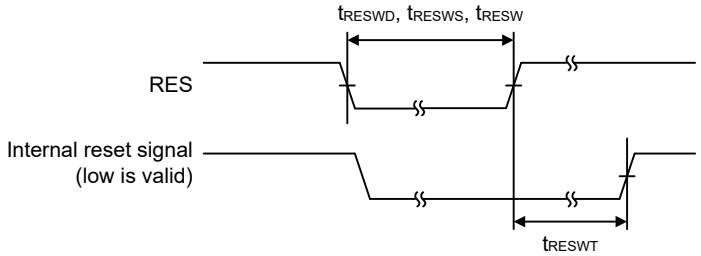


Figure 2.8 Reset input timing

2.3.4 Wakeup Timing

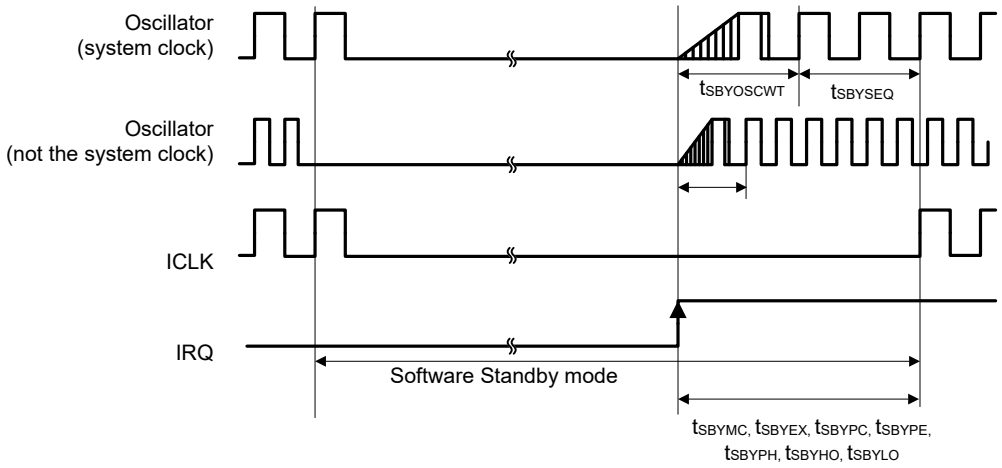
Table 2.16 Timing of recovery from low power modes

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*11	—	2.1	2.4	ms	Figure 2.9 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*11	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*11	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*11	—	170	255	µs	
	System clock source is LOCO*6		t_{SBYLO}*11	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*7		t_{SBYHO}*11	—	55	130	µs	
	System clock source is PLL with HOCO*8		t_{SBYPH}*11	—	175	265	µs	
	System clock source is MOCO clock oscillator*9		t_{SBYMO}*11	—	35	65	µs	
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E		t_{DSBY}	—	0.38	0.54	ms	Figure 2.10
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19		t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	56	—	57	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		t_{SNZ}	—	35*10	70*10	µs	Figure 2.11
	High-speed mode when system clock source is MOCO (8 MHz)		t_{SNZ}	—	11*10	14*10	µs	

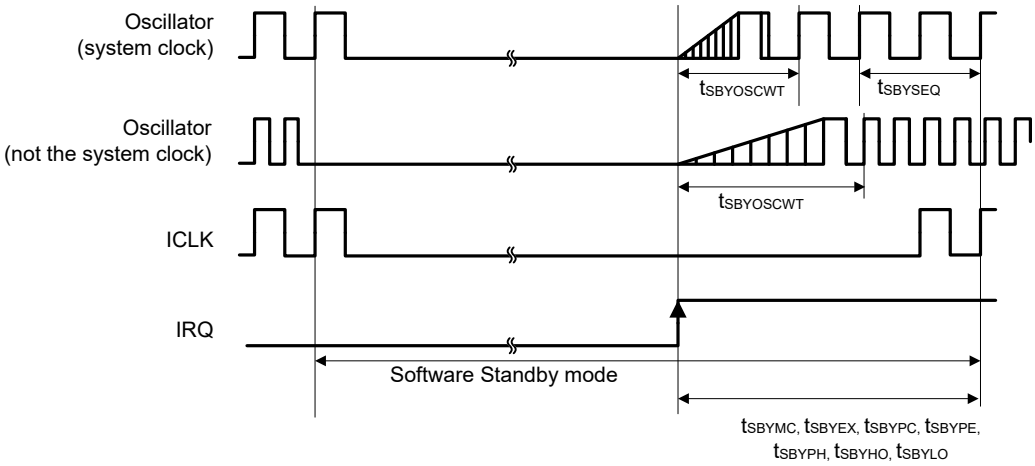
Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating).
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 7. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 8. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
Note 9. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.

Note 10. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 11. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs



When stabilization of the system clock oscillator is slower



When stabilization of an oscillator other than the system clock is slower

Figure 2.9 Software Standby mode cancellation timing

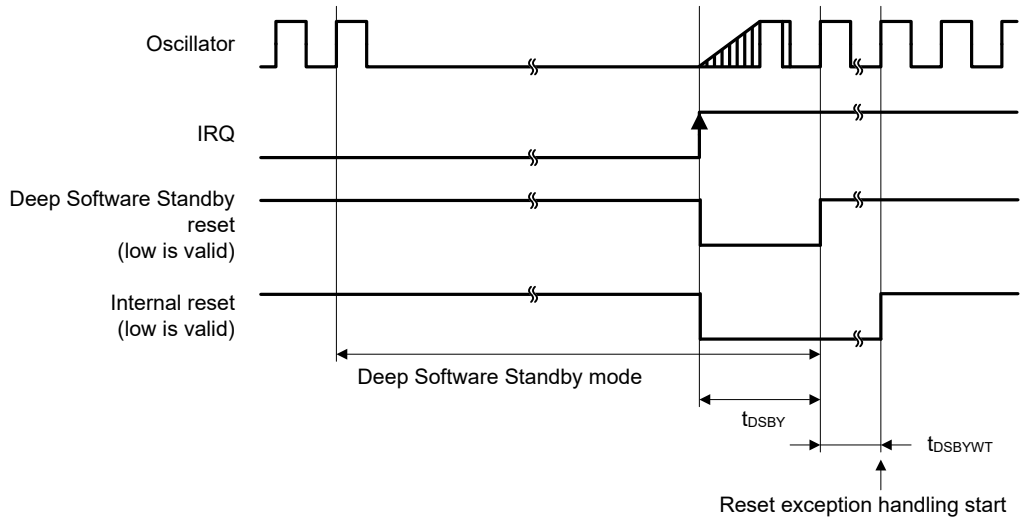
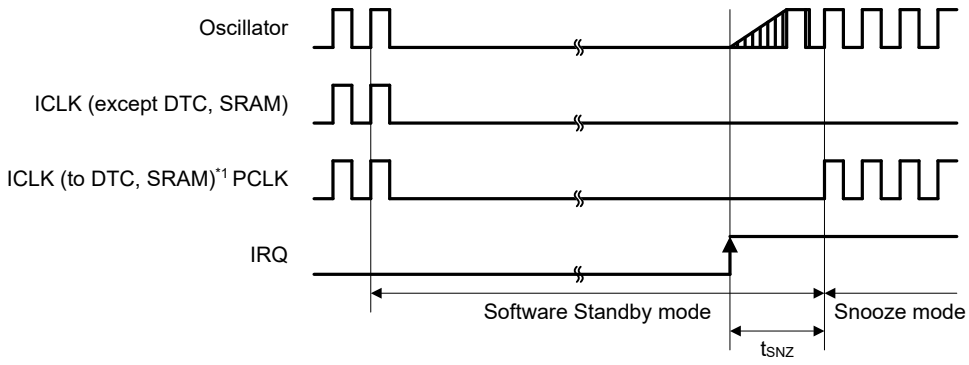


Figure 2.10 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.11 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

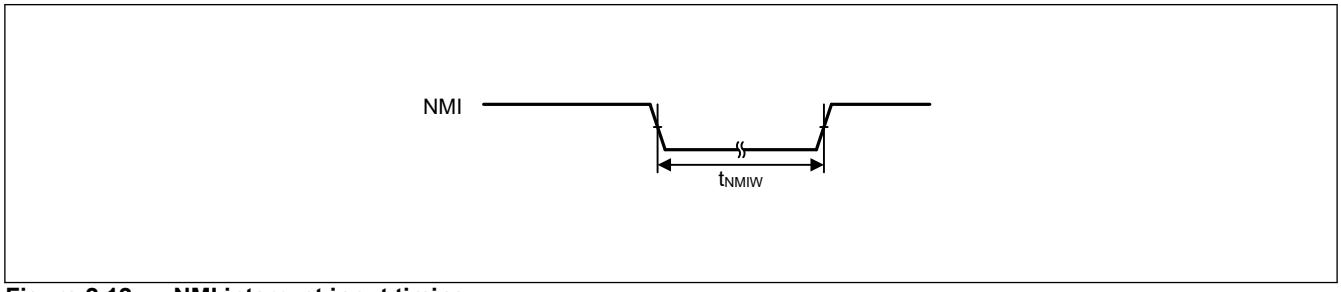


Figure 2.12 NMI interrupt input timing

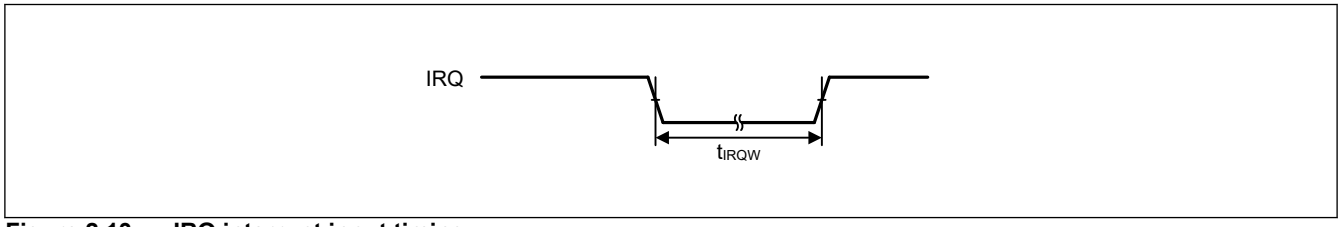


Figure 2.13 IRQ interrupt input timing

2.3.6 I/O Ports, GPT, and AGT Timing

Table 2.18 I/O ports, GPT, and AGT timing

GPT16 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 2.14
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.15
		Dual edge		2.5	—		
	GTIOCxY output skew (x = 4 to 7, Y = A or B)	Middle drive buffer	t_{GTISK}*1	—	4	ns	Figure 2.16
		High drive buffer		—	4		
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*2	100	—	ns	Figure 2.17
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	—	ns	

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

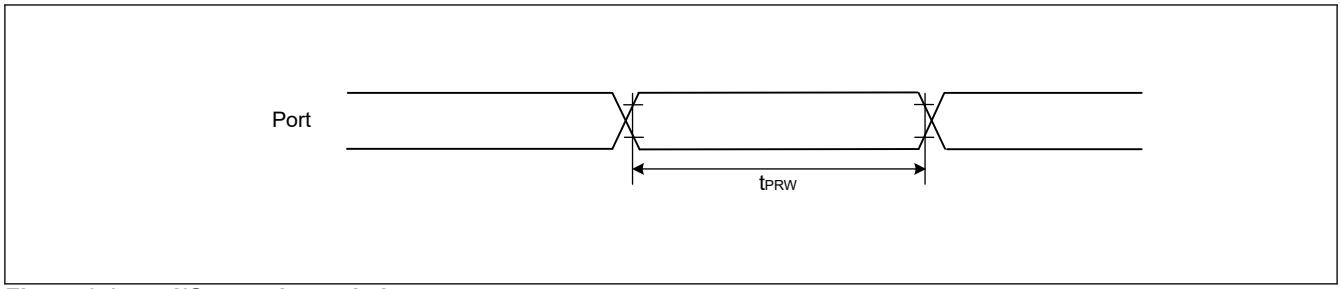


Figure 2.14 I/O ports input timing

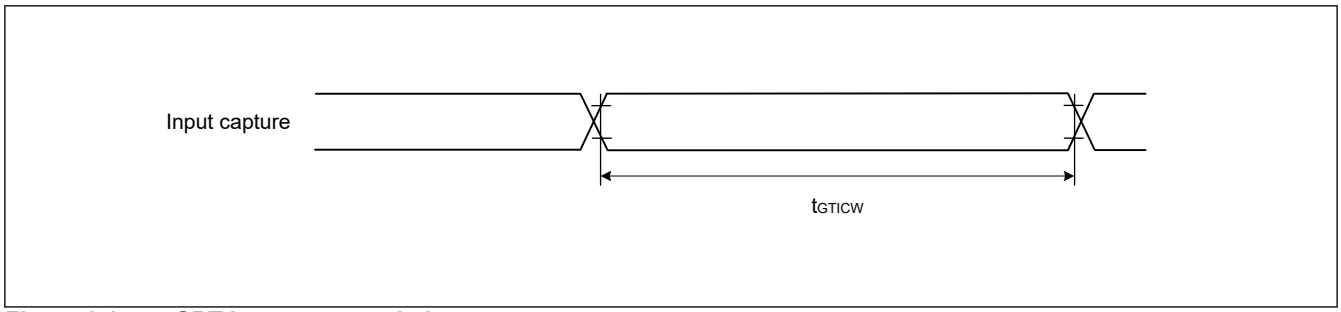


Figure 2.15 GPT input capture timing

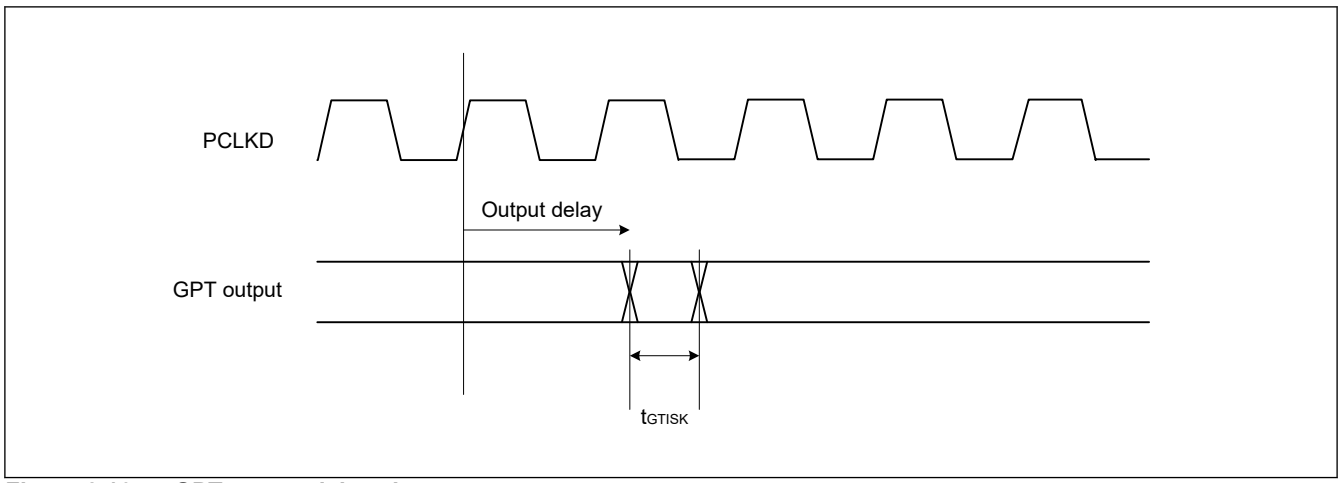


Figure 2.16 GPT output delay skew

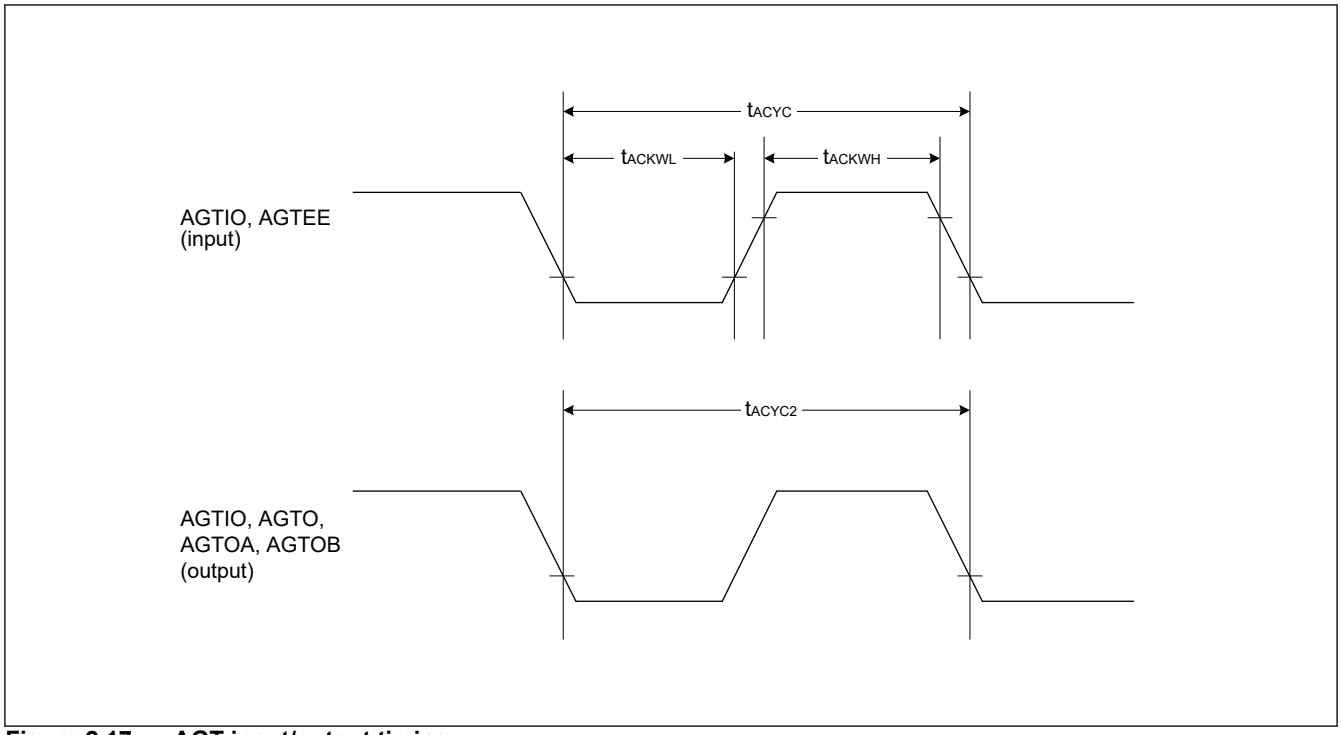


Figure 2.17 AGT input/output timing

2.3.7 CAC Timing

Table 2.19 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$ *1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$ *1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

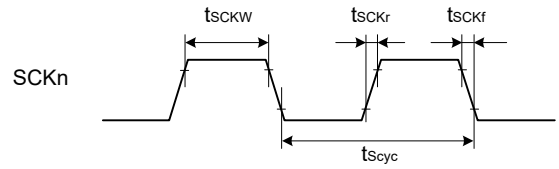
2.3.8 SCI Timing

Table 2.20 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

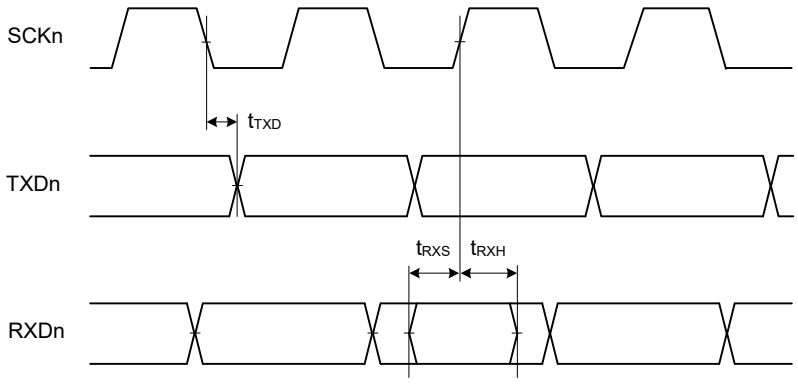
Parameter			Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.18
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay	Clock synchronous master mode (internal clock)	t_{TXD}	—	5	ns	Figure 2.19
		Clock synchronous slave mode (external clock)	t_{TXD}	—	25	ns	
	Receive data setup time	Clock synchronous master mode (internal clock)	t_{RXS}	15	—	ns	
		Clock synchronous slave mode (external clock)	t_{RXS}	5	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.



Note: n = 0, 9

Figure 2.18 SCK clock input/output timing



Note: n = 0, 9

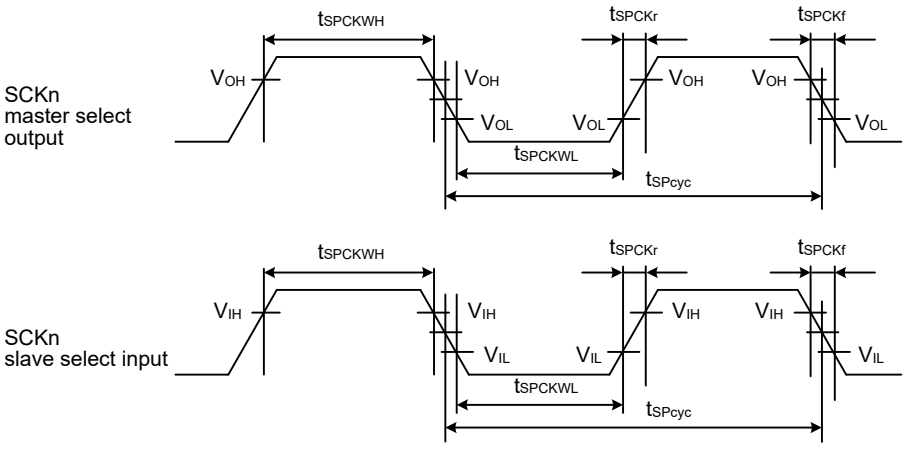
Figure 2.19 SCI input/output timing in clock synchronous mode

Table 2.21 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.20
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Data input setup time	master	t_{SU}	15	—	ns	Figure 2.21 to Figure 2.24
		slave		5	—	ns	
	Data input hold time		t_{H}	5	—	ns	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay	master	t_{OD}	—	5	ns	
		slave		—	25	ns	
	Data output hold time		t_{OH}	-5	—	ns	
	Data rise and fall time		t_{Dr}, t_{Df}	—	5	ns	
	SS input rise and fall time		t_{SSLr}, t_{SSLf}	—	5	ns	
	Slave access time		t_{SA}	—	$3 \times t_{Pcyc} + 25$	ns	Figure 2.24
	Slave output release time		t_{REL}	—	$3 \times t_{Pcyc} + 25$	ns	

Note: t_{Pcyc}: PCLKA cycle.



$V_{OH} = 0.7 \times VCC$, $V_{OL} = 0.3 \times VCC$, $V_{IH} = 0.7 \times VCC$, $V_{IL} = 0.3 \times VCC$

Note: n = 0, 9

Figure 2.20 SCI simple SPI mode clock timing

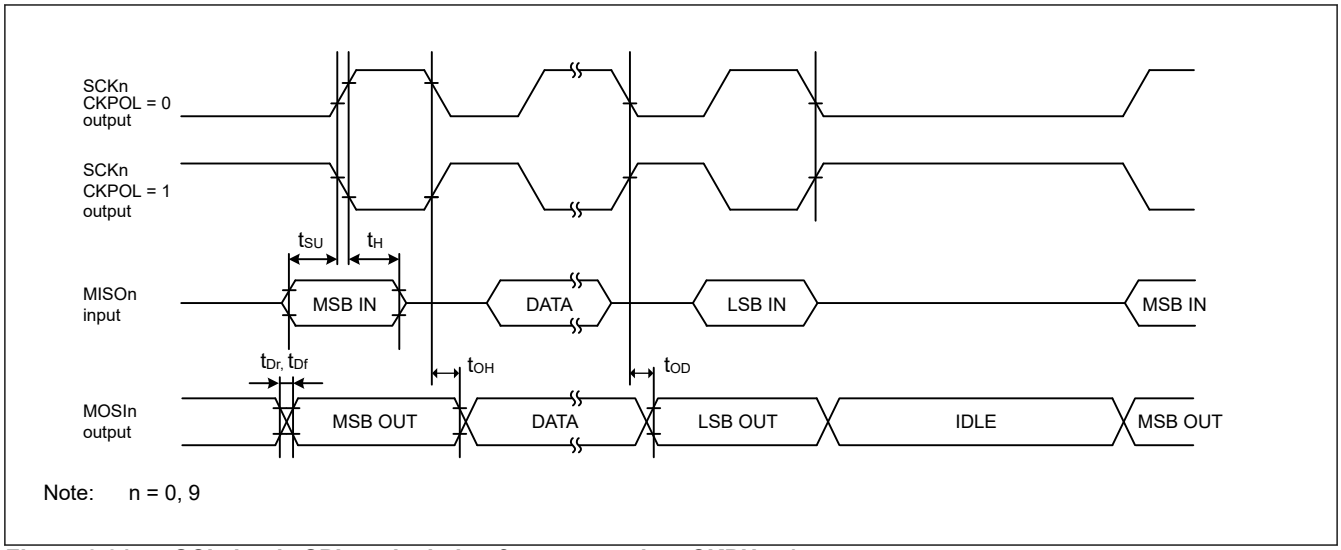


Figure 2.21 SCI simple SPI mode timing for master when CKPH = 1

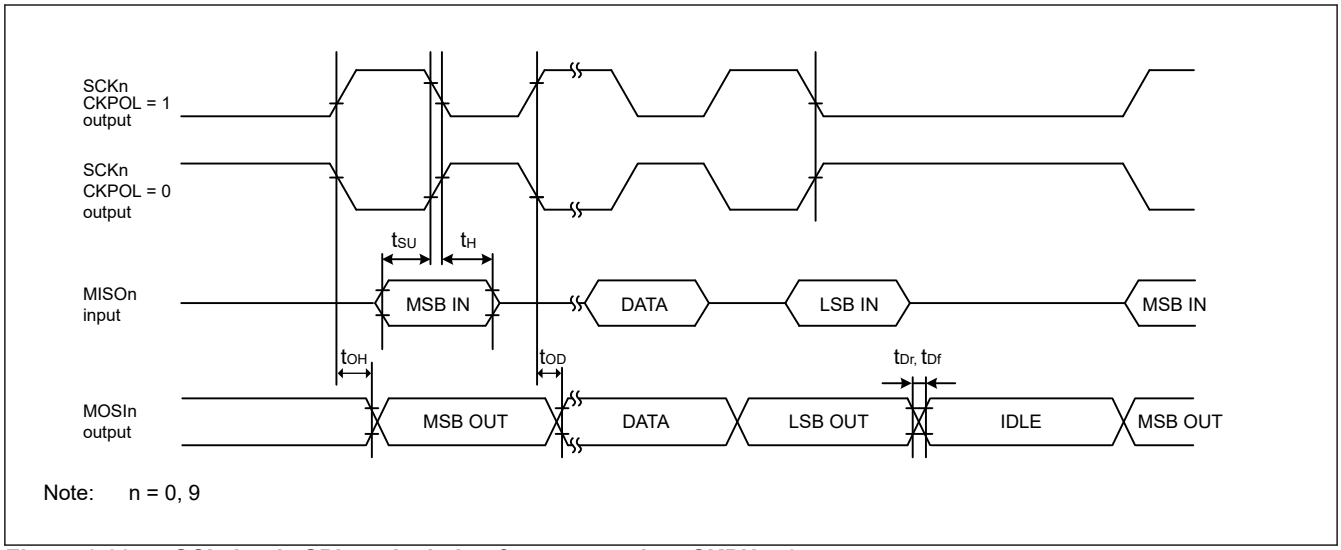


Figure 2.22 SCI simple SPI mode timing for master when CKPH = 0

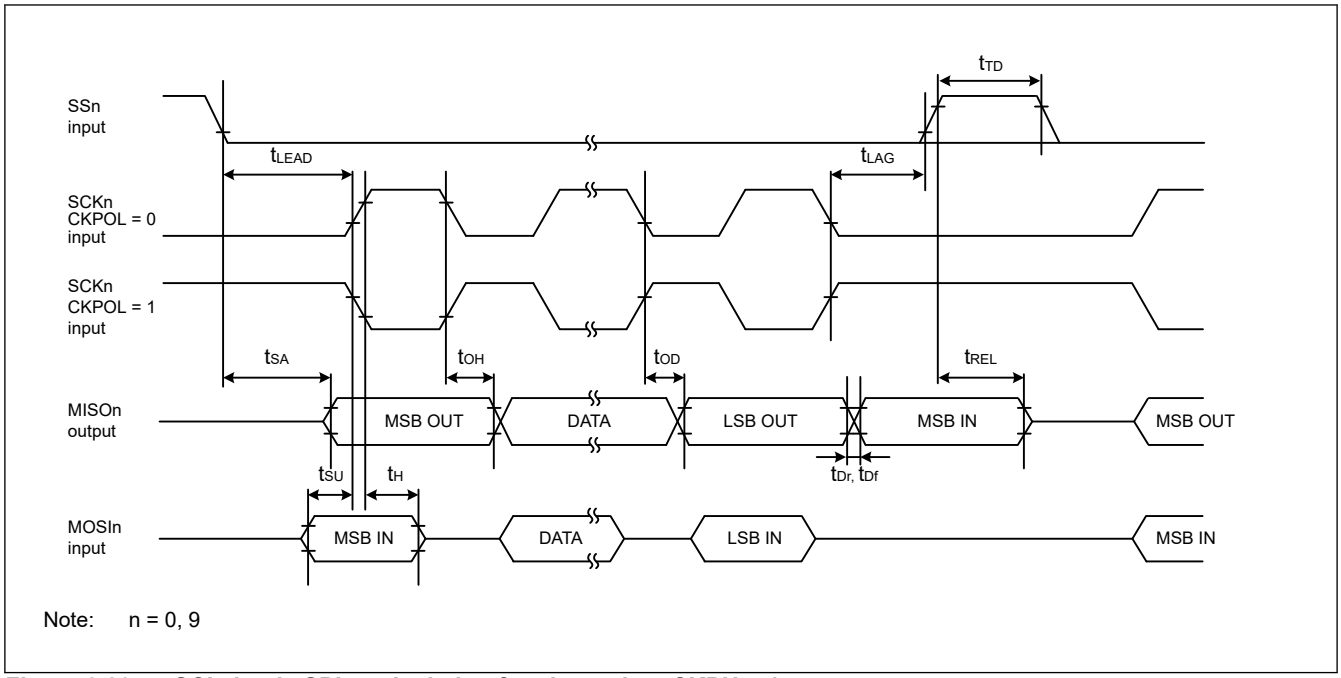


Figure 2.23 SCI simple SPI mode timing for slave when CKPH = 1

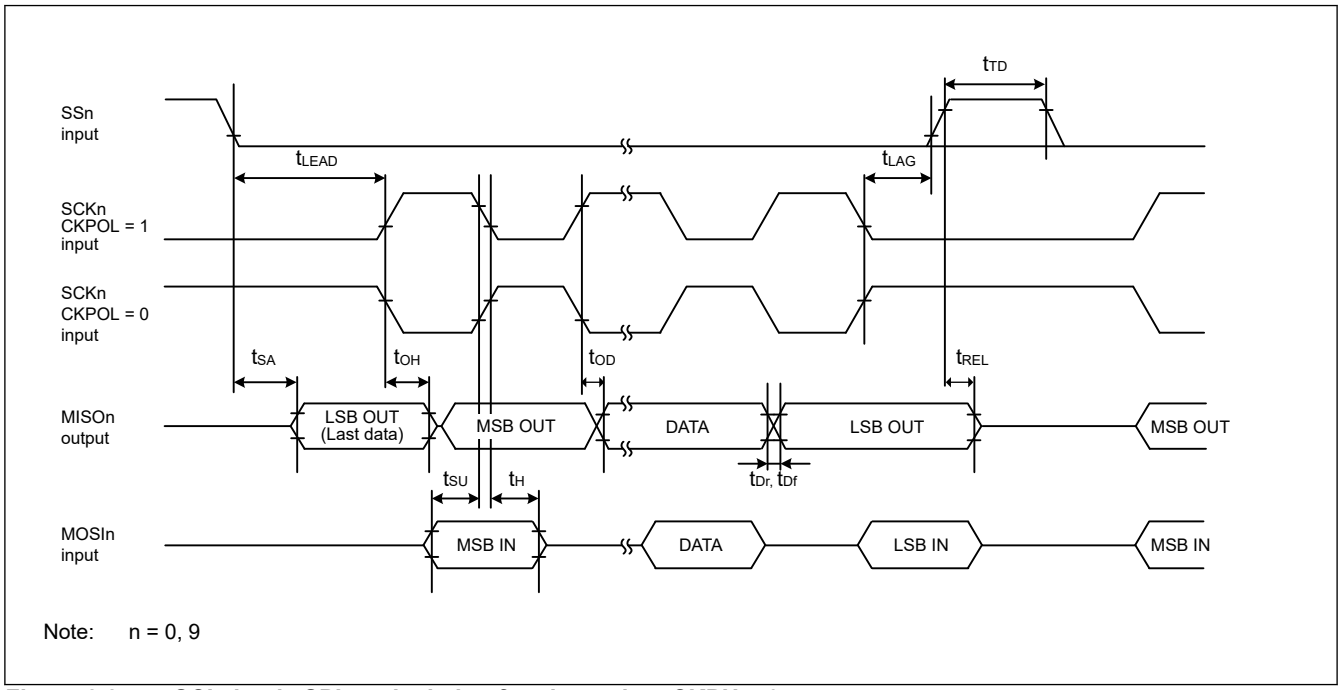


Figure 2.24 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.22 SCI timing (3) (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

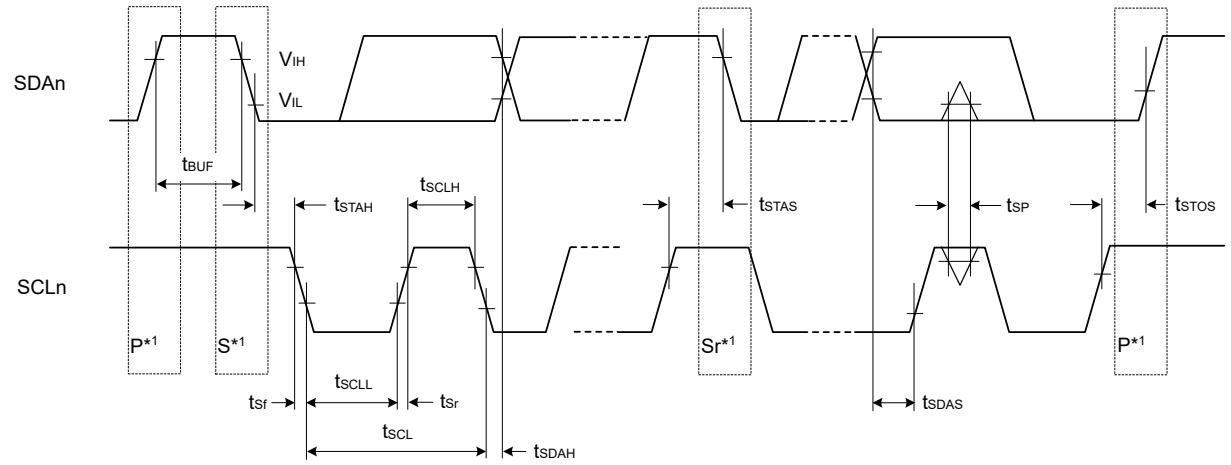
Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.25
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Table 2.22 SCI timing (3) (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.25
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.25 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.23 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.26
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	µs	
	Data input setup time	Master	t_{SU}	4	—	ns	Figure 2.27 to Figure 2.32
		Slave		5	—		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	—	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_{H}	t_{Pcyc}	—		
		Slave	t_{H}	20	—		
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc} - 10^{*1}$	$N \times t_{SPcyc} + 100^{*1}$	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc} - 10^{*2}$	$N \times t_{SPcyc} + 100^{*2}$	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	Data output delay	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}	—	6.3		
		Slave	t_{OD}	—	20		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	25	ns	Figure 2.31 and Figure 2.32
	Slave output release time		t_{REL}	—	25		

Note: t_{Pcyc}: PCLKA cycle.

Note: Must use pins that have a letter appended to their name, for instance “_A”, “_B”, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. N is set to an integer from 1 to 8 by the SPCKD register.
Note 2. N is set to an integer from 1 to 8 by the SSLND register.

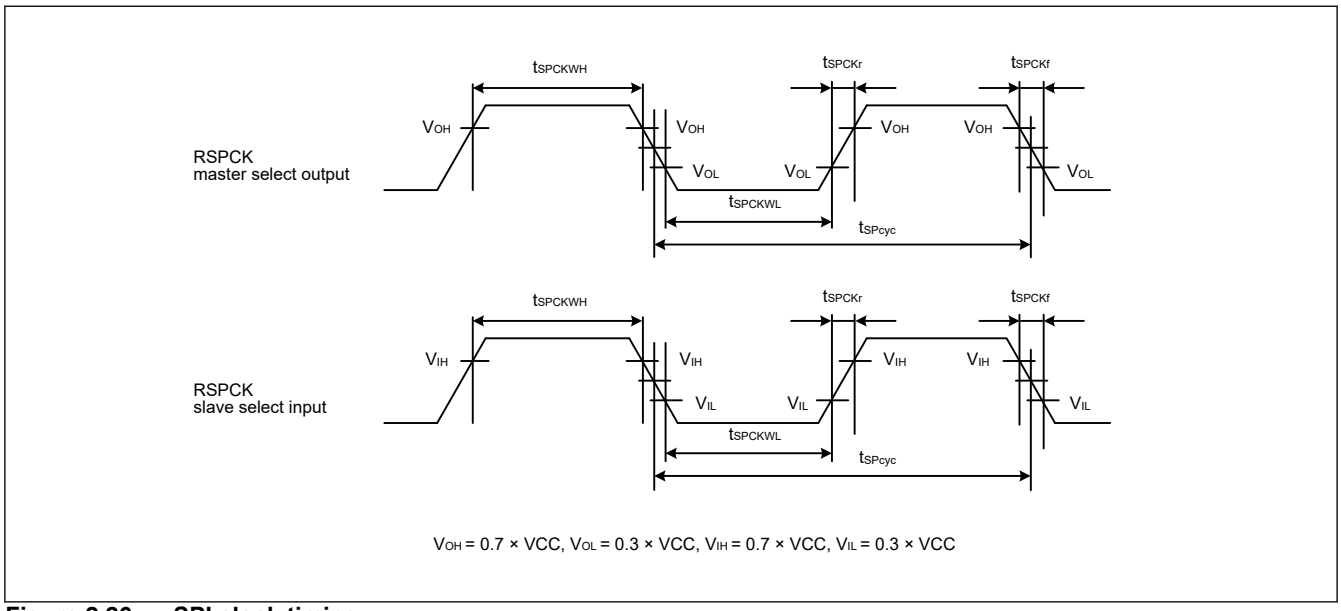


Figure 2.26 SPI clock timing

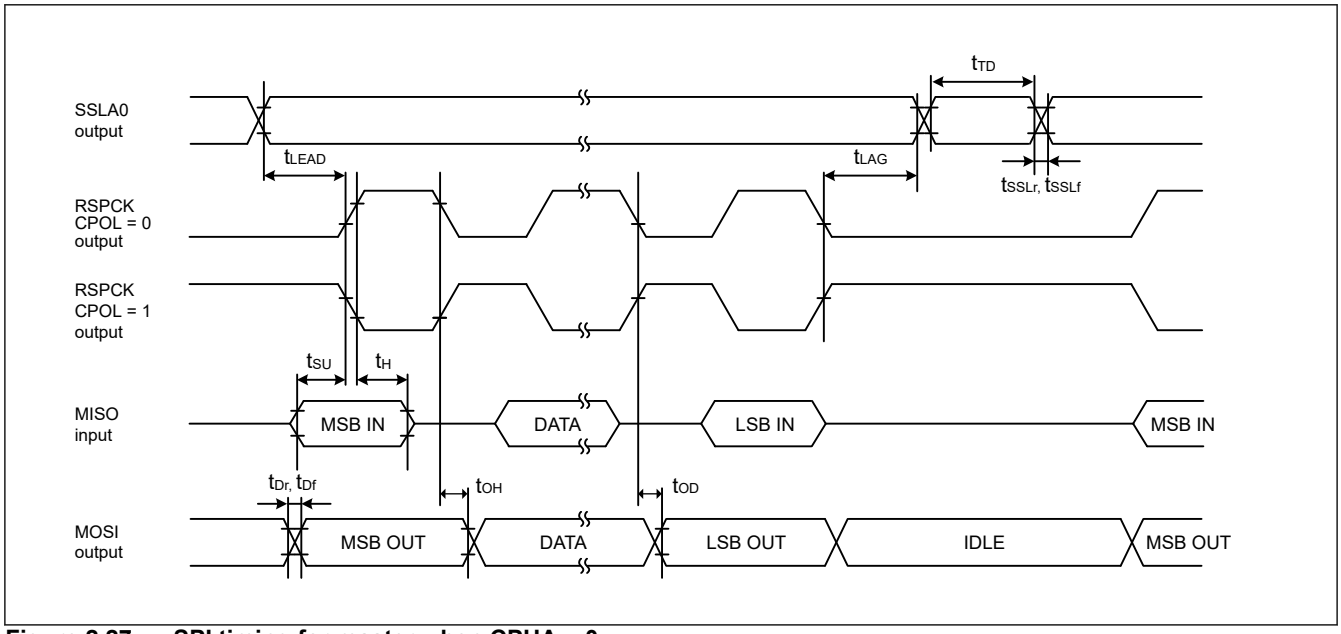


Figure 2.27 SPI timing for master when CPHA = 0

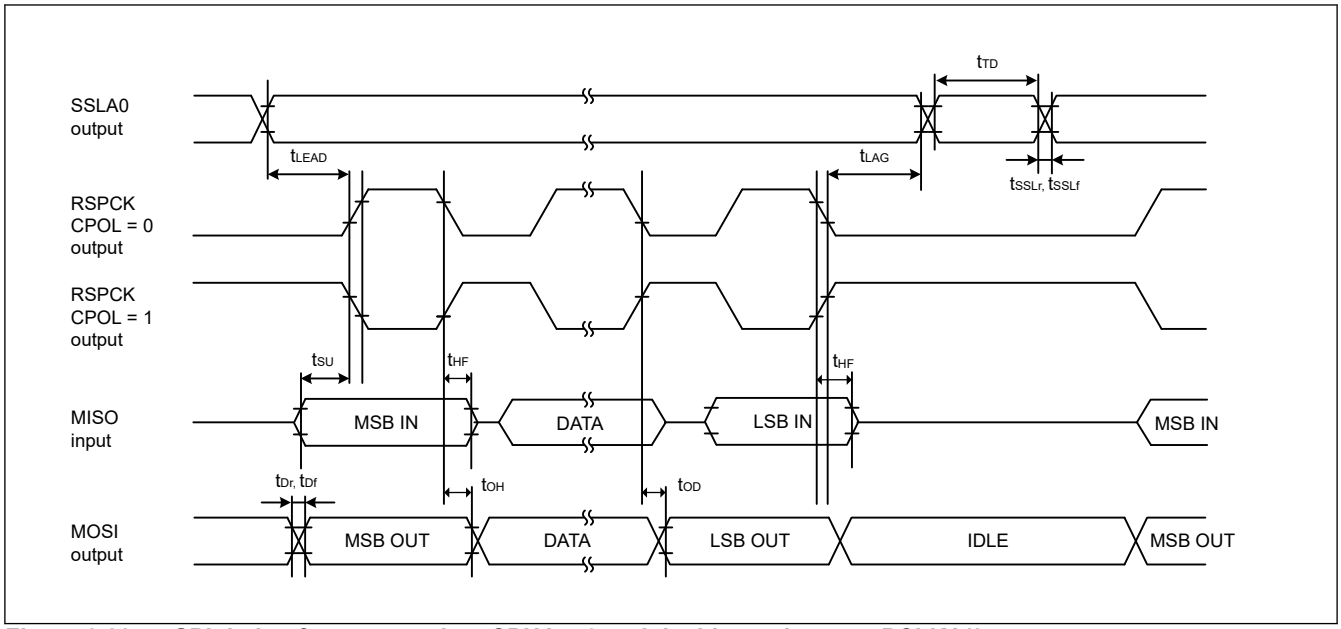


Figure 2.28 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

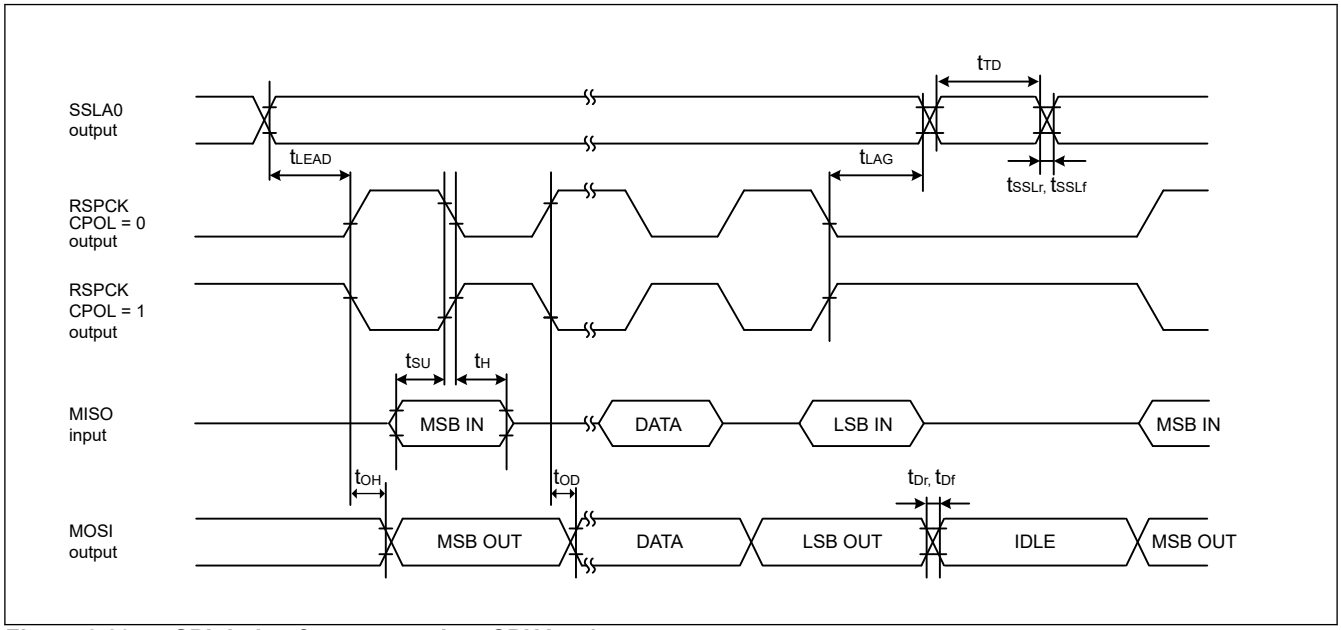


Figure 2.29 SPI timing for master when CPHA = 1

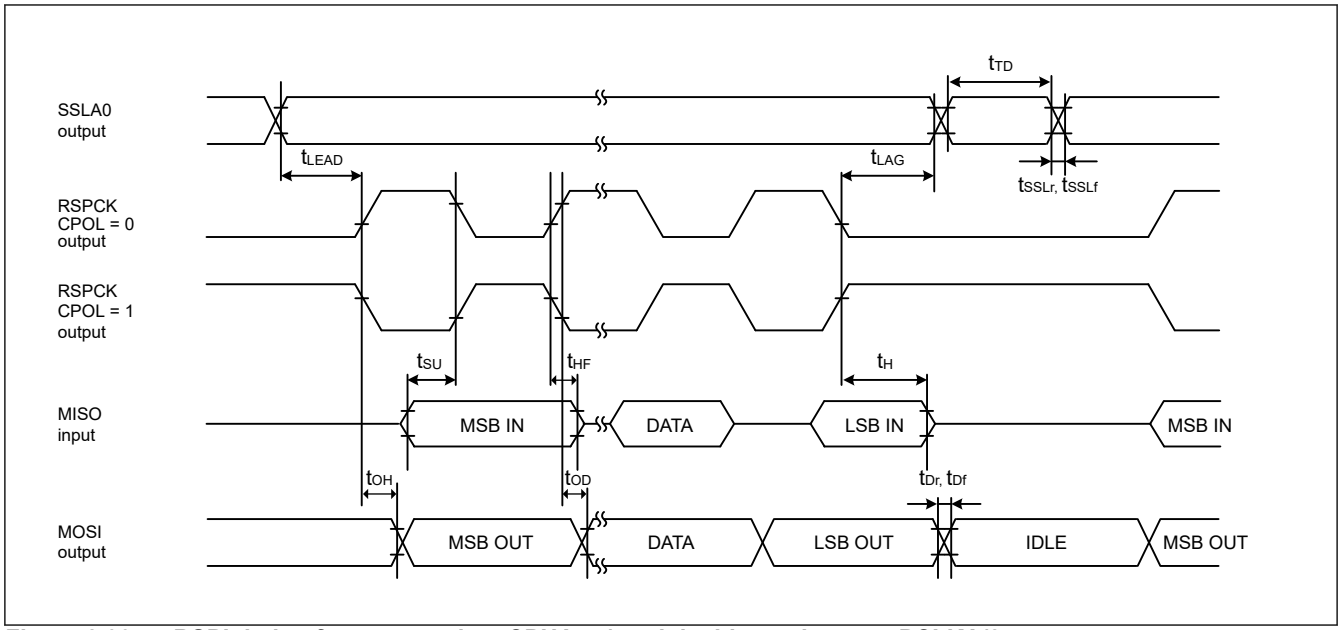


Figure 2.30 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

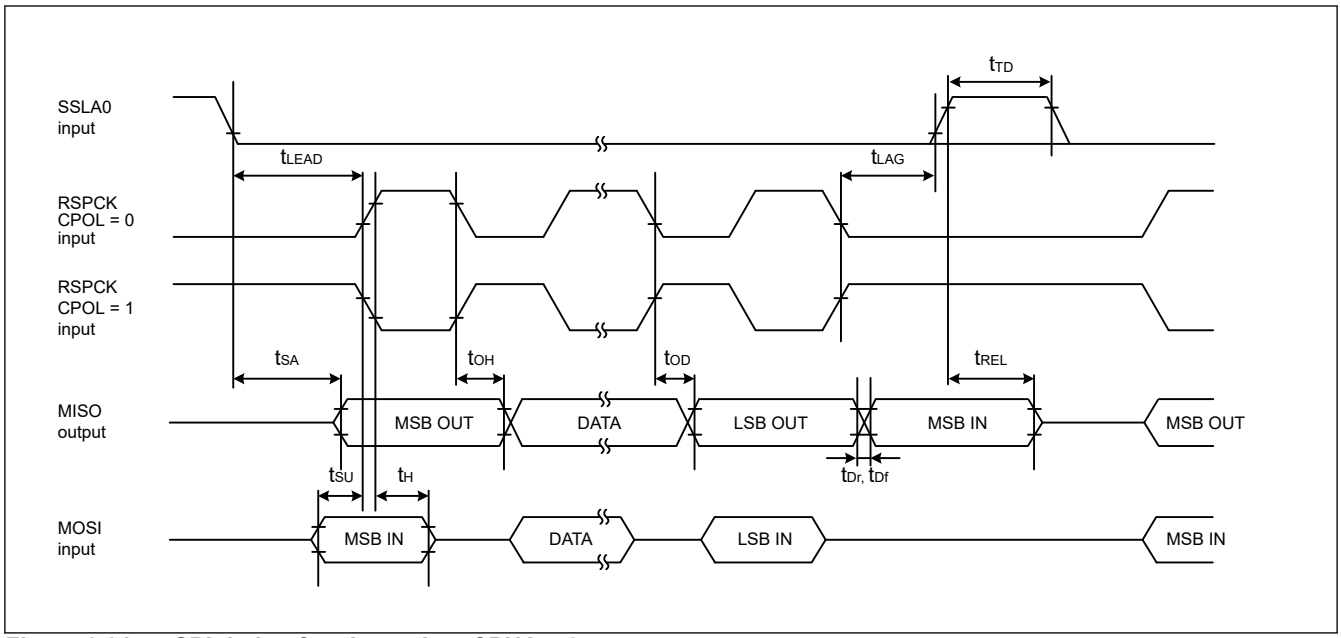


Figure 2.31 SPI timing for slave when CPHA = 0

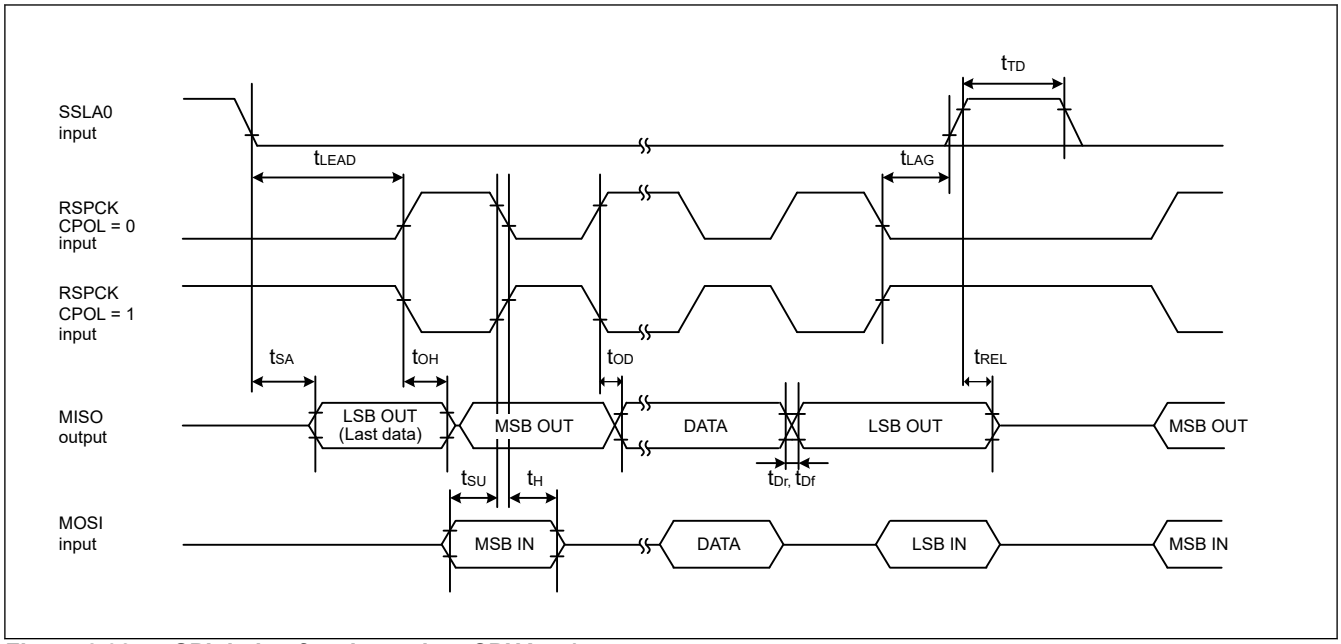


Figure 2.32 SPI timing for slave when CPHA = 1

2.3.10 QSPI Timing

Table 2.24 QSPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.33
	QSPCK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	—	ns	
	QSPCK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	—	ns	
	Data input setup time	t_{Su}	10	—	ns	Figure 2.34
	Data input hold time	t_{IH}	0	—	ns	
	QSSL setup time	t_{LEAD}	(N + 0.5) × t_{Qscyc} - 5*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	QSSL hold time	t_{LAG}	(N + 0.5) × t_{Qscyc} - 5*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	Data output delay	t_{OD}	—	4	ns	
	Data output hold time	t_{OH}	–3.3	—	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set to 0 or 1 in SFMSLD.
Note 2. N is set to 0 or 1 in SFMSHD.

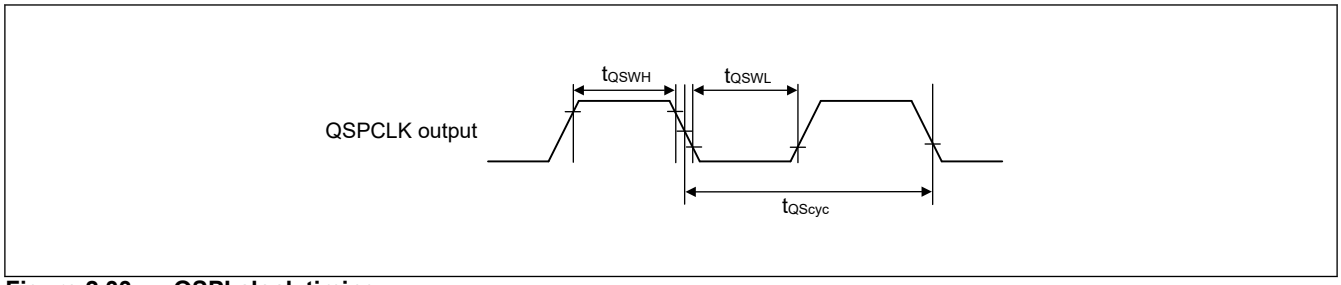


Figure 2.33 QSPI clock timing

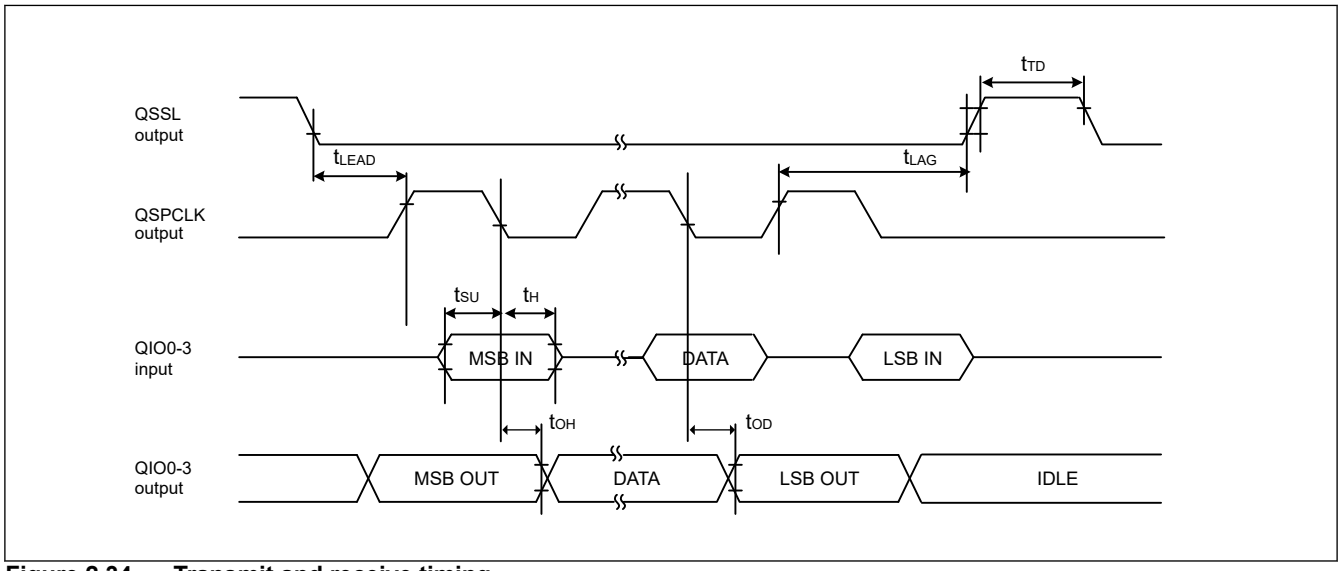


Figure 2.34 Transmit and receive timing

2.3.11 I3C Timing

Specific HDR Modes are not covered by conformance test suite (CTS).

When CTS for HDR Modes is available, Renesas will confirm CTS tests.

Table 2.25 I2C mode timing (1)-1

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA, SCL
AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns
	SCL, SDA rise time	t_{Sr}	—	1000	ns
	SCL, SDA fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	1000	—	ns
	STOP condition input setup time	t_{STOS}	1000	—	ns
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b	—	400	pF

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle
Note: Values in parentheses apply when INCTL.DNFS[1:0] is set to 11b while the digital filter is enabled with INCTR.DNFE set to 1.

Table 2.26 I2C mode timing (1)-2

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA, SCL
AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Fast mode)	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/5.5 V)	300	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 300	—	ns
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	300	—	ns
	STOP condition input setup time	t_{STOS}	300	—	ns
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b	—	400	pF

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle
Note: Values in parentheses apply when INCTL.DNFS[1:0] is set to 11b while the digital filter is enabled with INCTR.DNFE set to 1.

Table 2.27 I2C mode timing (1)-3

Setting of the SCL, SDA pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit
IIC (Fast mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10 (18) × t_{IICcyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	5 (9) × t_{IICcyc}	—	ns
	SCL input low pulse width	t_{SCLL}	5 (9) × t_{IICcyc}	—	ns
	SCL, SDA rise time	t_{Sr}	—	120	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)*1	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns
	SDA input bus free time	t_{BUF}	5 (9) × t_{IICcyc} + 120	—	ns
	START condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns
	Repeated START condition input setup time	t_{STAS}	120	—	ns
	STOP condition input setup time	t_{STOS}	120	—	ns
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	550	pF

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle

Note: Values in parentheses apply when INCTL.DNFS[1:0] is set to 11b while the digital filter is enabled with INCTR.DNFE set to 1.

Note 1. C_b indicates the total capacity of the bus line.

Table 2.28 I2C mode timing (2)

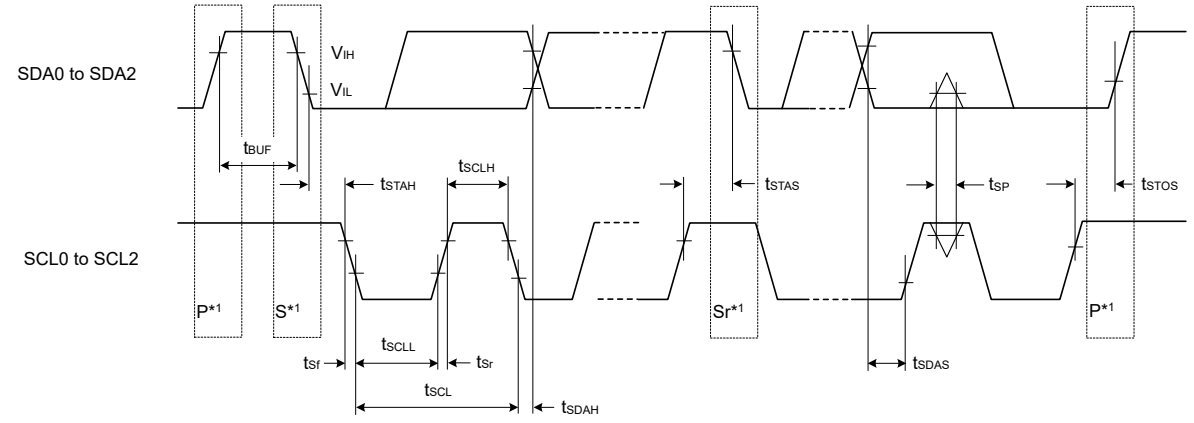
Setting of the SCL, SDA pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit
IIC (Hs mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	10(12) × t_{IICcyc} + 80	—	ns
	SCL input high pulse width		t_{SCLH}	5(6) × t_{IICcyc}	—	ns
	SCL input low pulse width		t_{SCLL}	5(6) × t_{IICcyc}	—	ns
	SCL clock frequency	C_b = 400 pF	f_{SCL}	0	1.7	MHz
		C_b = 100 pF		0	3.4	MHz
	LOW period of the SCL clock	C_b = 400 pF	t_{LOW}	320	—	ns
		C_b = 100 pF		160	—	ns
	HIGH period of the SCL clock	C_b = 400 pF	t_{HIGH}	215	—	ns
		C_b = 100 pF		115	—	ns
	SCL rise time	C_b = 400 pF	t_{SrCL}	—	80	ns
		C_b = 100 pF		—	40	ns
	SDA rise time	C_b = 400 pF	t_{SrDA}	—	160	ns
		C_b = 100 pF		—	80	ns
	SCL fall time	C_b = 400 pF	t_{SfCL}	—	80	ns
		C_b = 100 pF		—	40	ns
	SDA fall time	C_b = 400 pF	t_{SfDA}	—	160	ns
		C_b = 100 pF		—	80	ns
	SCL, SDA input spike pulse removal time		t_{SP}	0	1(1) × t_{IICcyc}	ns
	Repeated START condition input setup time		t_{STAS}	40	—	ns
	STOP condition input setup time		t_{STOS}	40	—	ns
	Data input setup time		t_{SDAS}	10	—	ns
	Data input hold time	C_b = 400 pF	t_{SDAH}	0	150	ns
	Data input hold time	C_b = 100 pF	t_{SDAH}	0	70	ns
	SCL, SDA capacitive load		C_b*1	—	400	pF

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle

Note: Values in parentheses apply when INCTL.DNFS[1:0] is set to 11b while the digital filter is enabled with INCTR.DNFE set to 1.

Note 1. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA (ICFER.FMPE = 0)
V_{OL} = 0.4 V, I_{OL} = 15 mA (ICFER.FMPE = 1)

Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.35 I^2C bus interface input/output timing

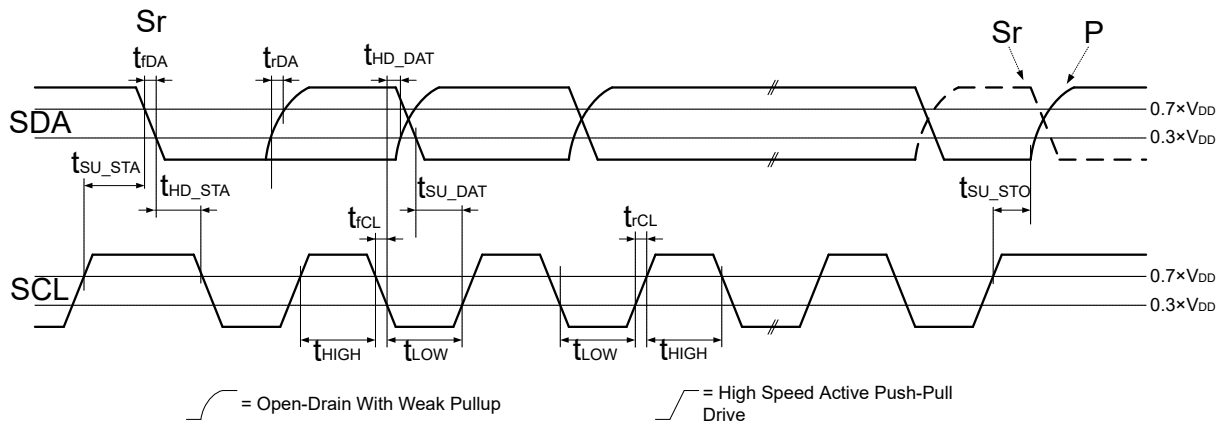


Figure 2.36 I2C bus interface input/output timing (Hs-mode)

Table 2.29 I3C mode timing (Open Drain Timing Parameters) (1 of 2)

Parameter	Symbol	Timing Diagram	Min	Max	Units	Notes
SCL Clock Low Period	t_{LOW_OD}	Figure 2.39	55	—	ns	*1, *2
	$t_{DIG\_OD\_L}$	Figure 2.39	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	—
SCL Clock High Period	t_{HIGH}	Figure 2.37	—	41	ns	*3, *4
	t_{DIG_H}	Figure 2.37	—	t_{HIGH} + t_{CF}	ns	—
		Figure 2.36				

Table 2.29 I3C mode timing (Open Drain Timing Parameters) (2 of 2)

Parameter	Symbol	Timing Diagram	Min	Max	Units	Notes
SDA Signal Fall Time	t_{fDA_OD}	Figure 2.39	—	12	ns	—
SDA Data Setup Time Open Drain Mode	t_{SU_OD}	Figure 2.38 Figure 2.39	17	—	ns	*1
Clock After START (S) Condition	t_{CAS}	Figure 2.39	38.4 nano	For ENAS0: 1 µ For ENAS1: 100 µ For ENAS2: 2 milli For ENAS3: 50 milli	seconds	*5, *6
Clock Before STOP (P) Condition	t_{CBP}	Figure 2.40	t_{CASmin} / 2	—	seconds	—
Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	Figure 2.46	$t_{DIG\_OD\_Lmin}$	—	ns	—
Bus Available Condition	t_{AVAL}	—	1	—	µs	*7
Bus Idle Condition	t_{IDLE}	—	1	—	ms	—
Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	Figure 2.46	$t_{AVALmin}$	—	µs	—

Note 1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_ODmin}$
Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above V_{IH}
Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect
Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I2C Devices, and/or in consideration of the interconnect (e.g., a short Bus).
Note 5. On a Legacy Bus where I2C Devices need to see Start
Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
Note 7. On a Mixed Bus with Fm Legacy I2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Specific HDR Modes are not covered by conformance test suite (CTS).

When CTS for HDR Modes is available, Renesas will confirm CTS tests.

Table 2.30 I3C mode timing (Push-Pull Timing Parameters for SDR and HDR-DDR Modes) (1 of 2)

Parameter	Symbol	Timing Diagram	Min	Typ	Max	Units	Notes
SCL Clock Frequency	f_{SCL}	—	0.01	—	12.5	MHz	*1
SCL Clock Low Period	t_{LOW}	Figure 2.36	24	—	—	ns	—
	t_{DIG_L}	Figure 2.37	35	—	—	ns	*2, *4
SCL Clock High Period for Mixed Bus	t_{HIGH_MIXED}	Figure 2.37	24	—	—	ns	—
	$t_{DIG\_H\_MIXED}$	Figure 2.37	35	—	45	ns	*2, *3
SCL Clock High Period	t_{HIGH}	Figure 2.36	24	—	—	ns	—
	t_{DIG_H}	Figure 2.37 Figure 2.36	35	—	—	ns	*2
Clock in to Data Out for Slave	t_{SCO}	Figure 2.42	—	—	9.7	ns	—
SCL Clock Rise Time	t_{CR}	Figure 2.36	—	—	150 * 1 /f_{SCL} (capped at 60)	ns	—
SCL Clock Fall Time	t_{CF}	Figure 2.36	—	—	150 * 1 /f_{SCL} (capped at 60)	ns	—

Table 2.30 I3C mode timing (Push-Pull Timing Parameters for SDR and HDR-DDR Modes) (2 of 2)

Parameter		Symbol	Timing Diagram	Min	Typ	Max	Units	Notes
SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP}	Figure 2.41	t_{CR} + 3 and t_{CF} + 3	—	—	—	*4
	Slave	t_{HD_PP}	Figure 2.43 Figure 2.44	0	—	—	—	—
SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	Figure 2.41 Figure 2.42	17	—	N/A	ns	—
Clock After Repeated START (Sr)		t_{CASr}	Figure 2.45	t_{CASmin}	—	N/A	ns	—
Clock Before Repeated START (Sr)		t_{CBSr}	Figure 2.45	t_{CASmin} / 2	—	N/A	ns	—
Capacitive Load per Bus Line (SDA/SCL)		C_b	—	—	—	50	pF	—

Note 1. FSCL = 1 / (t_{DIG_L} + t_{DIG_H})

Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}. (see Figure 2.36)

Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I2C Devices do not interpret I3C signaling as valid I2C signaling.

Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

Table 2.31 I3C mode timing (Push-Pull Timing Parameters for HDR-TSP and HDR-TSL Modes)

Parameter	Symbol	Timig Diagram	Min	Typ	Max	Units	Notes
Edge-to-Edge Period	t_{EDGE}	Figure 2.47	t_{DIG_H}	—	—	ns	*1, *2
Allowed Difference Between Signals for Simultaneous Change	t_{SKEW}	Figure 2.47	—	—	9	ns	—
Stable Condition Between Symbols	t_{EYE}	Figure 2.47	12	—	—	ns	—
Time Between Successive Symbols	t_{SYMBOL}	Figure 2.47	t_{EDGE} Min	—	—	ns	—

Note 1. Edges occur at the rate of 1 / (t_{EDGE} * 2)

Note 2. In a Mixed Bus, HDR-TSL shall respect the maximum $t_{DIG\_H\_MIXED}$ shown in Table 2.30.

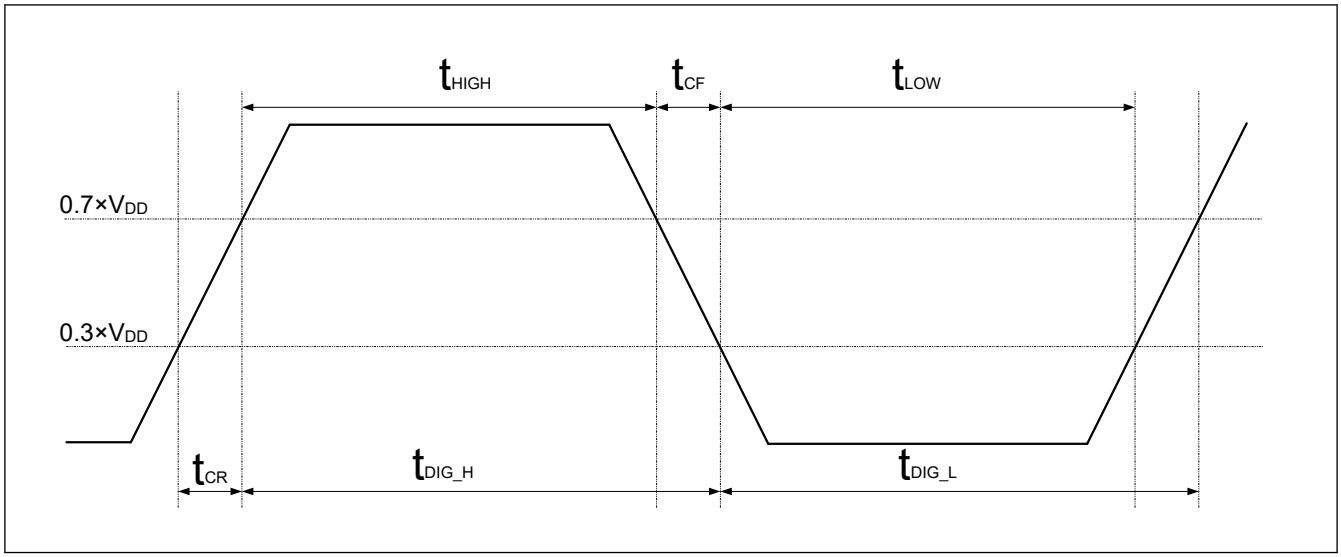
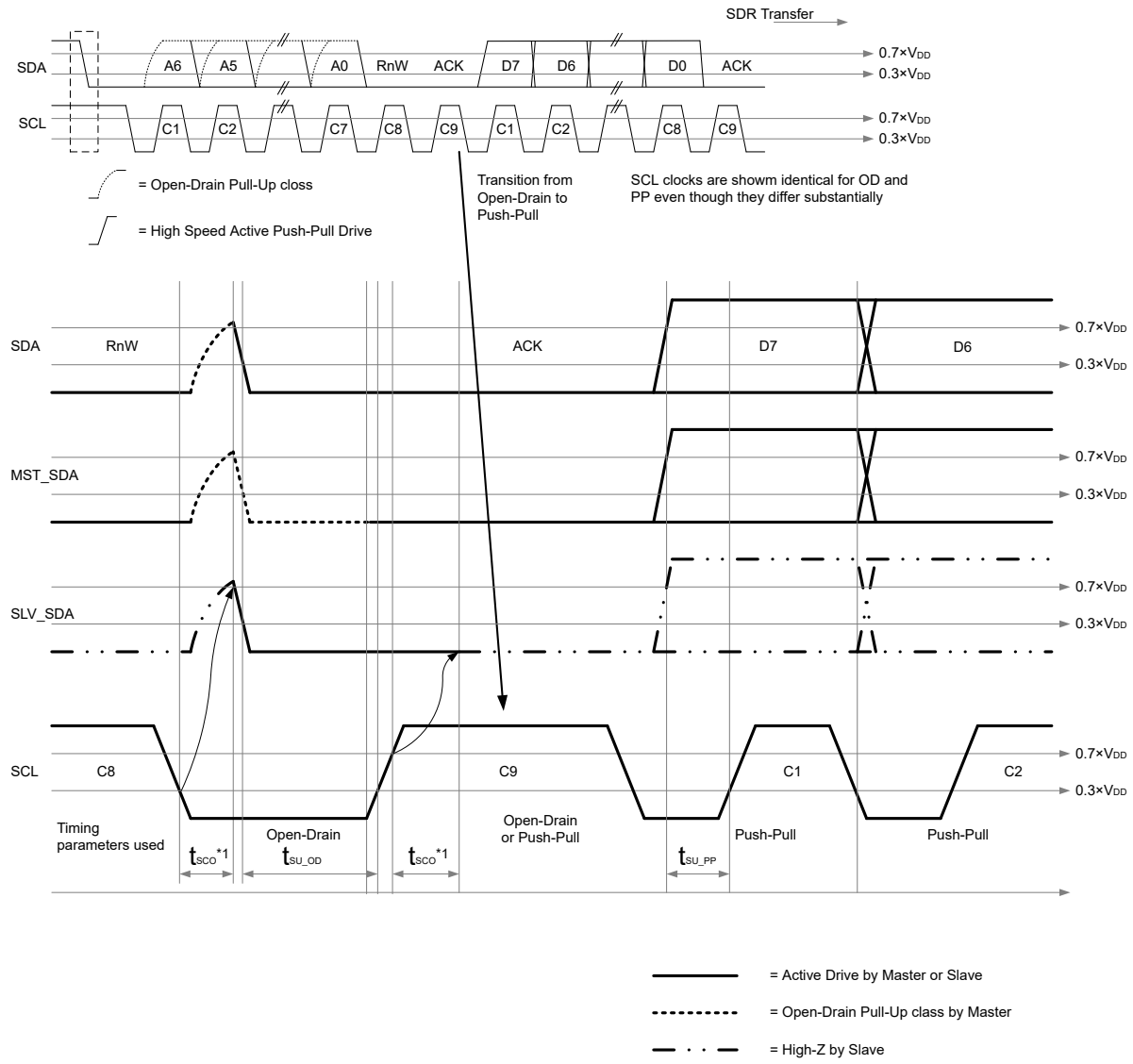


Figure 2.37 t_{DIG_H} and t_{DIG_L}



Note: Open-Drain: Master releases SDA after a suitable delay from SCL edges
Push-Pull: Master drives SDA after a suitable delay from SCL edges
Note 1. t_{SCO} is depicted for informative purposes only

Figure 2.38 I3C Data Transfer–ACK by Slave

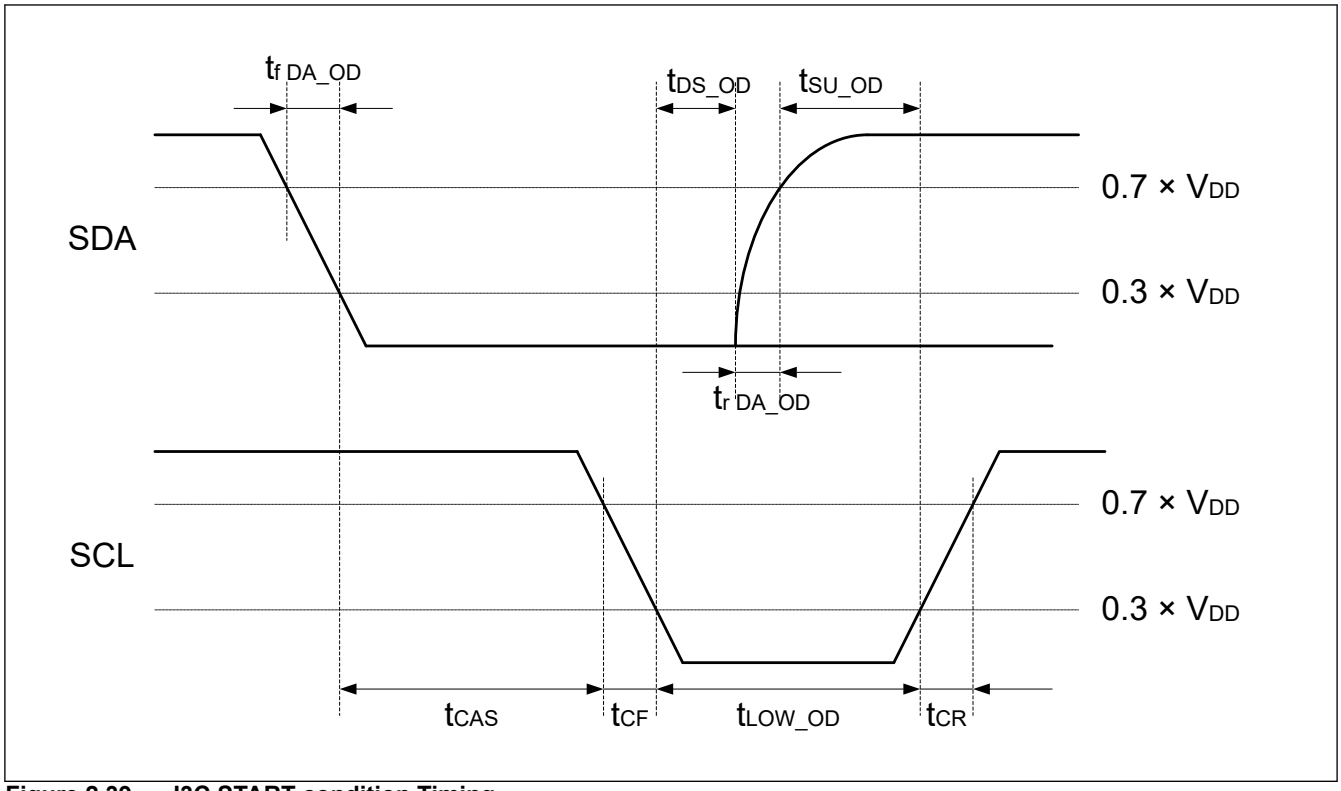


Figure 2.39 I3C START condition Timing

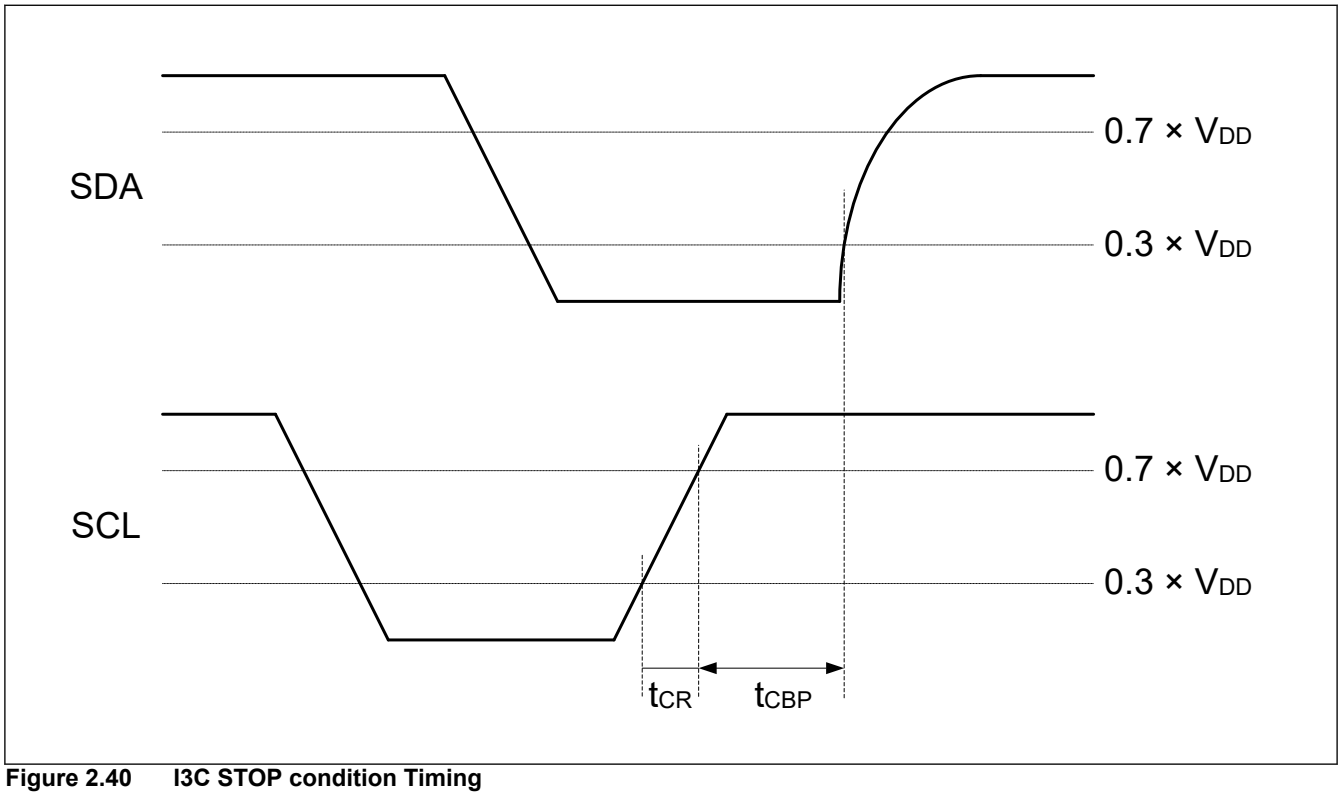


Figure 2.40 I3C STOP condition Timing

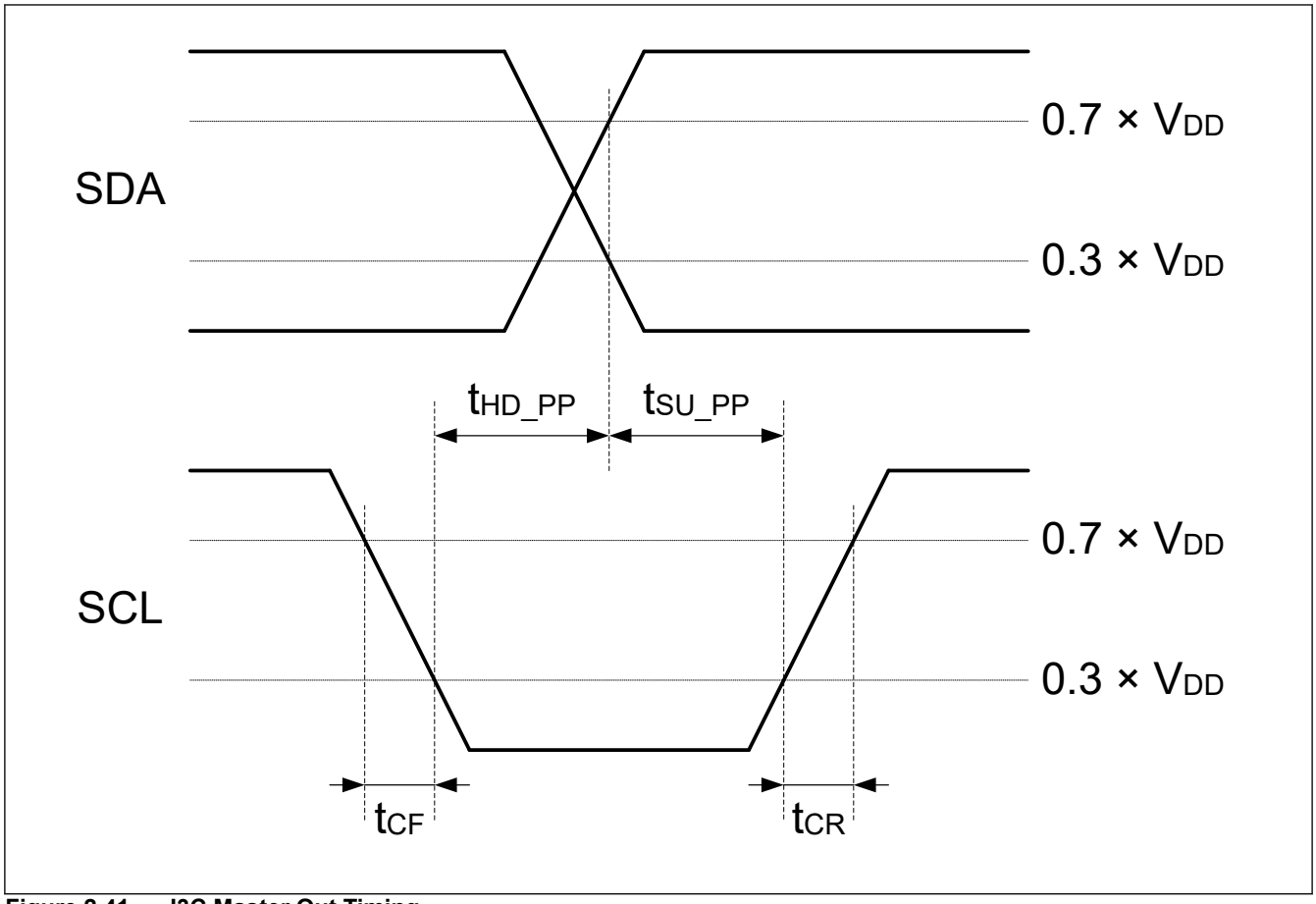


Figure 2.41 I3C Master Out Timing

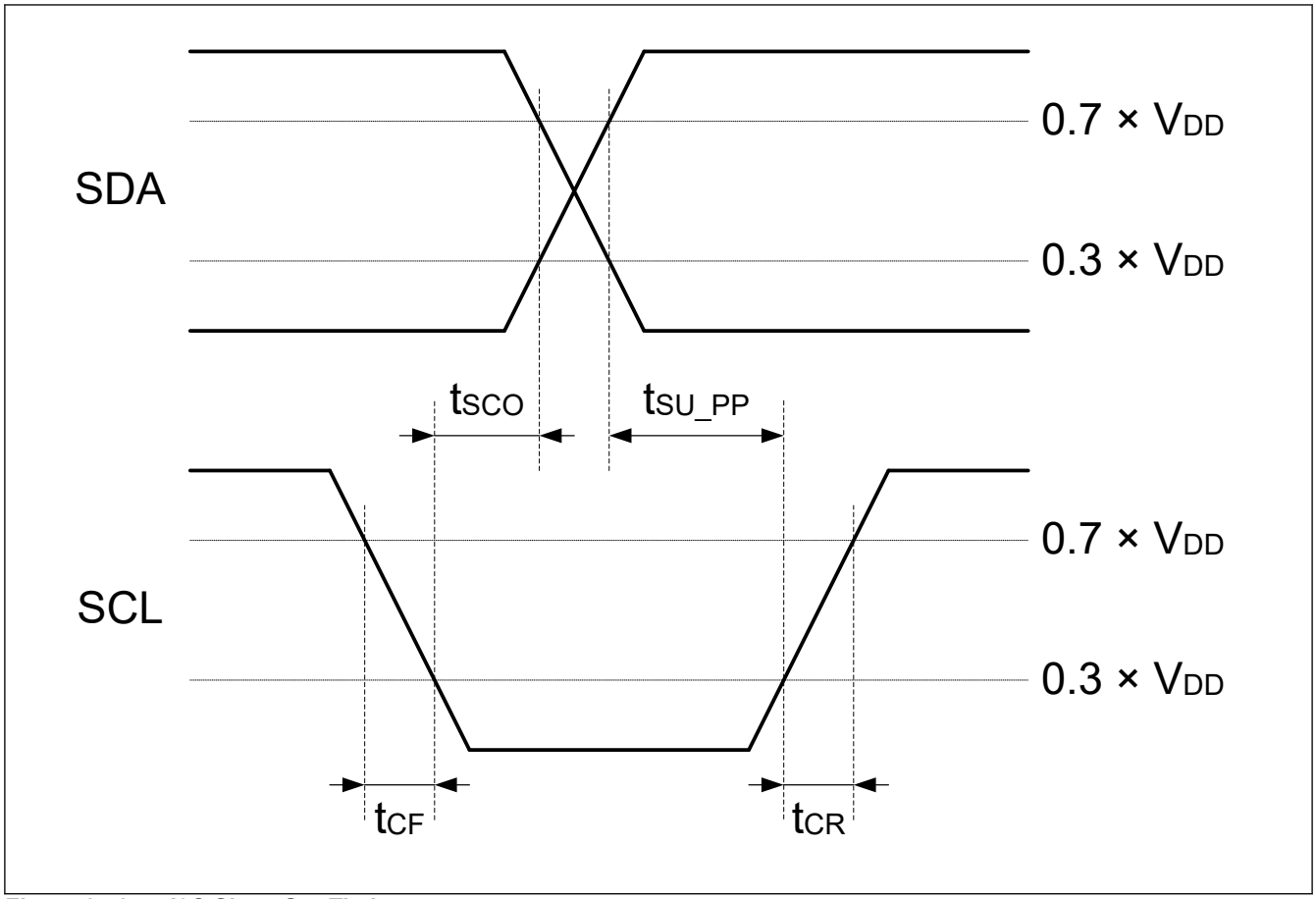


Figure 2.42 I3C Slave Out Timing

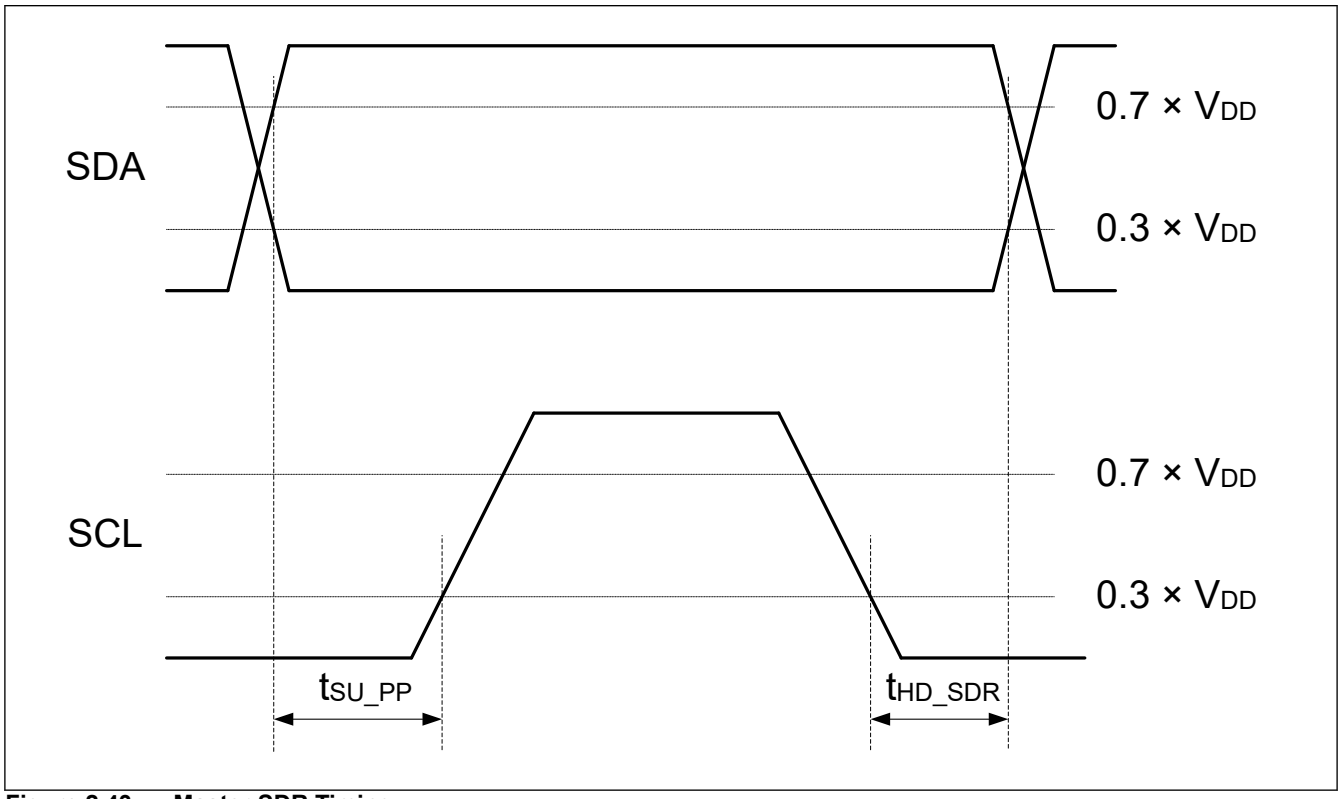


Figure 2.43 Master SDR Timing

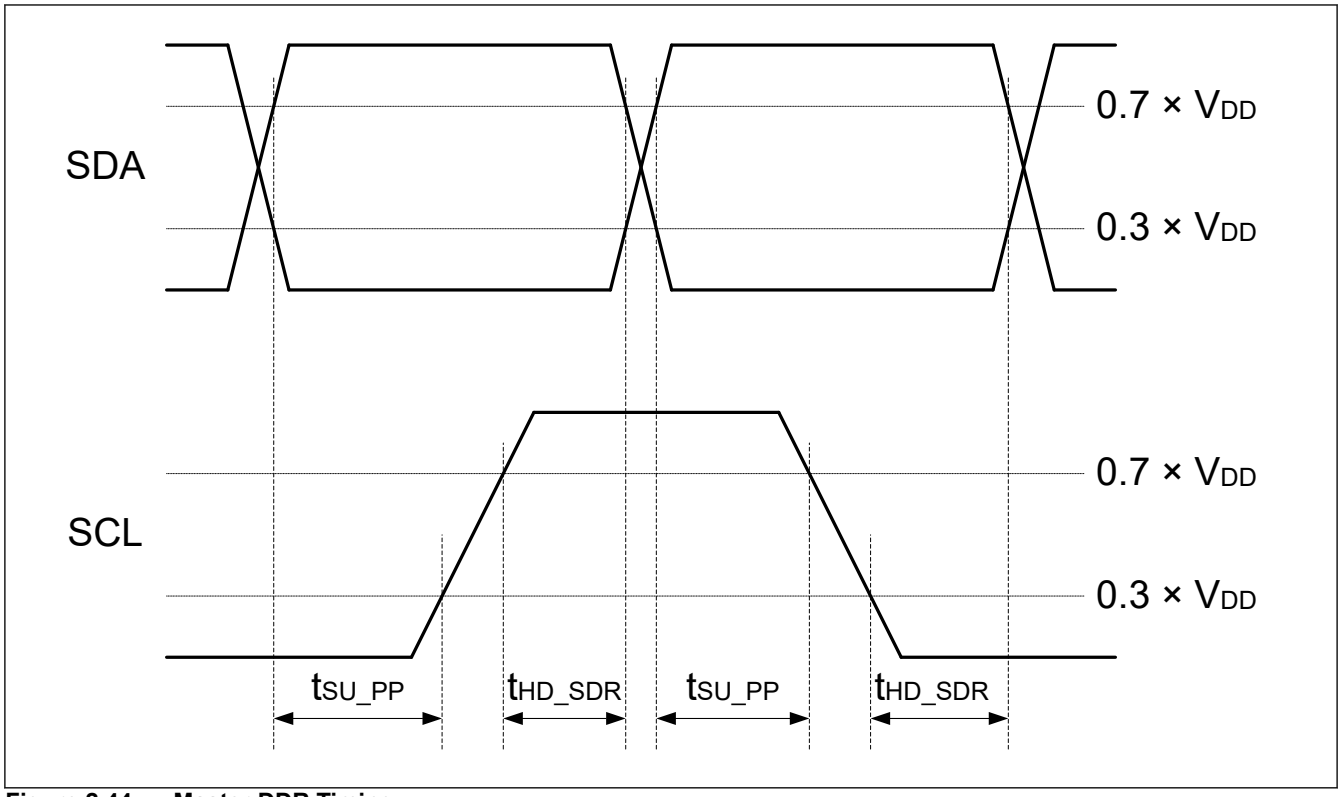
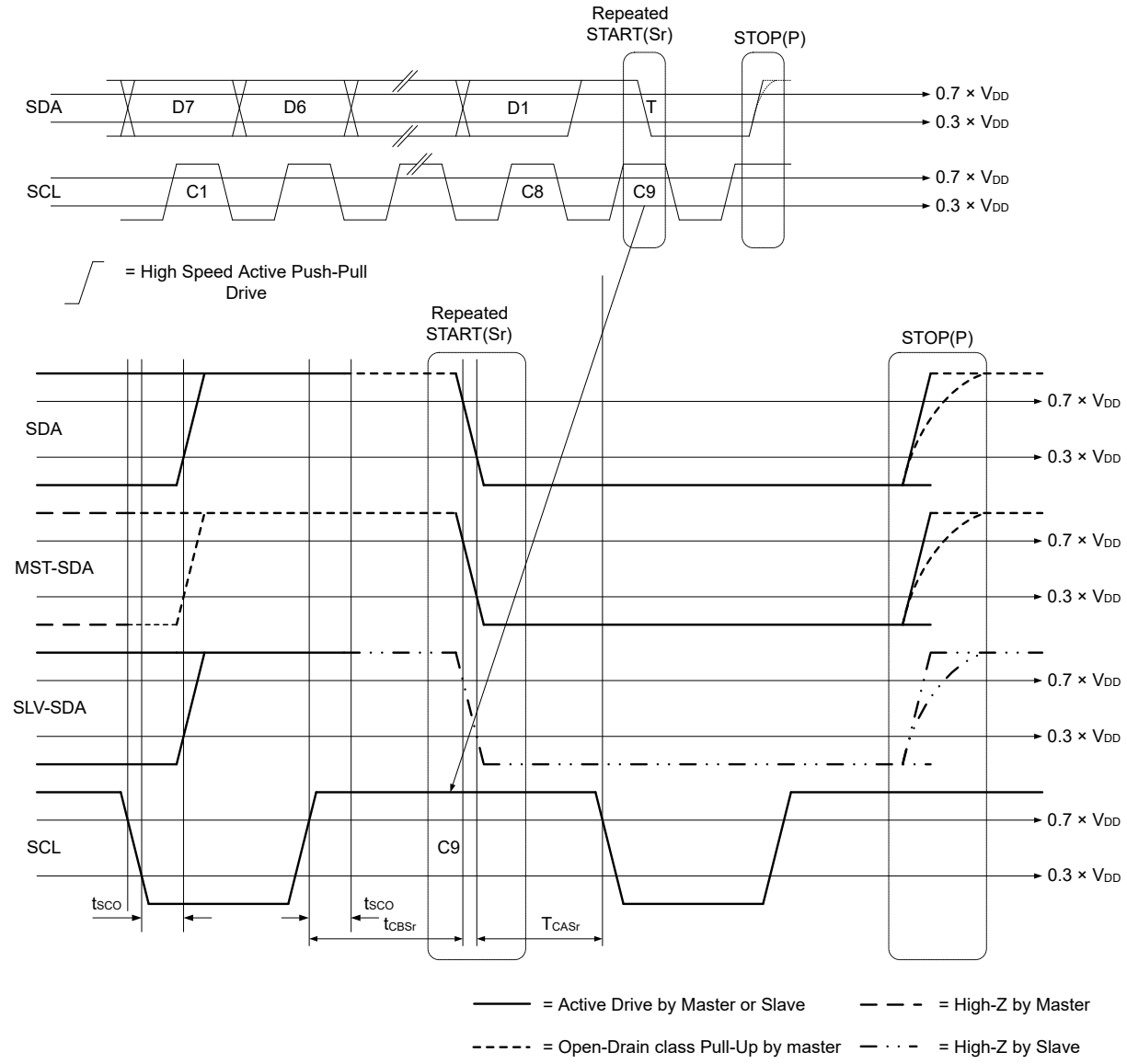
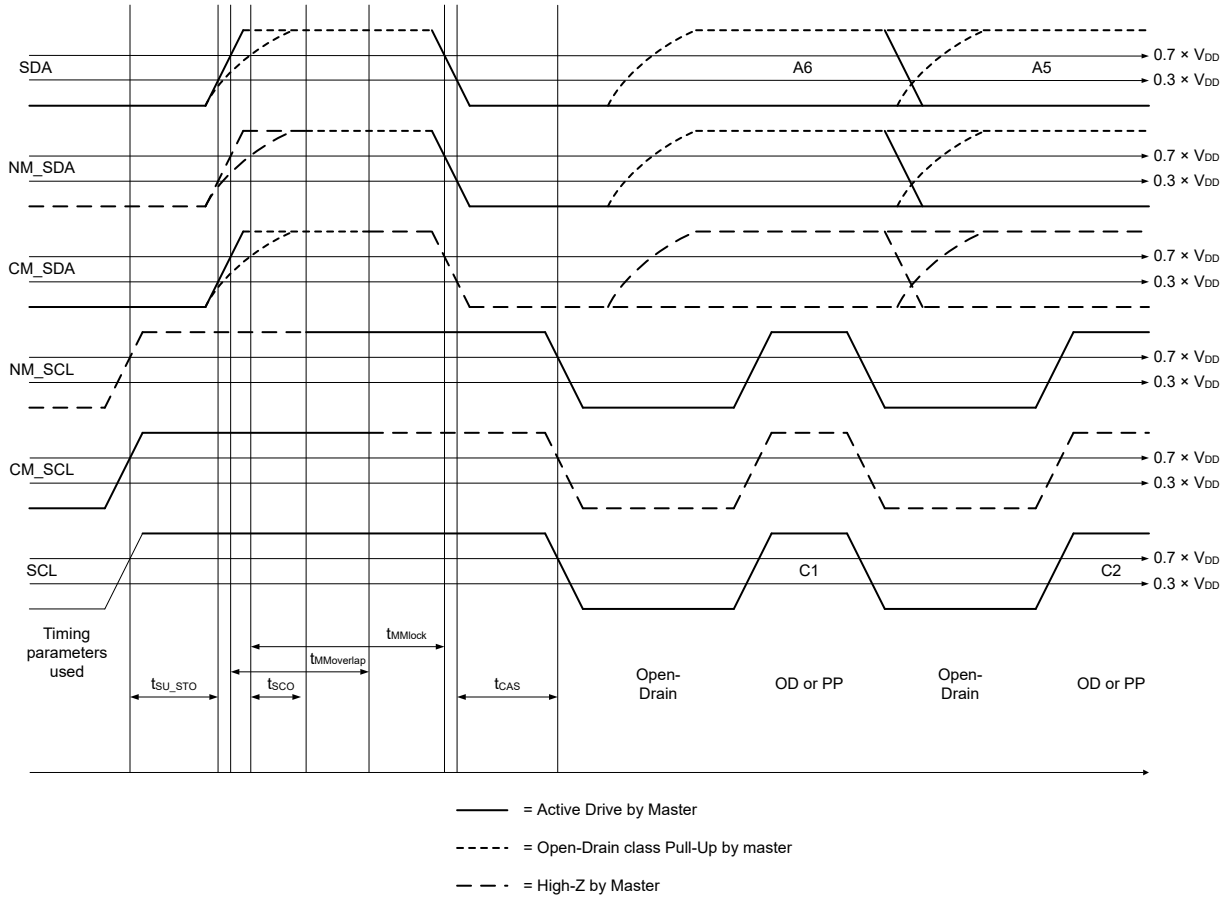


Figure 2.44 Master DDR Timing



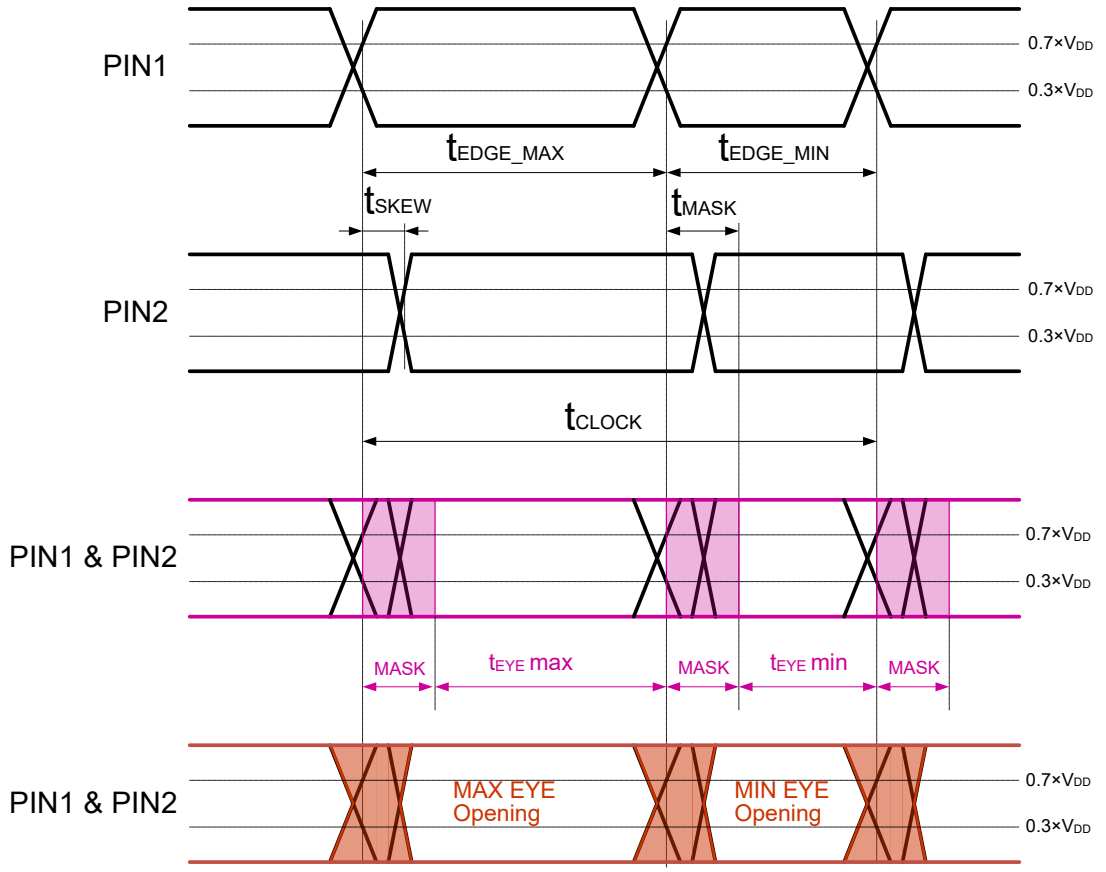
Note: Sr immediately followed by P is illegal for I2C devices, however many devices are not adversely affected by it.The condition is not illegal for I3C devices

Figure 2.45 T-Bit When Master Ends Read with Repeated START and STOP



Note: Master releases or drives SDA after a suitable delay from SCL edges

Figure 2.46 I3C IP Timing (1)



Design Conditions

1. The The differences of load magnitude and drive strength between the SDA and SCL lines result in different slopes, as shown
2. MASK period ≥ MAX t_{SKEW} + MAX rise/fall time between 0.3 × V_{DD} and 0.7 × V_{DD}, respectively, decreased by the time crossing the hysteresis window.

Simplifying Assumptions

1. t_{SKEW} is the same for both edges
2. Base CLOCK (e.g. 12.5MHz) is asymmetrical
3. Falling edges are equal rising edges
4. The MASK is shown as starting, from the last possible moment, whereas in reality it could be shifted left (towards the start point) delayed by the hysteresis window

Figure 2.47 I3C IP Timing (2)

2.3.12 SSIE Timing

Table 2.32 SSIE timing

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register for SSIBCK1, SSILRCK1/SSIFS1, SSIDATA1, SSIBCK0, SSILRCK0/SSIFS0 pins.
(2) Low drive output is selected with the Port Drive Capability bit in the PmnPFS register for SSIDATA0 pins.

Parameter			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCKn	Cycle	Master	t_O	80	—	ns	Figure 2.48
		Slave	t_I	80	—	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	—	t_O	
		Slave		0.35	—	t_I	
	Rising time/ falling time	Master	t_{RC}/t_{FC}	—	0.15	t_O / t_I	
		Slave		—	0.15	t_O / t_I	
SSILRCKn/ SSIFSn, SSIDATAn	Input set up time	Master	t_{SR}	12	—	ns	Figure 2.50, Figure 2.51
		Slave		12	—	ns	
	Input hold time	Master	t_{HR}	8	—	ns	
		Slave		15	—	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.50, Figure 2.51
	Output delay time from SSILRCKn/ SSIFSn change	Slave	t_{DTRW}	—	20	ns	Figure 2.52*1
GTIOC4A, AUDIO_CLKn	Cycle		t_{EXcyc}	20	—	ns	Figure 2.49
	High level/ low level		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCKn/SSIFSn pin is used to generate transmit data, and the transmit data is logically output to the SSIDATAn pin.

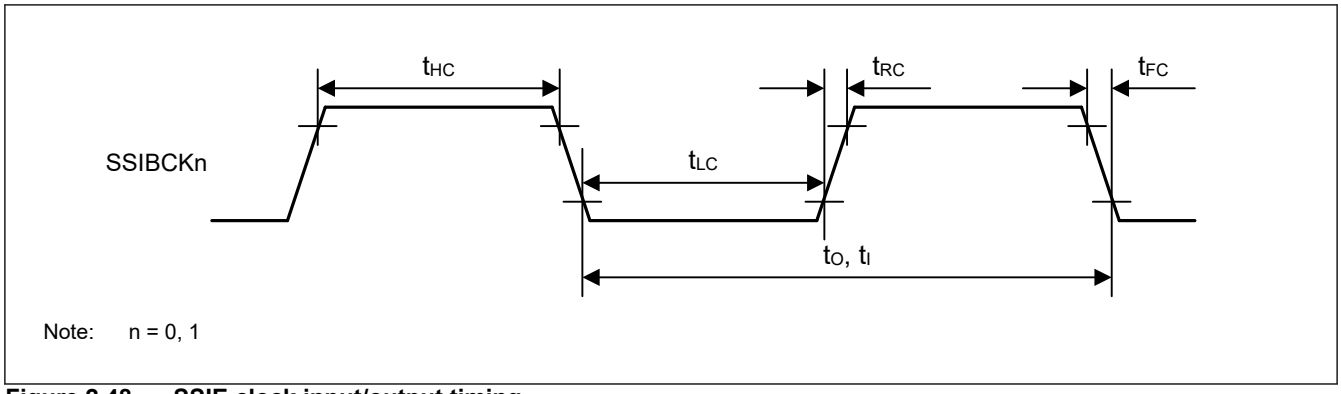
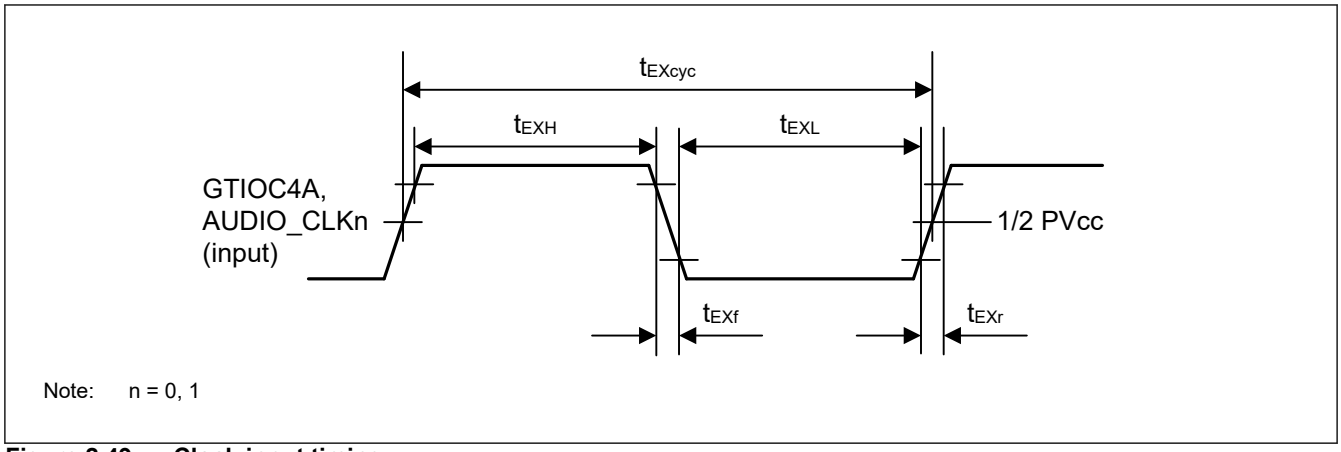
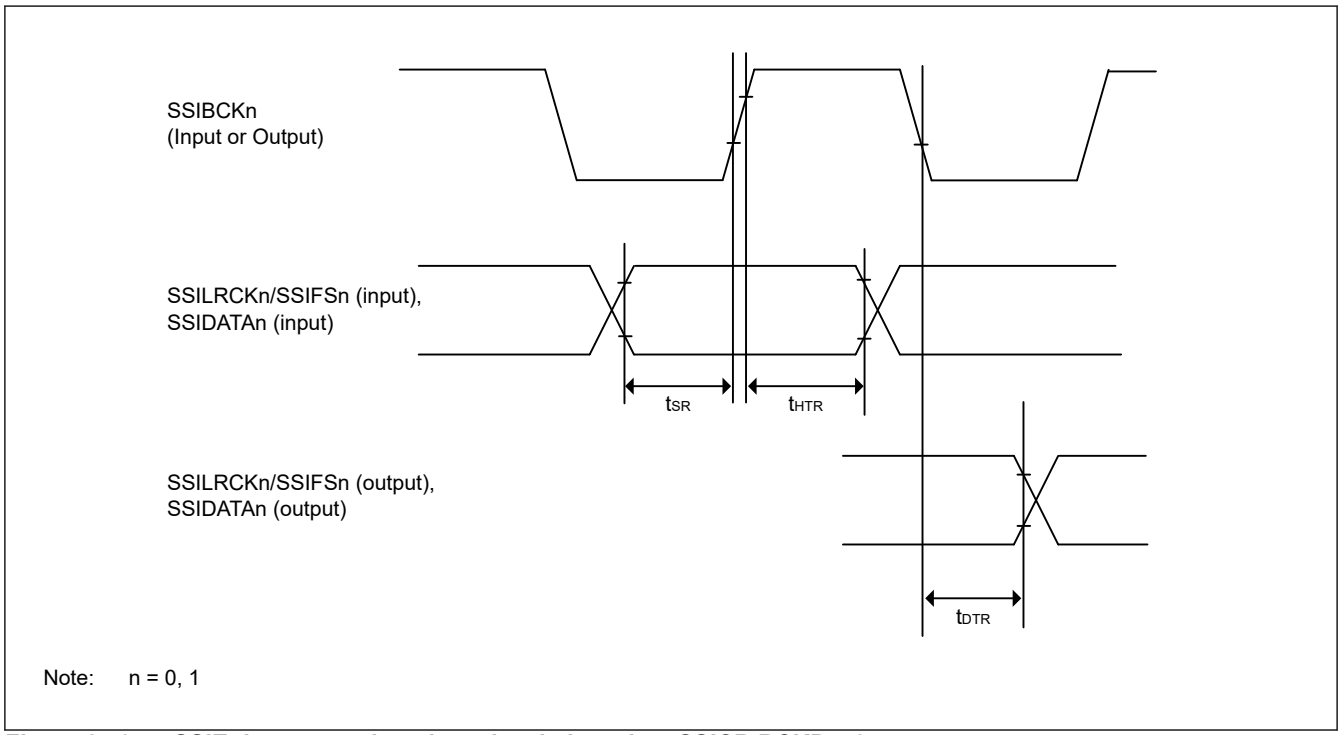


Figure 2.48 SSIE clock input/output timing



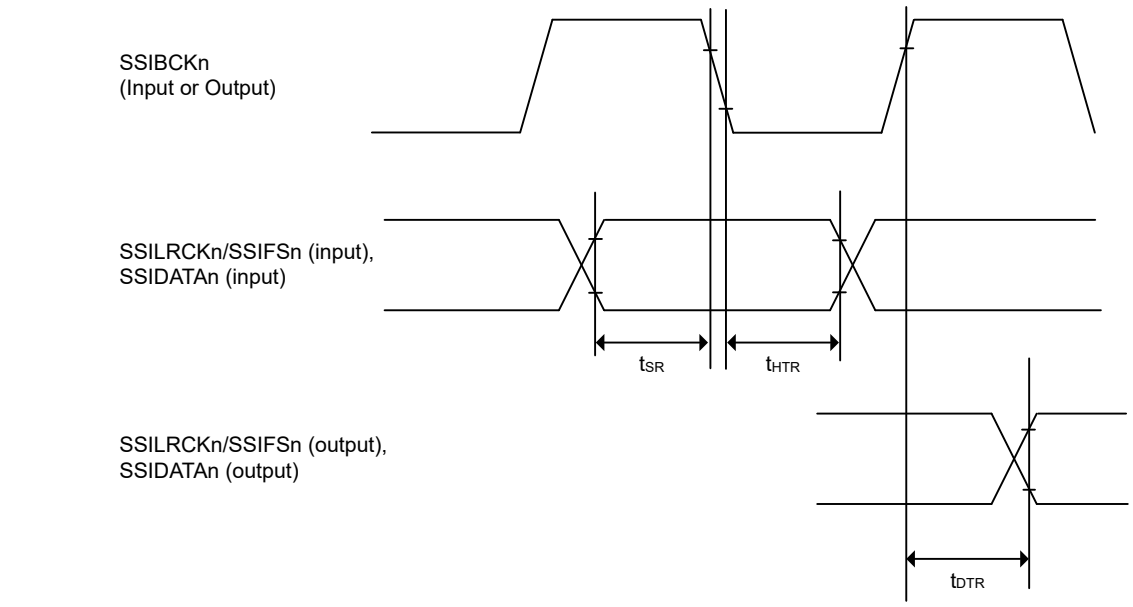
Note: n = 0, 1

Figure 2.49 Clock input timing



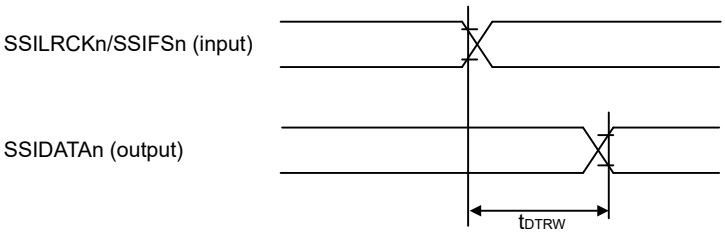
Note: n = 0, 1

Figure 2.50 SSIE data transmit and receive timing when SSICR.BCKP = 0



Note: n = 0, 1

Figure 2.51 SSIE data transmit and receive timing when SSICR.BCKP = 1



MSB bit output delay after SSILRCK0/SSIFS0 change for slave transmitter when DEL = 1, SDTA = 0 or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0] in SSICR.

Note: n = 0, 1

Figure 2.52 SSIE data output delay after SSILRCKn/SSIFSn change

2.3.13 PDM timing

Table 2.33 PDM timing (1 of 2)

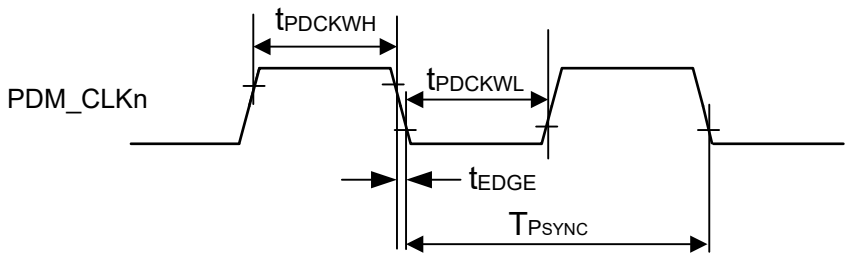
Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: PDM_CLK0, PDM_DATA0
Low drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: PDM_CLK1, PDM_DATA1

No.	Item	Symbol	min	max	Unit	Measurement condition
1	Clock period	T_{Psync}	250	4000	ns	Figure 2.53
2	Clock high level period	t_{PDCKWH}	T_{Psync} × 0.45	T_{Psync} × 0.55	ns	
3	Clock low level period	t_{PDCKWL}	T_{Psync} × 0.45	T_{Psync} × 0.55	ns	
4	Clock rise/fall time (High drive)	t_{EDGE}	—	3	ns	
5	Clock rise/fall time (Low drive)	t_{EDGE}	—	7	ns	

Table 2.33 PDM timing (2 of 2)

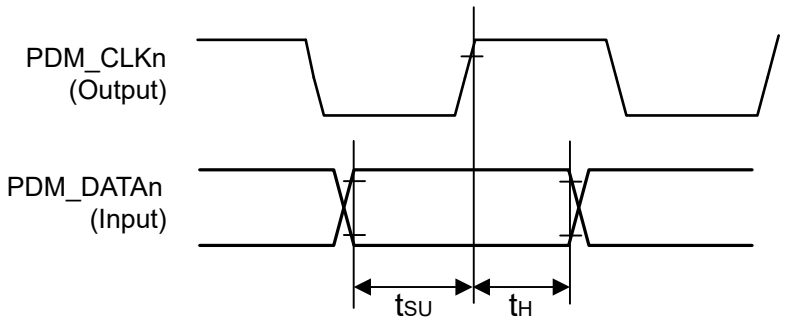
Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: PDM_CLK0, PDM_DATA0
Low drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: PDM_CLK1, PDM_DATA1

No.	Item	Symbol	min	max	Unit	Measurement condition
6	Setup time	t_{SU}	15	—	ns	Figure 2.54 Figure 2.55
7	Hold time	t_H	0	—	ns	



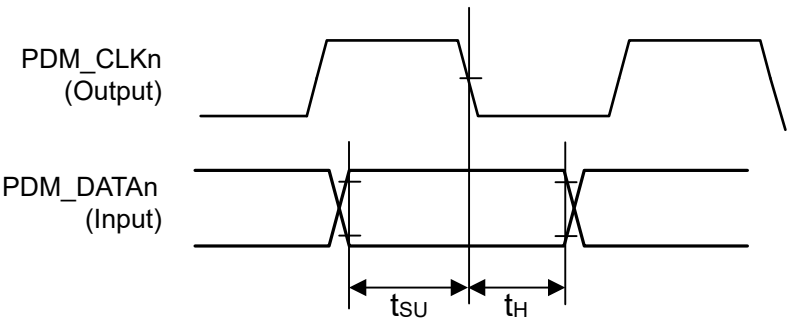
Note: n = 0, 1

Figure 2.53 Timing of clock output (PDM_CLKn)



Note: n = 0, 1

Figure 2.54 Receive Timing (Synchronized with the rise of PDM_CLKn)



Note: n = 0, 1

Figure 2.55 Receive Timing (Synchronized with the fall of PDM_CLKn)

2.4 ADC12 Characteristics

Table 2.34 A/D conversion characteristics for unit 0

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
High-precision high-speed channels Channel-dedicated sample-and-hold circuits in use (AN000, AN001)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.12 (0.4 + 0.26)*2	—	—	µs	• Sampling of channelded icated sample-and-hold circuits in 20 states • Sampling in 13 states
	Offset error		—	±2.5	±5	LSB	AN000, AN001 = 0.25 V
	Full-scale error		—	±2.5	±4	LSB	AN000, AN001 = VREFH - 0.25 V
	Absolute accuracy		—	±3.5	±7	LSB	—
	DNL differential nonlinearity error		—	±1.5	±2.3	LSB	—
	INL integral nonlinearity error		—	±1.5	±3.5	LSB	—
	Holding characteristics of sample-and hold circuits		—	—	20	µs	—
	Dynamic range		0.25	—	VREFH - 0.25	V	—
High-precision high-speed channels Channel-dedicated sample-and-hold circuits not in use (AN000 to AN003)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	µs	Sampling in 13 states
		Permissible signal source impedance Max. = 400 Ω	0.40 (0.14)*2	—	—	µs	Sampling in 7states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤AVCC0
	Offset error		—	±2.0	±4.0	LSB	—
	Full-scale error		—	±2.0	±3.0	LSB	—
	Absolute accuracy		—	±2.5	±6.0	LSB	—
	DNL differential nonlinearity error		—	±1.0	±1.8	LSB	—
	INL integral nonlinearity error		—	±1.0	±3.0	LSB	—
Normal-precision channels (AN016, AN017)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±2.0	±7.0	LSB	—
	Full-scale error		—	±2.0	±6.0	LSB	—
	Absolute accuracy		—	±2.5	±9.0	LSB	—
	DNL differential nonlinearity error		—	±1.0	±4.8	LSB	—
	INL integral nonlinearity error		—	±1.0	±6.0	LSB	—

Note: The characteristics apply when pin functions other than 12-bit A/D converter input are not used or when P/E is not performed in FLASH. If other pin functions are used or P/E is performed during AD conversion,values might not fall within the specified ranges. The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH, VREFL, and 12-bit A/D converter input voltage are stable.

Note: AVCC, AVSS and VREFL pin does not exist in QFN32/24.
ADC power is supplied from VCC.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.35 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	—
Sampling time	4.15	—	—	µs	—

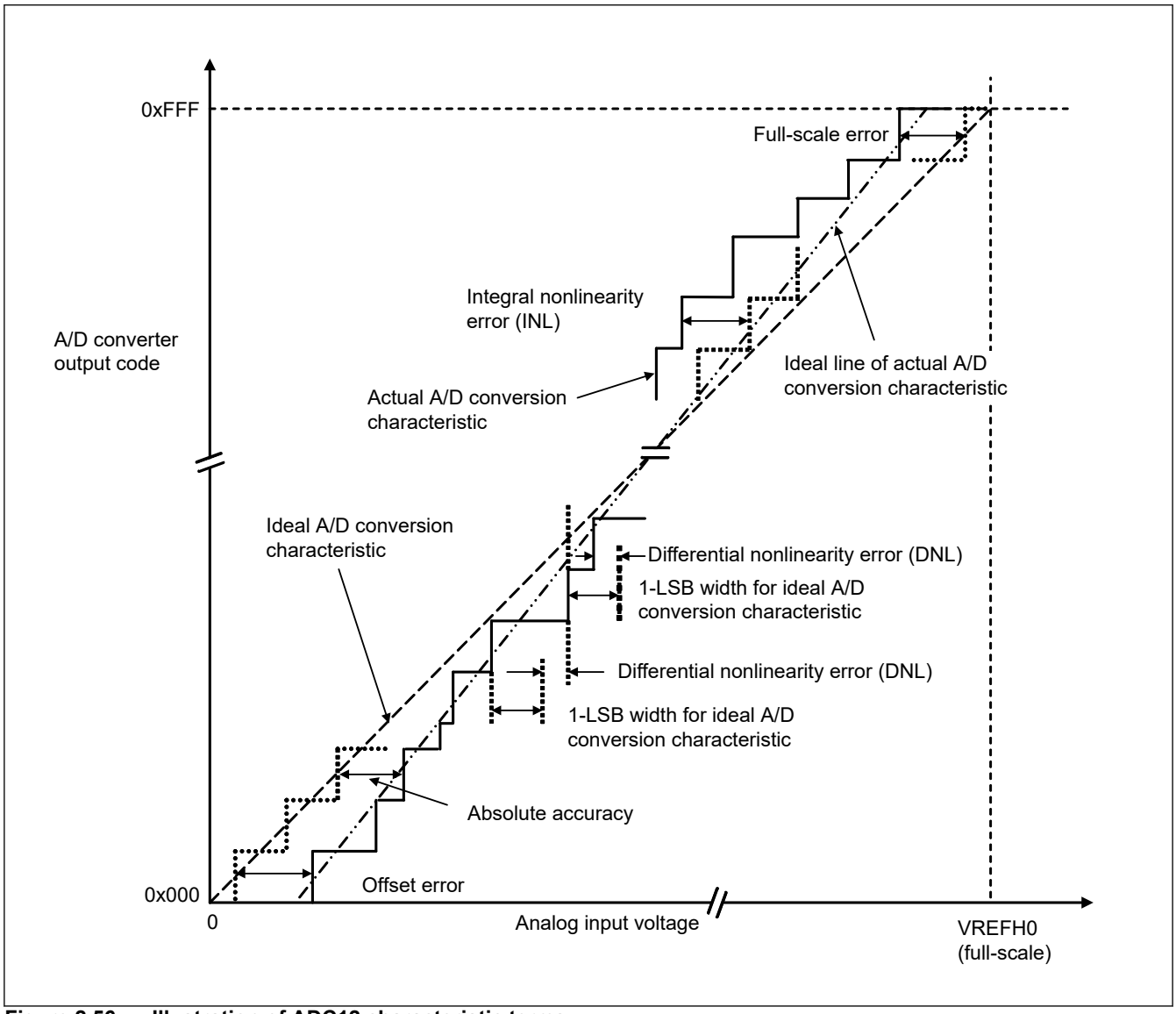


Figure 2.56 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D

conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 DAC12 Characteristics

Table 2.36 D/A conversion characteristics for QFN-48

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±25	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	AVCC	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	AVCC - 0.2	V	—

Table 2.37 D/A conversion characteristics for QFN-32 and QFN-24 (1 of 2)

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±27.5	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	VCC	V	—
With output amplifier					

Table 2.37 D/A conversion characteristics for QFN-32 and QFN-24 (2 of 2)

Parameter	Min	Typ	Max	Unit	Test conditions
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	VCC - 0.2	V	—

2.6 TSN Characteristics

Table 2.38 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	±1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.20	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

2.7 OSC Stop Detect Characteristics

Table 2.39 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.57

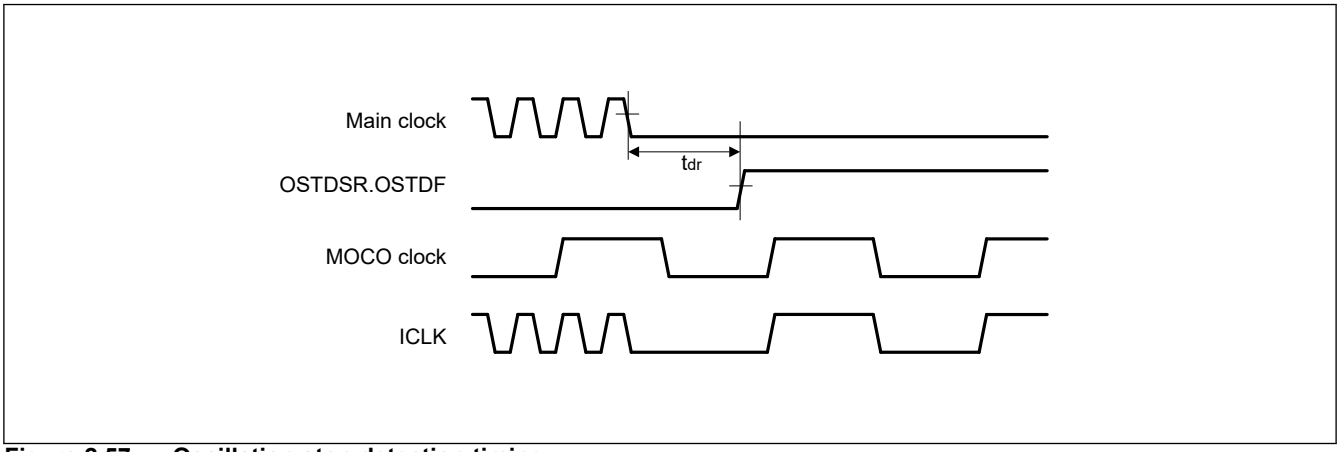


Figure 2.57 Oscillation stop detection timing

2.8 POR and LVD Characteristics

Table 2.40 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 2.58
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.59
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.60
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.61
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 2.58
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 2.59
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 2.60
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 2.61
Minimum VCC down time*1			t_{VOFF}	200	—	—	µs	Figure 2.58, Figure 2.59
Response delay			t_{det}	—	—	200	µs	Figure 2.59 to Figure 2.61
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	µs	Figure 2.60, Figure 2.61
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

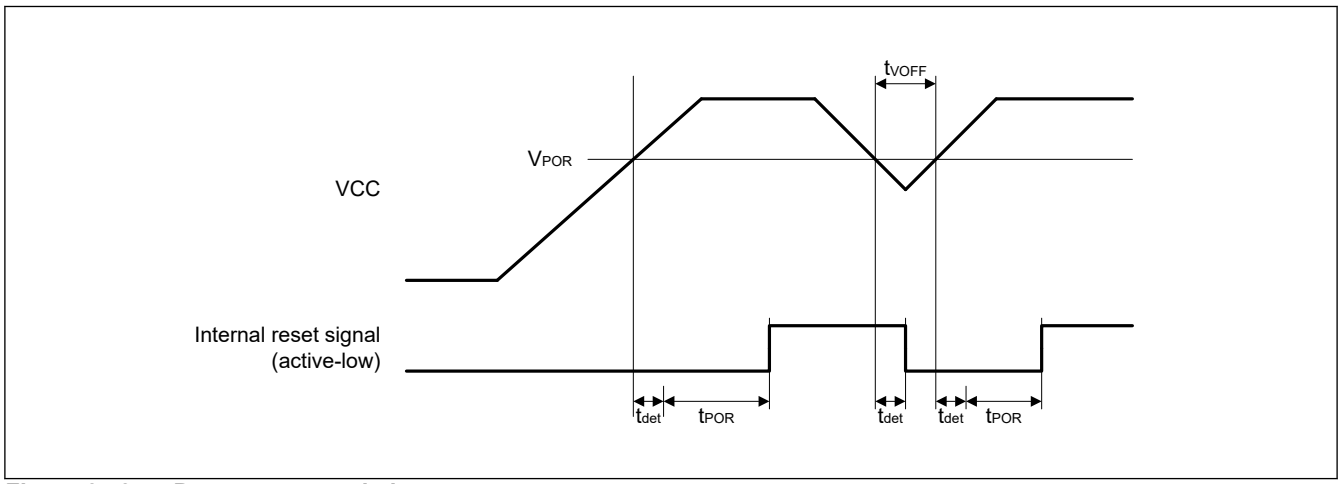


Figure 2.58 Power-on reset timing

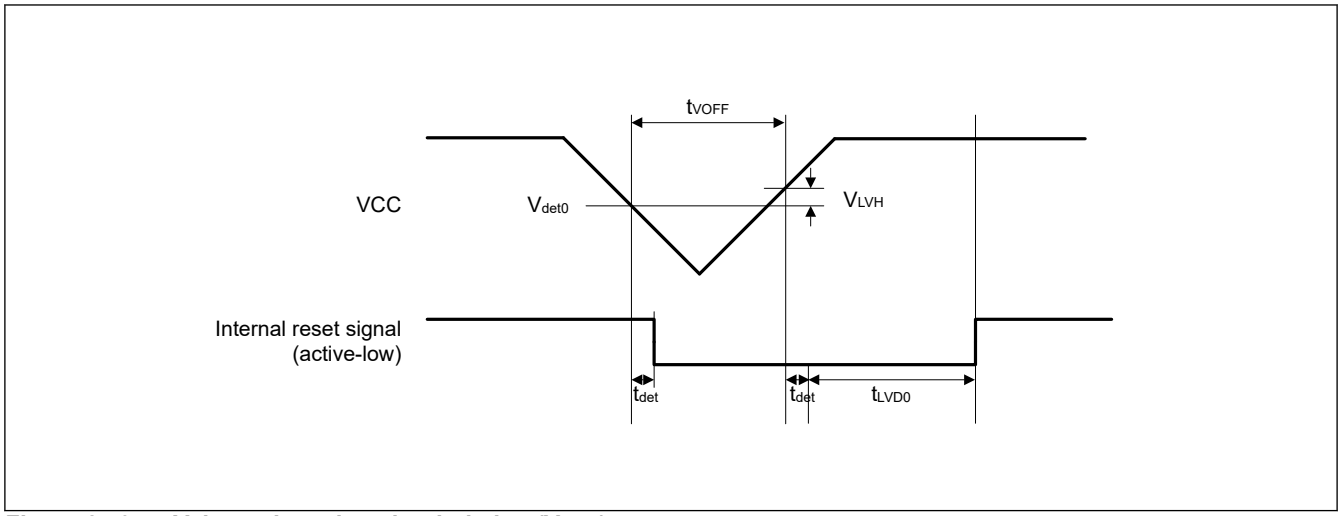


Figure 2.59 Voltage detection circuit timing (V_{det0})

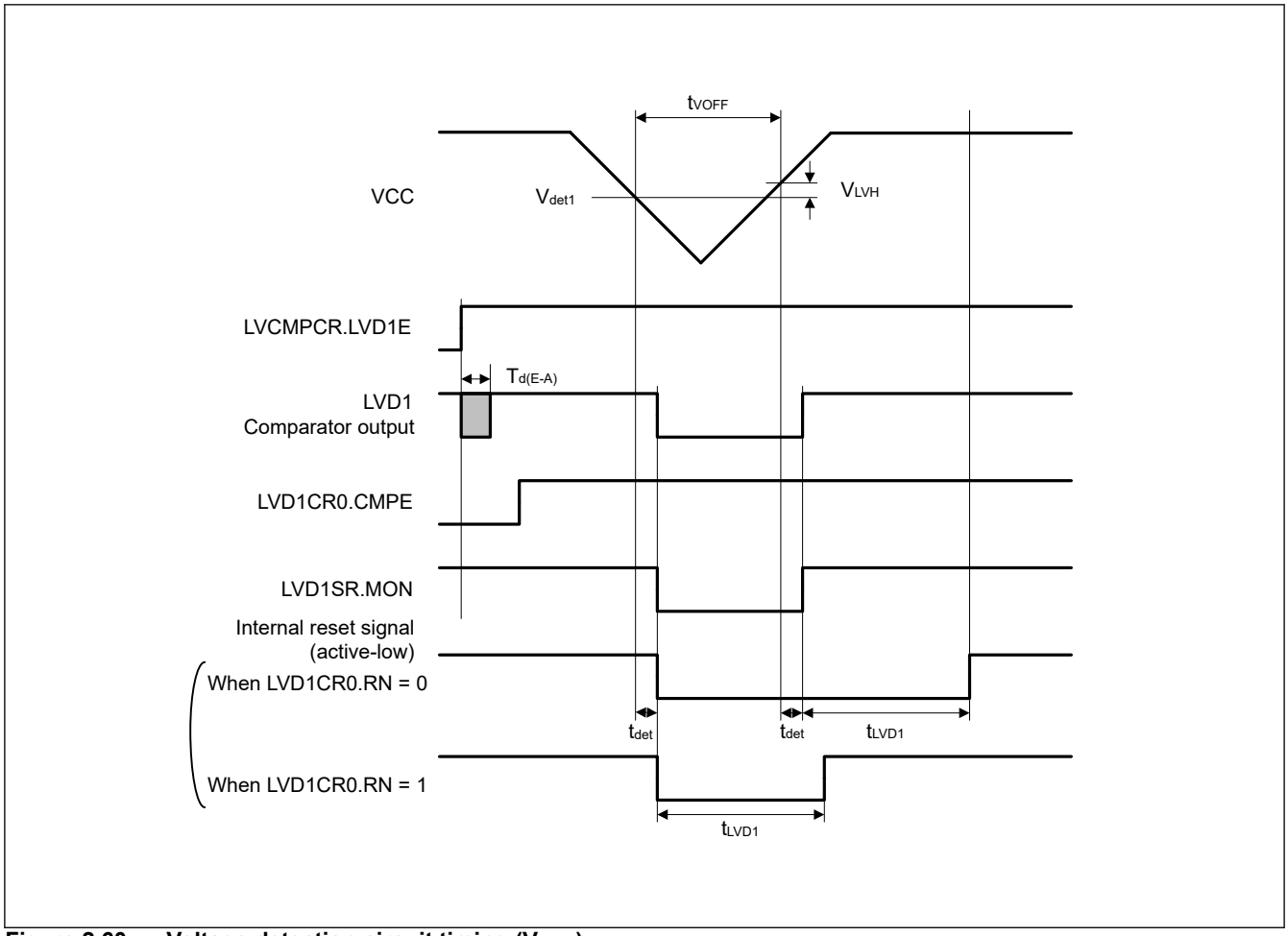


Figure 2.60 Voltage detection circuit timing (V_{det1})

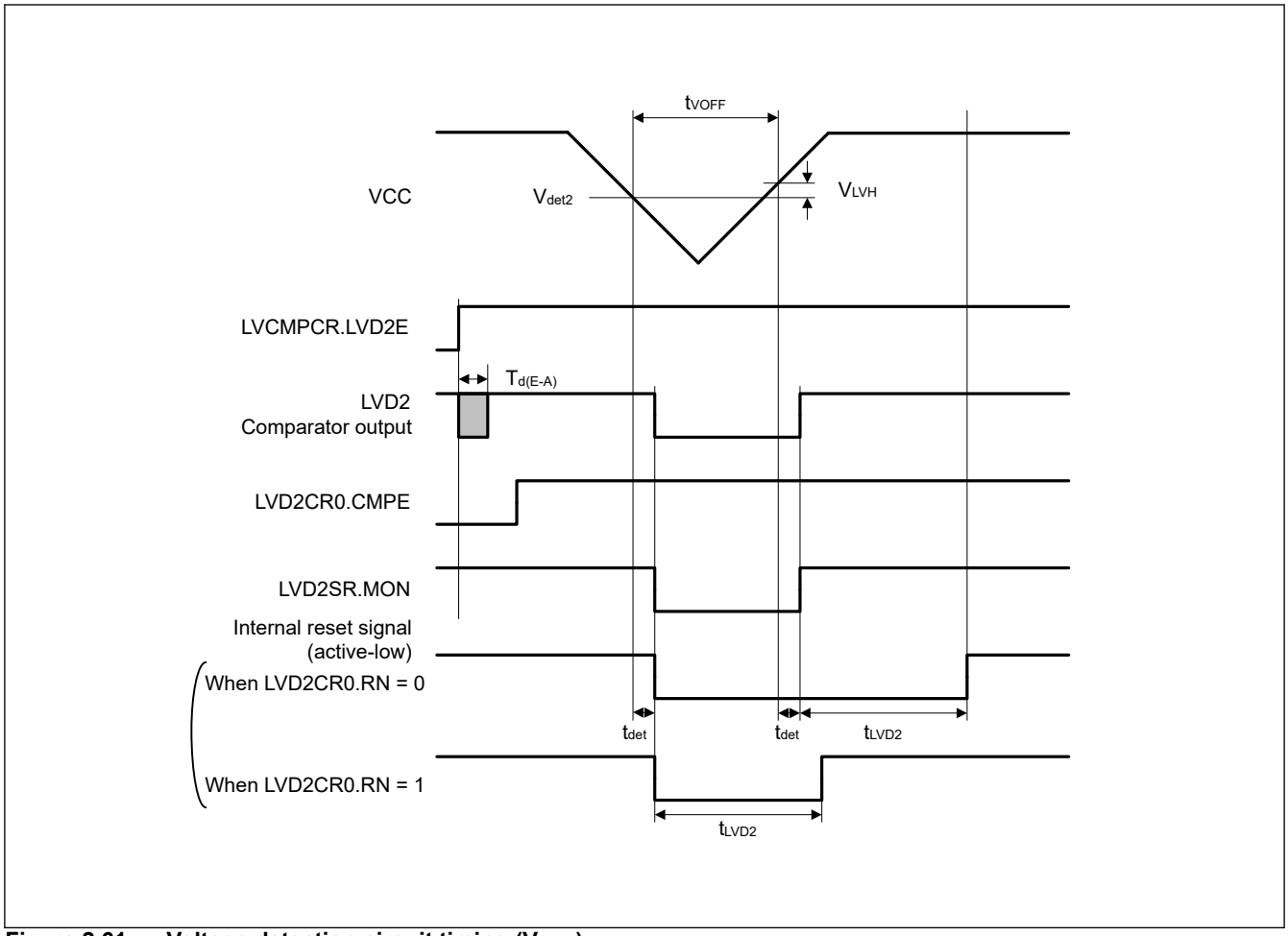


Figure 2.61 Voltage detection circuit timing (V_{det2})

2.9 Flash Memory Characteristics

2.9.1 Code Flash Memory Characteristics

Table 2.41 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	

Table 2.41 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*6	Max	Min	Typ*6	Max		
Suspend delay during programming	t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time	t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode	t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode	t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5	t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode	t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode	t_{REET}	—	—	144	—	—	80	µs	
Forced stop command	t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

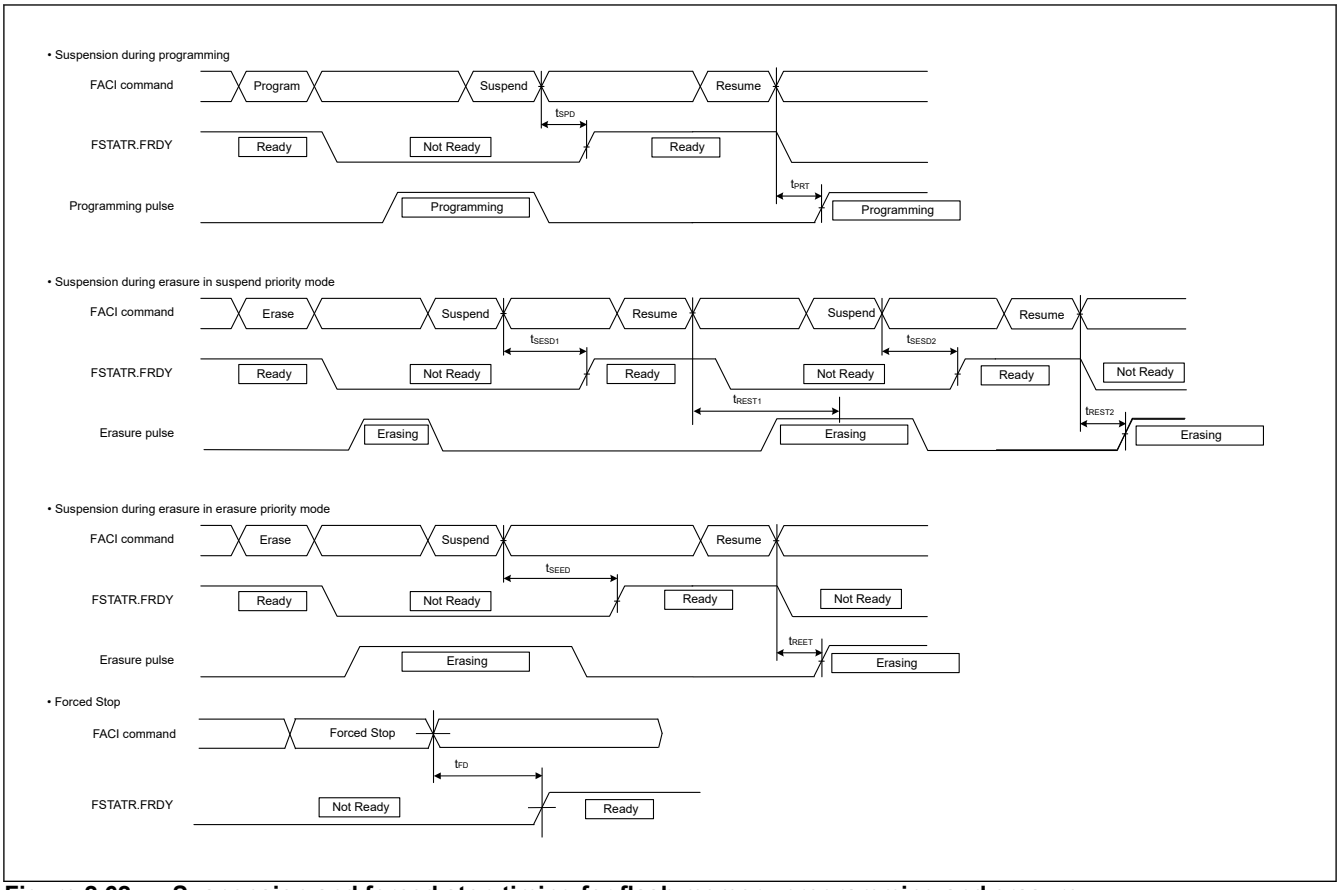


Figure 2.62 Suspension and forced stop timing for flash memory programming and erasure

2.9.2 Data Flash Memory Characteristics

Table 2.42 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

Table 2.42 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	µs	
Second erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	µs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

2.9.3 Option Setting Memory Characteristics

Table 2.43 Option setting memory characteristics

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

2.10 Joint Test Action Group (JTAG)

Table 2.44 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	—	—	ns	Figure 2.63
TCK clock high pulse width	t_{TCKH}	15	—	—	ns	
TCK clock low pulse width	t_{TCKL}	15	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	8	—	—	ns	Figure 2.64
TMS hold time	t_{TMSH}	8	—	—	ns	
TDI setup time	t_{TDIS}	8	—	—	ns	
TDI hold time	t_{TDIH}	8	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	20	ns	

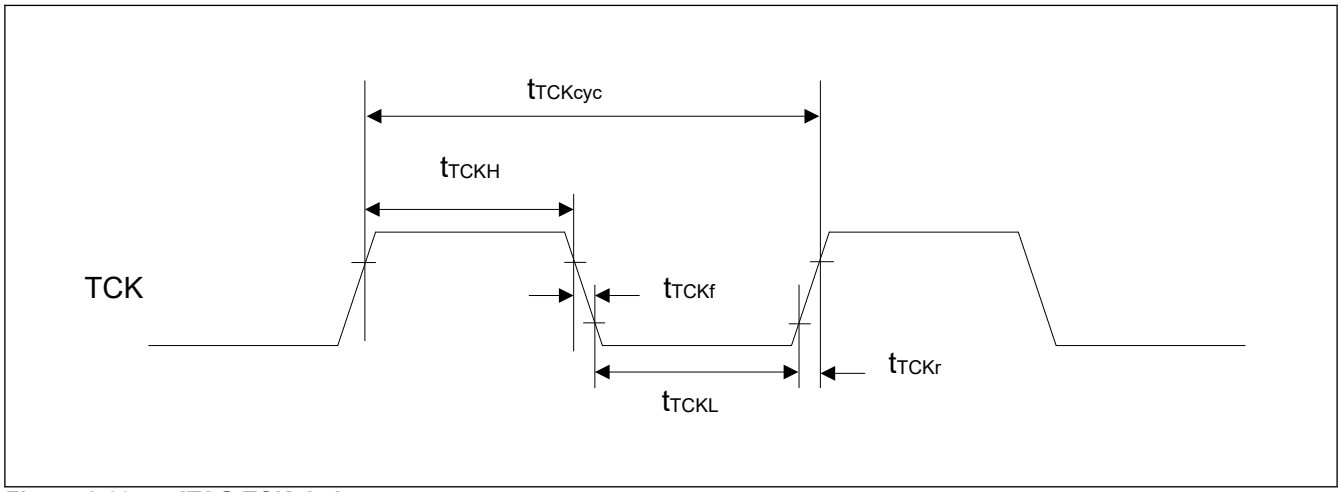


Figure 2.63 JTAG TCK timing

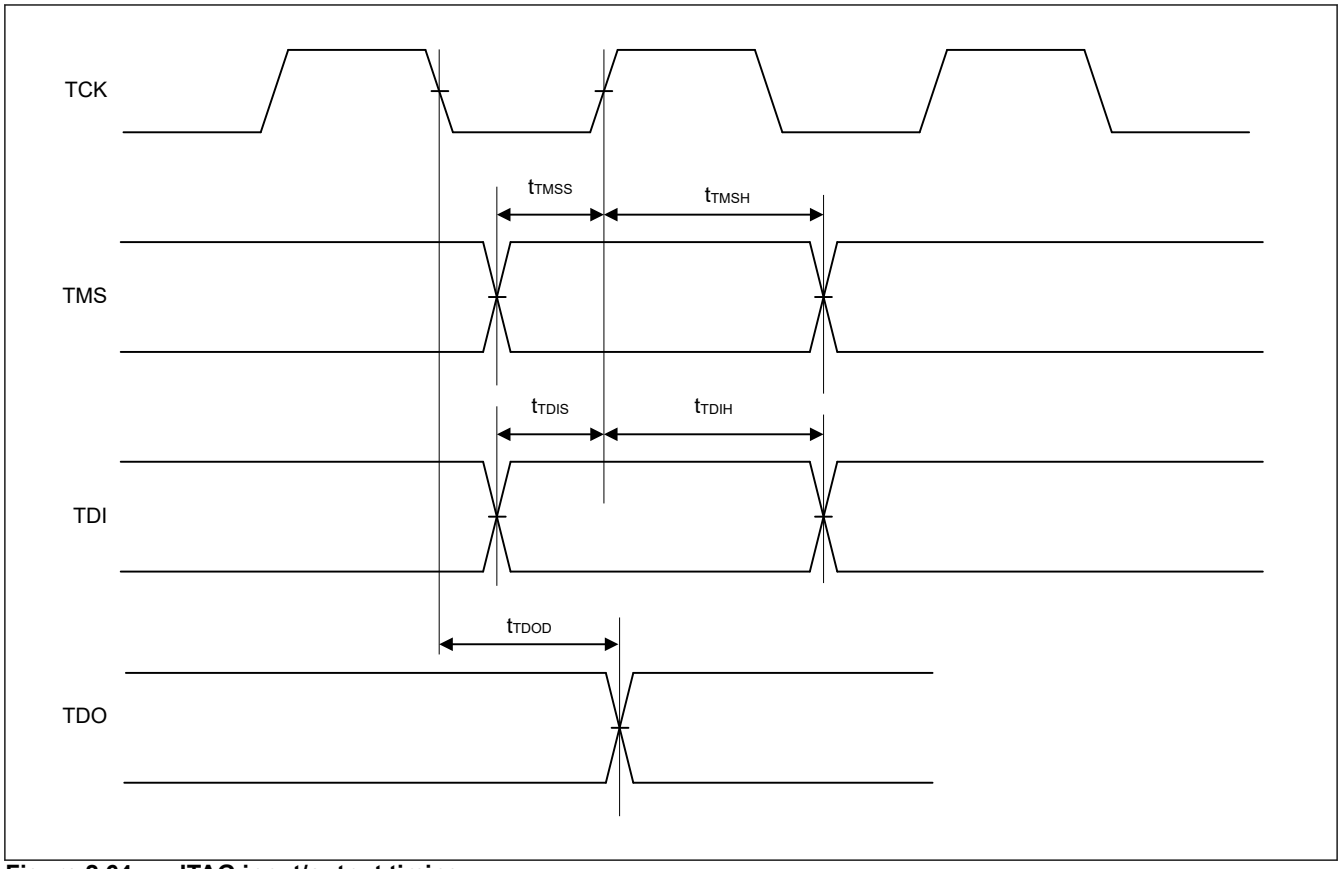


Figure 2.64 JTAG input/output timing

Appendix 1. Port States in Each Processing Mode

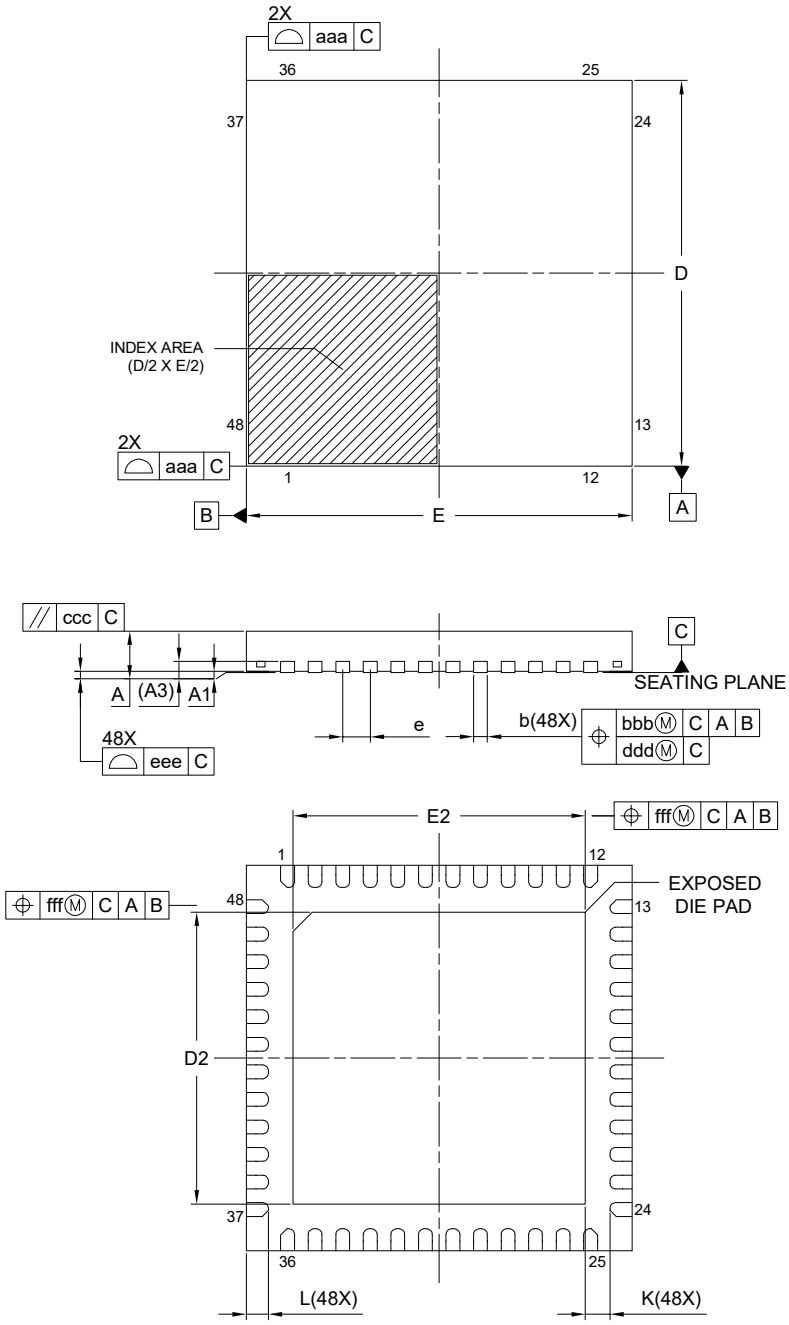
Function	Pin function	Reset	Software Standby mode	Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
					IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
JTAG	TCK/TMS/TDI	Pull-up	Keep-O	Keep	Hi-Z	Keep
	TDO	TDO output	Keep-O	Keep	TDO output	Keep
IRQ	IRQn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	IRQn-DS	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	AGTIOn (n = 1, 3)	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
PDM	PDM_DATAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	PDM_CLKn	Hi-Z	[SSPCR.PDMSOS = 1] PDM_CLK output	Keep	Hi-Z	Keep
I3C	SCLn/SDAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
DAC12	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

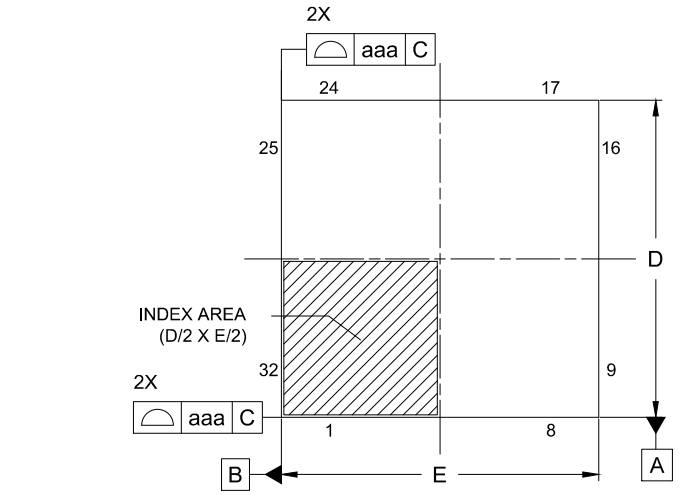
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

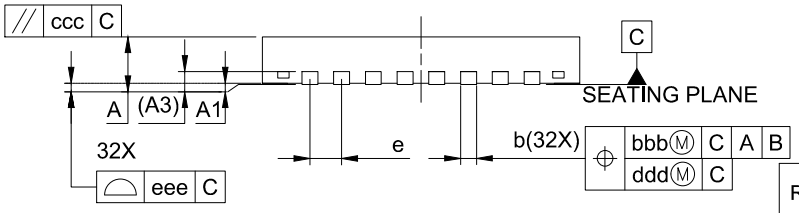


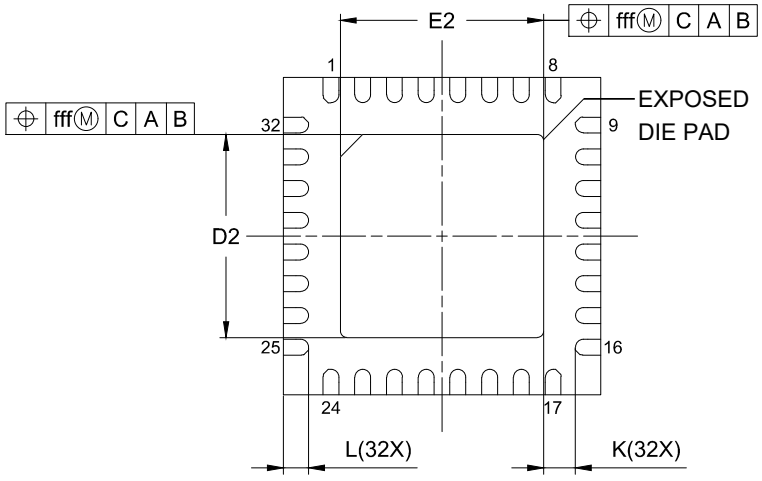
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.1 QFN 48-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



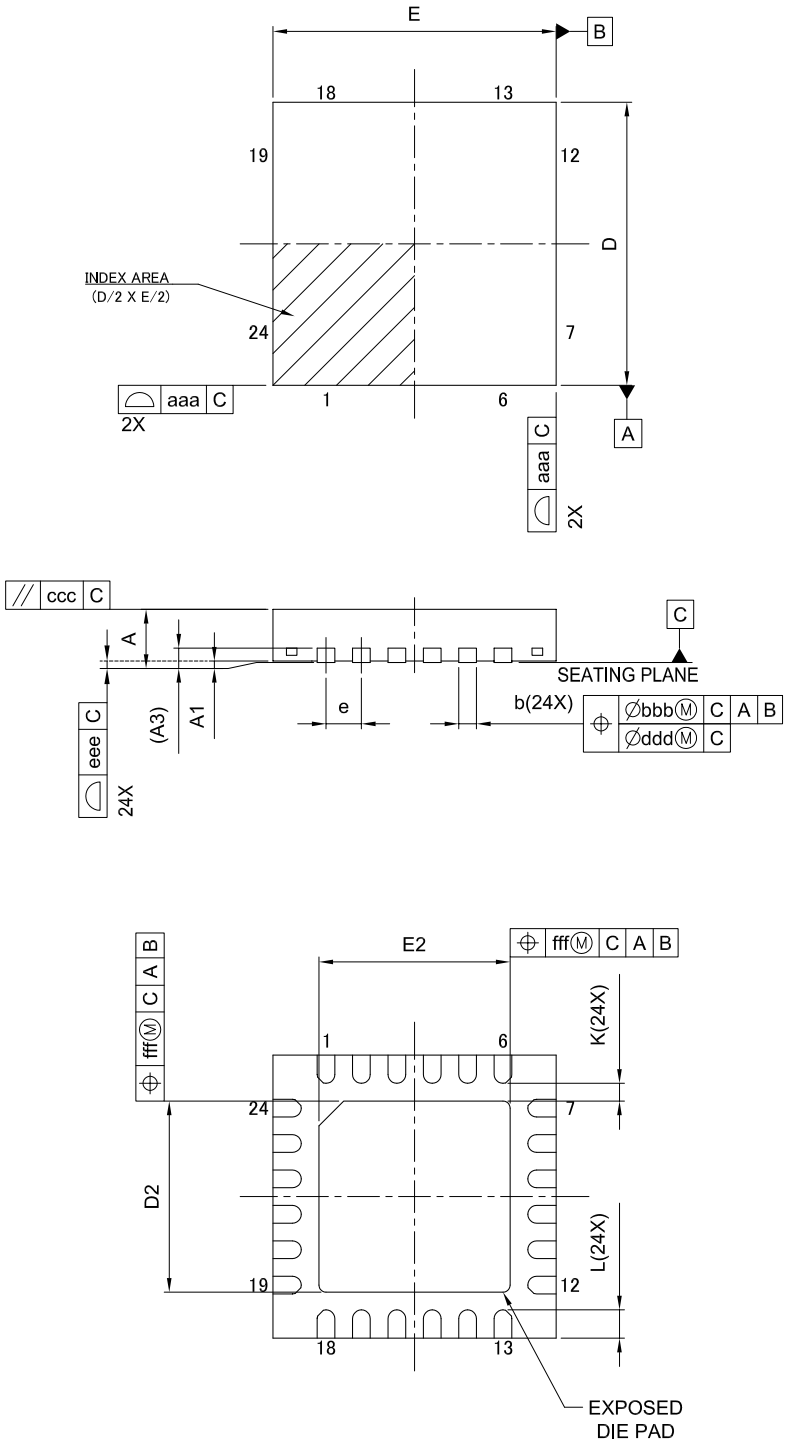




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.2 QFN 32-pin

JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HWQFN24-4×4-0.50	PWQN0024KG-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	2.65	2.70	2.75
E_2	2.65	2.70	2.75
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 2.3 QFN 24-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
DBG	Debug Function	0x4001_B000
FCACHE	Flash Cache	0x4001_C100
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4008_0000
PORT1	Port 1 Control Registers	0x4008_0020
PORT2	Port 2 Control Registers	0x4008_0040
PORT3	Port 3 Control Registers	0x4008_0060
PORT4	Port 4 Control Registers	0x4008_0080
PFS	Pmn Pin Function Control Register	0x4008_0800
ELC	Event Link Controller	0x4008_2000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D, E	0x4008_4000
SSIE0	Serial Sound Interface Enhanced 0	0x4009_D000
SSIE1	Serial Sound Interface Enhanced 1	0x4009_D100
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
AGT2	Low Power Asynchronous General purpose Timer 2	0x400E_8200
AGT3	Low Power Asynchronous General purpose Timer 3	0x400E_8300
TSN	Temperature Sensor	0x400F_3000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
SCI0	Serial Communication Interface 0	0x4011_8000
SCI9	Serial Communication Interface 9	0x4011_8900
IrDA	IrDA Interface	0x4011_8F00
SPI0	Serial Peripheral Interface 0	0x4011_A000
I3C	I3C Bus Interface	0x4011_F000
I3CWU	I3C Bus Interface Wake-up Unit	0x4011_F090
PDM	PDM Interface	0x4013_1000
GPT164	General PWM 16-Bit Timer 4	0x4016_9400
GPT165	General PWM 16-Bit Timer 5	0x4016_9500
GPT166	General PWM 16-Bit Timer 6	0x4016_9600
GPT167	General PWM 16-Bit Timer 7	0x4016_9700
ADC120	12-bit A/D Converter 0	0x4017_0000
DAC12	12-bit D/A converter	0x4017_1000
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000
QSPI	Quad-SPI	0x6400_0000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 2)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
RMPU, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	2	2	2	2	ICLK	Renesas Memory Protection Unit, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
DBG, FCACHE	0x4000_8000	0x4001_CFFF	2	2	2	2	ICLK	Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	3	3	3	3	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	7	7	6 to 7	6 to 7	PCLKB	System Control
PORTn, PFS	0x4008_0000	0x4008_0FFF	3	3	3 to 4	3 to 4	PCLKB	Port n Control Registers, Pmn Pin Function Control Register
ELC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	3	3	3	3	PCLKB	Event Link Controller, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	3	3	3	3	PCLKB	Module Stop Control
SSIEn	0x4009_D000	0x4009_DFFF	3	3	3	3	PCLKB	Serial Sound Interface Enhanced n
AGTn	0x400E_8000	0x400E_8FFF	3	5	3	5 to 6	PCLKB	Low Power Asynchronous General purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	3	3	2 to 4	2 to 4	PCLKB	Temperature Sensor
CRC, DOC	0x4010_8000	0x4010_9FFF	3	3	2 to 4	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit
SCIn, IrDA	0x4011_8000	0x4011_8FFF	3*2	3*2	2 to 4*2	2 to 4*2	PCLKA	Serial Communication Interface n, IrDA Interface
SPIn	0x4011_A000	0x4011_AFFF	3*3	3*3	2 to 4*3	2 to 4*3	PCLKA	Serial Peripheral Interface n
I3C	0x4011_F000	0x4011_FFFF	3	3	2 to 4	2 to 4	PCLKA	I3C bus interface
PDM	0x4013_1000	0x4013_1FFF	3	3	2 to 4	2 to 4	PCLKA	PDM Interface
GPT16n	0x4016_9400	0x4016_9FFF	6	4	5 to 7	3 to 5	PCLKA	General PWM 16-Bit Timer n
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	3	3	2 to 4	2 to 4	PCLKA	12-bit A/D Converter n, 12-bit D/A converter
QSPI	0x6400_0000	0x6400_000F	3	13 to*4	2 to 4	13 to*4	PCLKA	Quad-SPI
QSPI	0x6400_0010	0x6400_0013	3	3	2 to 4	2 to 4	PCLKA	Quad-SPI
QSPI	0x6400_0014	0x6400_0037	3	13 to*4	2 to 4	14 to*4	PCLKA	Quad-SPI
QSPI	0x6400_0804	0x6400_0807	2	2	1 to 3	1 to 3	PCLKA	Quad-SPI

Table 3.2 Access cycles (2 of 2)

Peripherals	Address		Number of access cycles					
			ICLK = FCLK		ICLK > FCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	3	3	2 to 4	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.
Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.
Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.
Note 4. The access cycles depend on the QSPI bus cycles.

Revision History

Revision 1.00 — Nobember 18, 2022

First draft release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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