

# R1EV58256BxxN Series

# R1EV58256BxxR Series

256K EEPROM (32-Kword × 8-bit)  
 Ready/ $\overline{\text{Busy}}$  and  $\overline{\text{RES}}$  function (R1EV58256BxxR)

R10DS0208EJ0201  
 Rev.2.01  
 Apr. 01, 2020

## Description

Renesas Electronics' R1EV58256BxxN series and R1EV58256BxxR series are electrically erasable and programmable EEPROM's organized as 32768-word × 8-bit. They have realized high speed, low power consumption and high reliability by employing advanced MONOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

## Features

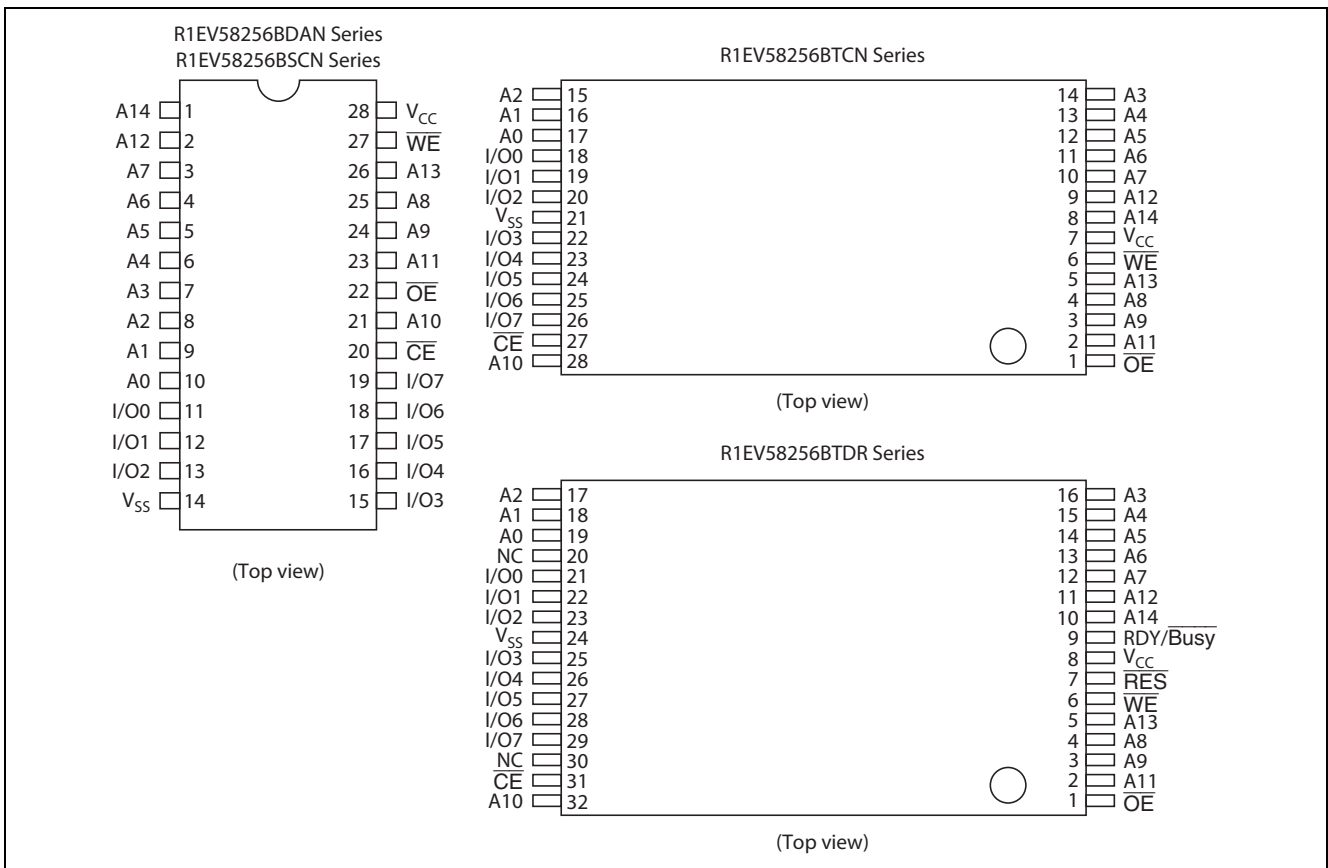
- Single supply: 2.7 to 5.5 V
- Access time:
  - 85 ns (max)/100 ns (max) at  $4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$
  - 120 ns (max) at  $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
- Power dissipation:
  - Active: 20 mW/MHz (typ)
  - Standby: 110  $\mu\text{W}$  (max)
- On-chip latches: address, data,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{WE}}$
- Automatic byte write: 10 ms (max)
- Automatic page write (64 bytes): 10 ms (max)
- Ready/ $\overline{\text{Busy}}$  (only the R1EV58256BxxR series)
- $\overline{\text{Data}}$  polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MONOS cell technology
- $10^5$  or more erase/write cycles
- 10 or more years data retention
- Software data protection
- Write protection by  $\overline{\text{RES}}$  pin (only the R1EV58256BxxR series)
- Temperature range:  $-40$  to  $85^\circ\text{C}$
- There are lead free products.

### Ordering Information

| Orderable Part Name | Access time          | Package   | Shipping Container | Quantity                                     |
|---------------------|----------------------|---|--------------------|--|
| R1EV58256BDANBI#B*  | 85ns/100ns/<br>120ns | 600mil 28-pin plastic DiP<br>PRDP0028AB-A (DP-28V)  | Tube               | Max. 13 pcs/tube<br>Max. 325pcs/inner box    |
| R1EV58256BSCNBI#B*  | 85ns/100ns/<br>120ns | 400mil 28-pin plastic SOP<br>PRSP0028DC-A (FP-28DV) | Tube               | Max. 25 pcs/tube<br>Max. 1,000 pcs/inner box |
| R1EV58256BSCNBI#S*  | 85ns/100ns/<br>120ns | 400mil 28-pin plastic SOP<br>PRSP0028DC-A (FP-28DV) | Tape and reel      | 1,000 pcs/reel                               |
| R1EV58256BTCNBI#B*  | 85ns/100ns/<br>120ns | 28-pin plastic TSOP<br>PTSA0028ZB-A (TFP-28DBV)     | Tray               | Max. 60 pcs/tray<br>Max. 600 pcs/inner box   |
| R1EV58256BTDRBI#B*  | 85ns/100ns/<br>120ns | 32-pin plastic TSOP<br>PTSA0032KD-A (TFP-32DAV)     | Tray               | Max. 60 pcs/tray<br>Max. 600 pcs/inner box   |

Notes 1. \*= Revision code (0,2 etc.)

### Pin Arrangement



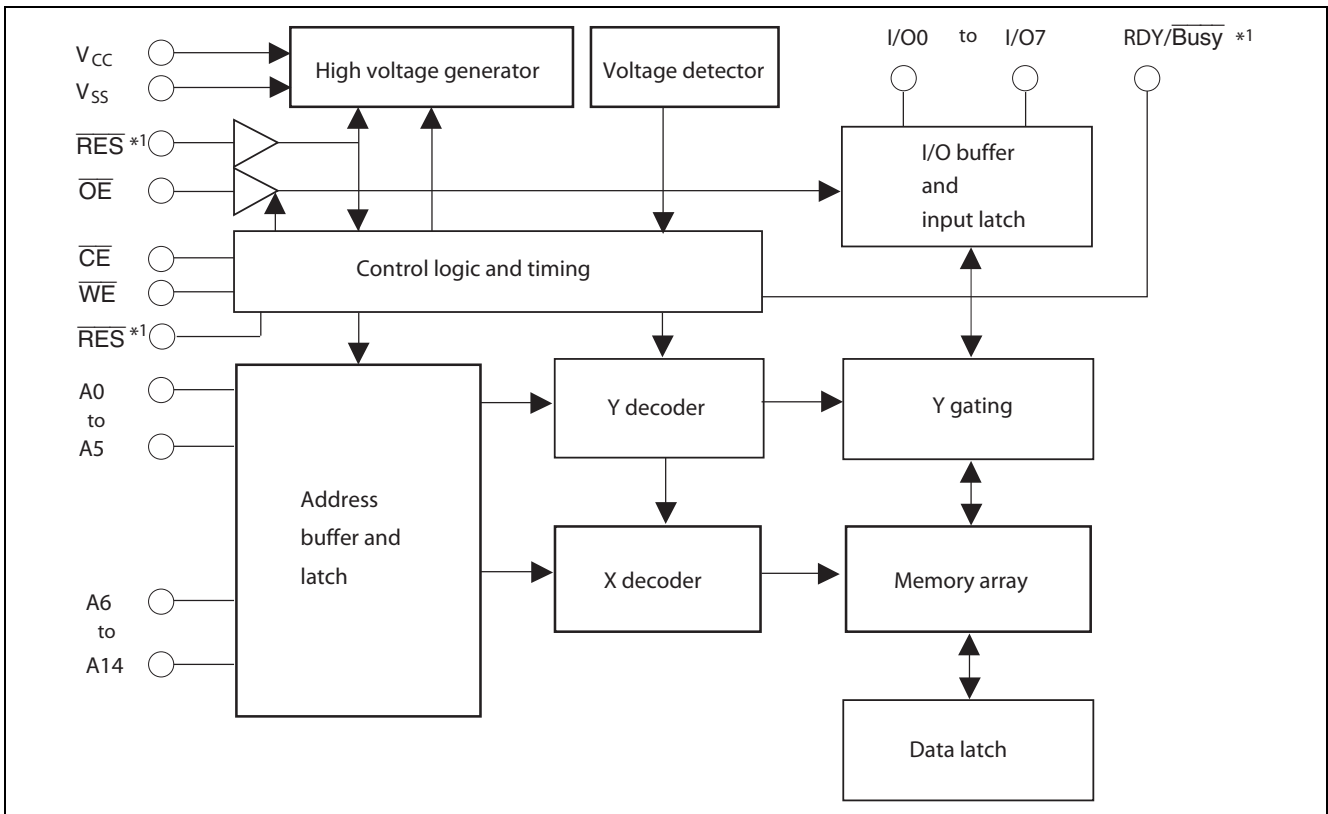
### Pin Description

| Pin name            | Function          |
|---------------------|-------------------|
| A0 to A14           | Address input     |
| I/O0 to I/O7        | Data input/output |
| $\overline{OE}$     | Output enable     |
| $\overline{CE}$     | Chip enable       |
| $\overline{WE}$     | Write enable      |
| V <sub>CC</sub>     | Power supply      |
| V <sub>SS</sub>     | Ground            |
| RDY/Busy*1          | Ready busy        |
| $\overline{RES}$ *1 | Reset             |
| NC                  | No connection     |

Note: 1. This function is supported by only the R1EV58256BxxR series.

### Block Diagram

Note: 1. This function is supported by only the R1EV58256BxxR series.



## Operation Table

| Operation     | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{RES}^{*3}$ | $RDY/Busy^{*3}$    | I/O             |
|---------------|-----------------|-----------------|-----------------|-----------------------|--------------------|-----------------|
| Read          | $V_{IL}$        | $V_{IL}$        | $V_{IH}$        | $V_H^{*1}$            | High-Z             | Dout            |
| Standby       | $V_{IH}$        | $\times^{*2}$   | $\times$        | $\times$              | High-Z             | High-Z          |
| Write         | $V_{IL}$        | $V_{IH}$        | $V_{IL}$        | $V_H$                 | High-Z to $V_{OL}$ | Din             |
| Deselect      | $V_{IL}$        | $V_{IH}$        | $V_{IH}$        | $V_H$                 | High-Z             | High-Z          |
| Write inhibit | $\times$        | $\times$        | $V_{IH}$        | $\times$              | —                  | —               |
|               | $\times$        | $V_{IL}$        | $\times$        | $\times$              | —                  | —               |
| Data polling  | $V_{IL}$        | $V_{IL}$        | $V_{IH}$        | $V_H$                 | $V_{OL}$           | Data out (I/O7) |
| Program reset | $\times$        | $\times$        | $\times$        | $V_{IL}$              | High-Z             | High-Z          |

- Notes: 1. Refer to the recommended DC operating condition.  
 2.  $\times$ : Don't care  
 3. This function is supported by only the R1EV58256BxxR series.

## Absolute Maximum Ratings

| Parameter                           | Symbol    | Value            | Unit |
|-------------------------------------|-----------|------------------|------|
| Supply voltage relative to $V_{SS}$ | $V_{CC}$  | -0.6 to +7.0     | V    |
| Input voltage relative to $V_{SS}$  | $V_{in}$  | -0.5*1 to +7.0*3 | V    |
| Operating temperature range*2       | $T_{opr}$ | -40 to +85       | °C   |
| Storage temperature range           | $T_{stg}$ | -55 to +125      | °C   |

- Notes: 1.  $V_{in\ min} = -3.0\ V$  for pulse width  $\leq 50\ ns$   
 2. Including electrical characteristics and data retention  
 3. Should not exceed  $V_{CC} + 1.0\ V$ .

## Recommended DC Operating Conditions

| Parameter             | Symbol     | Min            | Typ | Max                 | Unit |
|-----------------------|------------|----------------|-----|---------------------|------|
| Supply voltage        | $V_{CC}$   | 2.7            | 3.0 | 5.5                 | V    |
|                       | $V_{SS}$   | 0              | 0   | 0                   | V    |
| Input voltage*5       | $V_{IL}$   | -0.3*1         | —   | 0.8                 | V    |
|                       | $V_{IH}$   | 1.9*2          | —   | $V_{CC} + 0.3^{*3}$ | V    |
|                       | $V_H^{*4}$ | $V_{CC} - 0.5$ | —   | $V_{CC} + 1.0$      | V    |
| Operating temperature | $T_{opr}$  | -40            | —   | +85                 | °C   |

- Notes: 1.  $V_{IL\ min}$ : -1.0 V for pulse width  $\leq 50\ ns$ .  
 2.  $V_{IH\ min}$  for  $V_{CC} = 3.6$  to  $5.5\ V$  is  $2.2\ V$ .  
 3.  $V_{IH\ max}$ :  $V_{CC} + 1.0\ V$  for pulse width  $\leq 50\ ns$ .  
 4. This function is supported by only the R1EV58256BxxR series  
 5. Refer to the recommended AC operating condition during read and write operation.

## DC Characteristics

(Ta = -40 to +85°C, V<sub>CC</sub> = 2.7 to 5.5 V)

| Parameter                         | Symbol           | Min                   | Typ | Max | Unit | Test conditions  |
|-----------------------------------|------------------|-----------------------|-----|-----|------|--|
| Input leakage current             | I <sub>LI</sub>  | —                     | —   | 2*1 | μA   | V <sub>CC</sub> = 5.5 V, V <sub>in</sub> = 5.5 V                                 |
| Output leakage current            | I <sub>LO</sub>  | —                     | —   | 2   | μA   | V <sub>CC</sub> = 5.5 V, V <sub>out</sub> = 5.5/0.4 V                            |
| Standby V <sub>CC</sub> current   | I <sub>CC1</sub> | —                     | —   | 20  | μA   | $\overline{CE} = V_{CC}$   |
|                                   | I <sub>CC2</sub> | —                     | —   | 1   | mA   | $\overline{CE} = V_{IH}$   |
| Operating V <sub>CC</sub> current | I <sub>CC3</sub> | —                     | —   | 8   | mA   | I <sub>out</sub> = 0 mA, Duty = 100%,<br>Cycle = 1 μs, V <sub>CC</sub> = 3.6 V   |
|                                   |                  | —                     | —   | 12  | mA   | I <sub>out</sub> = 0 mA, Duty = 100%,<br>Cycle = 1 μs, V <sub>CC</sub> = 5.5 V   |
|                                   |                  | —                     | —   | 12  | mA   | I <sub>out</sub> = 0 mA, Duty = 100%,<br>Cycle = 120 ns, V <sub>CC</sub> = 3.6 V |
|                                   |                  | —                     | —   | 30  | mA   | I <sub>out</sub> = 0 mA, Duty = 100%,<br>Cycle = 120 ns, V <sub>CC</sub> = 5.5 V |
| Output low voltage                | V <sub>OL</sub>  | —                     | —   | 0.4 | V    | I <sub>OL</sub> = 2.1 mA   |
| Output high voltage               | V <sub>OH</sub>  | V <sub>CC</sub> × 0.8 | —   | —   | V    | I <sub>OH</sub> = -400 μA  |

Note: 1. I<sub>LI</sub> on RES = 100 μA max (only the R1EV58256BXXR series)

## Capacitance

(Ta = +25°C, f = 1 MHz)

| Parameter            | Symbol           | Min | Typ | Max | Unit | Test conditions        |
|----------------------|------------------|-----|-----|-----|------|------------------------|
| Input capacitance*1  | C <sub>in</sub>  | —   | —   | 6   | pF   | V <sub>in</sub> = 0 V  |
| Output capacitance*1 | C <sub>out</sub> | —   | —   | 12  | pF   | V <sub>out</sub> = 0 V |

Note: 1. This parameter is periodically sampled and not 100% tested.

## AC Characteristics

(Ta = -40 to +85°C, V<sub>CC</sub> = 4.5V to 5.5V)

### Test Conditions

- Input pulse levels: 0.4 V to 3.0 V, 0 V to V<sub>CC</sub> ( $\overline{RES}$  pin\*2)
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 2.0 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.5 V, 1.5 V

### Read Cycle

| Parameter  | Symbol           | Min | Max | Unit | Test conditions  |
|--|------------------|-----|-----|------|--|
| Address to output delay                                    | t <sub>ACC</sub> | —   | 85  | ns   | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| $\overline{CE}$ to output delay                            | t <sub>CE</sub>  | —   | 85  | ns   | $\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$                 |
| $\overline{OE}$ to output delay                            | t <sub>OE</sub>  | 10  | 40  | ns   | $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$                 |
| Address to output hold                                     | t <sub>OH</sub>  | 0   | —   | ns   | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| $\overline{OE}$ ( $\overline{CE}$ ) high to output float*1 | t <sub>DF</sub>  | 0   | 40  | ns   | $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$                 |
| $\overline{RES}$ low to output float*1, 2                  | t <sub>DFR</sub> | 0   | 350 | ns   | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| $\overline{RES}$ to output delay*2                         | t <sub>RR</sub>  | 0   | 450 | ns   | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |

## Write Cycle

| Parameter   | Symbol     | Min*3 | Typ | Max  | Unit    | Test conditions |
|---|------------|-------|-----|------|---------|-----------------|
| Address setup time  | $t_{AS}$   | 0     | —   | —    | ns      |                 |
| Address hold time   | $t_{AH}$   | 50    | —   | —    | ns      |                 |
| $\overline{CE}$ to write setup time ( $\overline{WE}$ controlled) | $t_{CS}$   | 0     | —   | —    | ns      |                 |
| $\overline{CE}$ hold time ( $\overline{WE}$ controlled)           | $t_{CH}$   | 0     | —   | —    | ns      |                 |
| $\overline{WE}$ to write setup time ( $\overline{CE}$ controlled) | $t_{WS}$   | 0     | —   | —    | ns      |                 |
| $\overline{WE}$ hold time ( $\overline{CE}$ controlled)           | $t_{WH}$   | 0     | —   | —    | ns      |                 |
| $\overline{OE}$ to write setup time                               | $t_{OES}$  | 0     | —   | —    | ns      |                 |
| $\overline{OE}$ hold time   | $t_{OEHL}$ | 0     | —   | —    | ns      |                 |
| Data setup time   | $t_{DS}$   | 50    | —   | —    | ns      |                 |
| Data hold time  | $t_{DH}$   | 0     | —   | —    | ns      |                 |
| $\overline{WE}$ pulse width ( $\overline{WE}$ controlled)         | $t_{WP}$   | 0.100 | —   | 30   | $\mu$ s |                 |
| $\overline{CE}$ pulse width ( $\overline{CE}$ controlled)         | $t_{CW}$   | 0.100 | —   | 30   | $\mu$ s |                 |
| Data latch time   | $t_{DL}$   | 50    | —   | —    | ns      |                 |
| Byte load cycle   | $t_{BLC}$  | 0.2   | —   | 30   | $\mu$ s |                 |
| Byte load window  | $t_{BL}$   | 100   | —   | —    | $\mu$ s |                 |
| Write cycle time  | $t_{WC}$   | —     | —   | 10*4 | ms      |                 |
| Time to device busy   | $t_{DB}$   | 120   | —   | —    | ns      |                 |
| Write start time  | $t_{DW}$   | 0*5   | —   | —    | ns      |                 |
| Reset protect time*2  | $t_{RP}$   | 100   | —   | —    | $\mu$ s |                 |
| Reset high time*2, 6  | $t_{RES}$  | 1     | —   | —    | $\mu$ s |                 |

- Notes:
1.  $t_{DF}$  and  $t_{DFR}$  are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
  2. This function is supported by only the R1EV58256BxxR series.
  3. Use this device in longer cycle than this value.
  4.  $t_{WC}$  must be longer than this value unless polling techniques or  $\overline{RDY}/\overline{Busy}$  (only the R1EV58256BxxR series) are used. This device automatically completes the internal write operation within this value.
  5. Next read or write operation can be initiated after  $t_{DW}$  if polling techniques or  $\overline{RDY}/\overline{Busy}$  (only the R1EV58256BxxR series) are used.
  6. This parameter is sampled and not 100% tested.
  7. A6 through A14 are page address and these addresses are latched at the first falling edge of  $\overline{WE}$ .
  8. A6 through A14 are page address and these addresses are latched at the first falling edge of  $\overline{CE}$ .
  9. See AC read characteristics.

**AC Characteristics**(Ta = -40 to +85°C, V<sub>CC</sub> = 2.7 to 5.5 V)**Test Conditions**

- Input pulse levels: 0.4 V to 2.4 V (V<sub>CC</sub> ≤ 3.6V), 0.4V to 3.0 V (V<sub>CC</sub> > 3.6 V), 0 V to V<sub>CC</sub> ( $\overline{\text{RES}}$  pin\*2)
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 1.8 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.5 V, 1.5 V

**Read Cycle**

| Parameter  | Symbol           | Min | Max | Unit | Test conditions   |
|--|------------------|-----|-----|------|---|
| Address to output delay                            | t <sub>ACC</sub> | —   | 120 | ns   | $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$ |
| $\overline{\text{CE}}$ to output delay             | t <sub>CE</sub>  | —   | 120 | ns   | $\overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$                        |
| $\overline{\text{OE}}$ to output delay             | t <sub>OE</sub>  | 10  | 60  | ns   | $\overline{\text{CE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$                        |
| Address to output hold                             | t <sub>OH</sub>  | 0   | —   | ns   | $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$ |
| $\overline{\text{OE}}$ (CE) high to output float*1 | t <sub>DF</sub>  | 0   | 40  | ns   | $\overline{\text{CE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$                        |
| $\overline{\text{RES}}$ low to output float*1, 2   | t <sub>DFR</sub> | 0   | 350 | ns   | $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$ |
| $\overline{\text{RES}}$ to output delay*2          | t <sub>RR</sub>  | 0   | 600 | ns   | $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$ |

**Write Cycle**

| Parameter   | Symbol    | Min*3 | Typ | Max  | Unit    | Test conditions |
|---|-----------|-------|-----|------|---------|-----------------|
| Address setup time  | $t_{AS}$  | 0     | —   | —    | ns      |                 |
| Address hold time   | $t_{AH}$  | 50    | —   | —    | ns      |                 |
| $\overline{CE}$ to write setup time ( $\overline{WE}$ controlled) | $t_{CS}$  | 0     | —   | —    | ns      |                 |
| $\overline{CE}$ hold time ( $\overline{WE}$ controlled)           | $t_{CH}$  | 0     | —   | —    | ns      |                 |
| $\overline{WE}$ to write setup time ( $\overline{CE}$ controlled) | $t_{WS}$  | 0     | —   | —    | ns      |                 |
| $\overline{WE}$ hold time ( $\overline{CE}$ controlled)           | $t_{WH}$  | 0     | —   | —    | ns      |                 |
| $\overline{OE}$ to write setup time                               | $t_{OES}$ | 0     | —   | —    | ns      |                 |
| $\overline{OE}$ hold time   | $t_{OEH}$ | 0     | —   | —    | ns      |                 |
| Data setup time   | $t_{DS}$  | 70    | —   | —    | ns      |                 |
| Data hold time  | $t_{DH}$  | 0     | —   | —    | ns      |                 |
| $\overline{WE}$ pulse width ( $\overline{WE}$ controlled)         | $t_{WP}$  | 0.200 | —   | 30   | $\mu$ s |                 |
| $\overline{CE}$ pulse width ( $\overline{CE}$ controlled)         | $t_{CW}$  | 0.200 | —   | 30   | $\mu$ s |                 |
| Data latch time   | $t_{DL}$  | 100   | —   | —    | ns      |                 |
| Byte load cycle   | $t_{BLC}$ | 0.3   | —   | 30   | $\mu$ s |                 |
| Byte load window  | $t_{BL}$  | 100   | —   | —    | $\mu$ s |                 |
| Write cycle time  | $t_{WC}$  | —     | —   | 10*4 | ms      |                 |
| Time to device busy   | $t_{DB}$  | 120   | —   | —    | ns      |                 |
| Write start time  | $t_{DW}$  | 0*5   | —   | —    | ns      |                 |
| Reset protect time*2  | $t_{RP}$  | 100   | —   | —    | $\mu$ s |                 |
| Reset high time*2, 6  | $t_{RES}$ | 1     | —   | —    | $\mu$ s |                 |

Notes: 1.  $t_{DF}$  and  $t_{DFR}$  are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

2. This function is supported by only the R1EV58256BxxR series.

3. Use this device in longer cycle than this value.

4.  $t_{WC}$  must be longer than this value unless polling techniques or  $\overline{RDY/Busy}$  (only the R1EV58256BxxR series) are used. This device automatically completes the internal write operation within this value.

5. Next read or write operation can be initiated after  $t_{DW}$  if polling techniques or  $\overline{RDY/Busy}$  (only the R1EV58256BxxR series) are used.

6. This parameter is sampled and not 100% tested.

7. A6 through A14 are page addresses and these addresses are latched at the first falling edge of  $\overline{WE}$ .

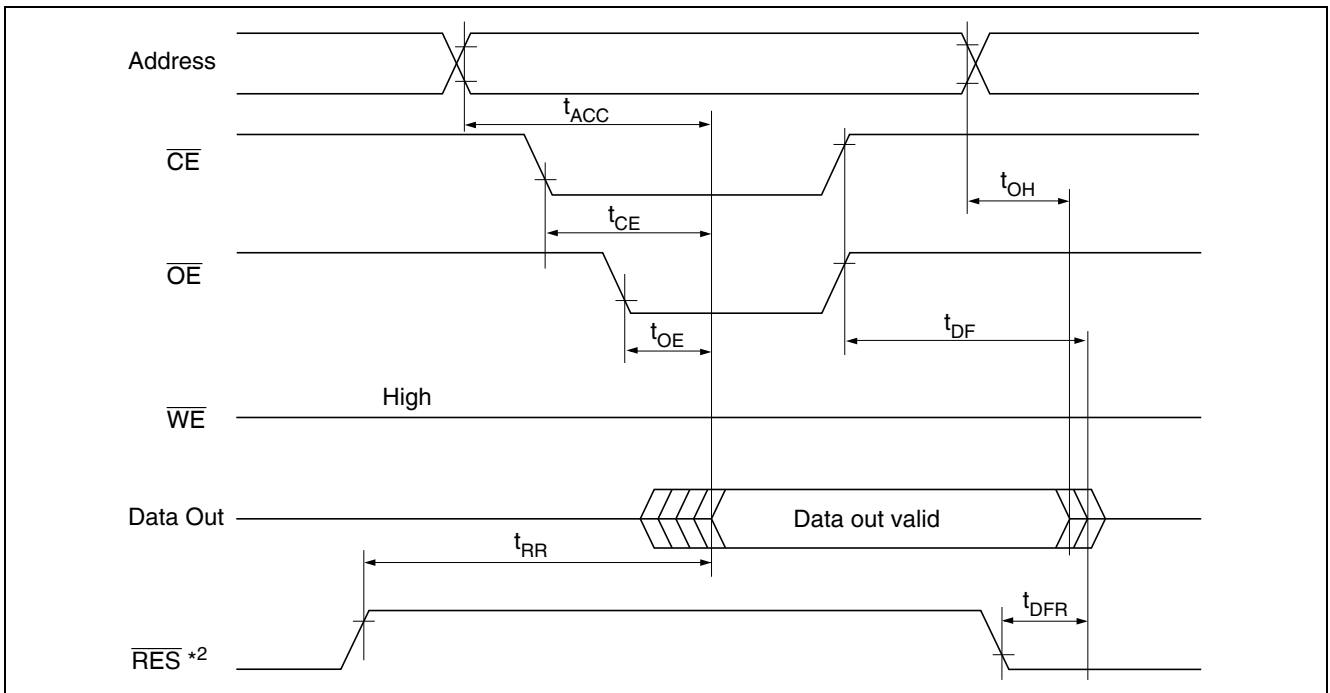
8. A6 through A14 are page addresses and these addresses are latched at the first falling edge of  $\overline{CE}$ .

9. See AC read characteristics.

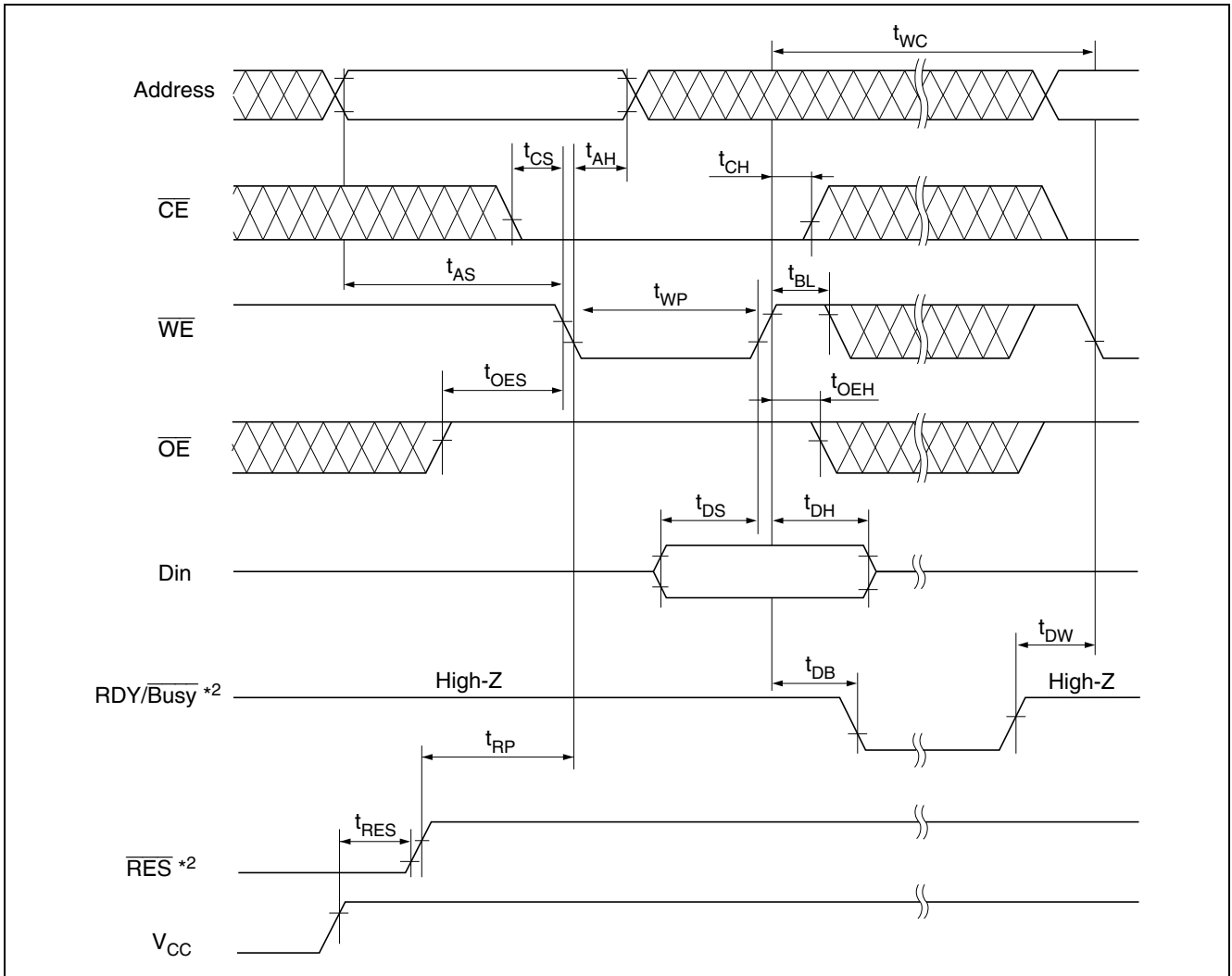


## Timing Waveforms

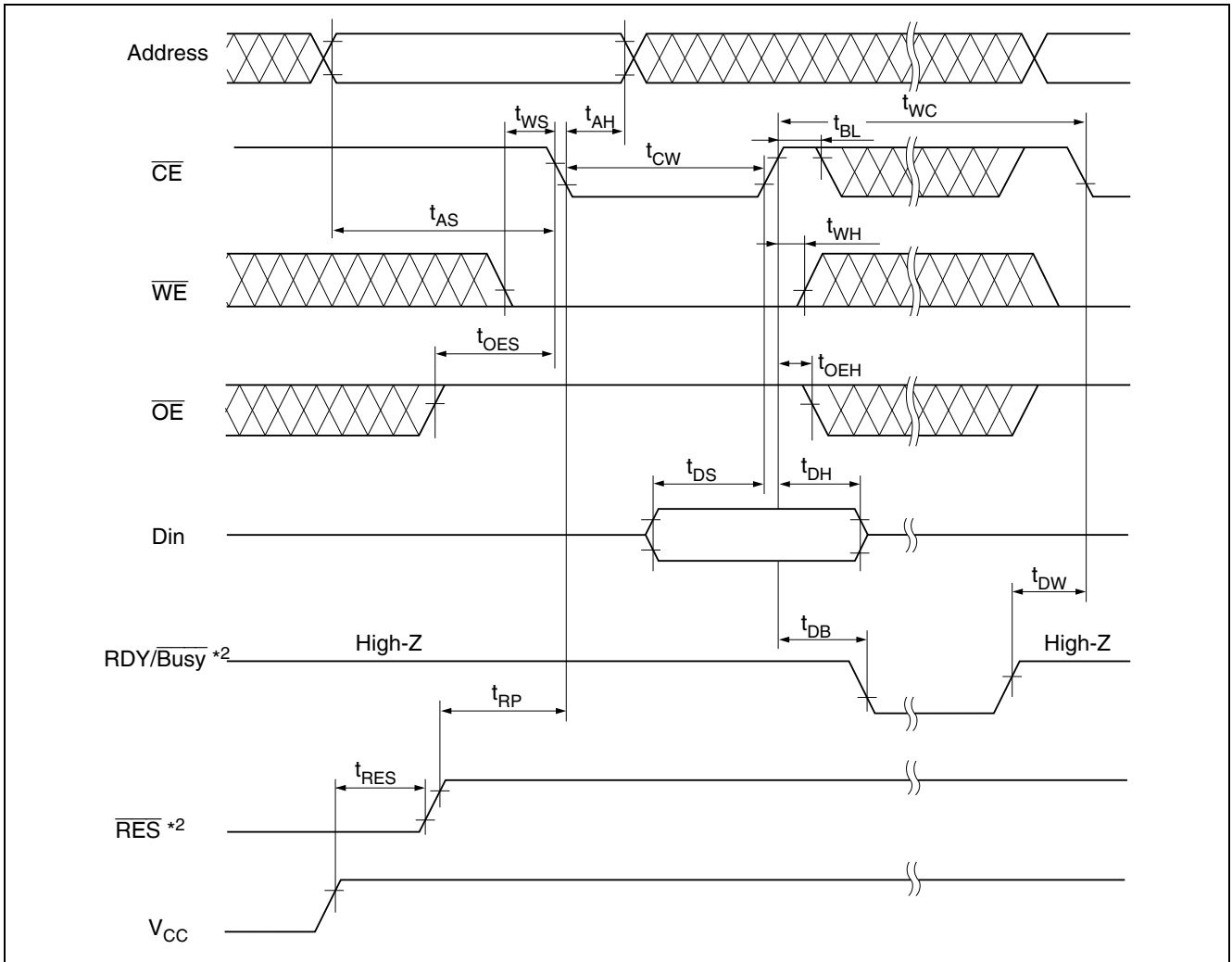
### Read Timing Waveform



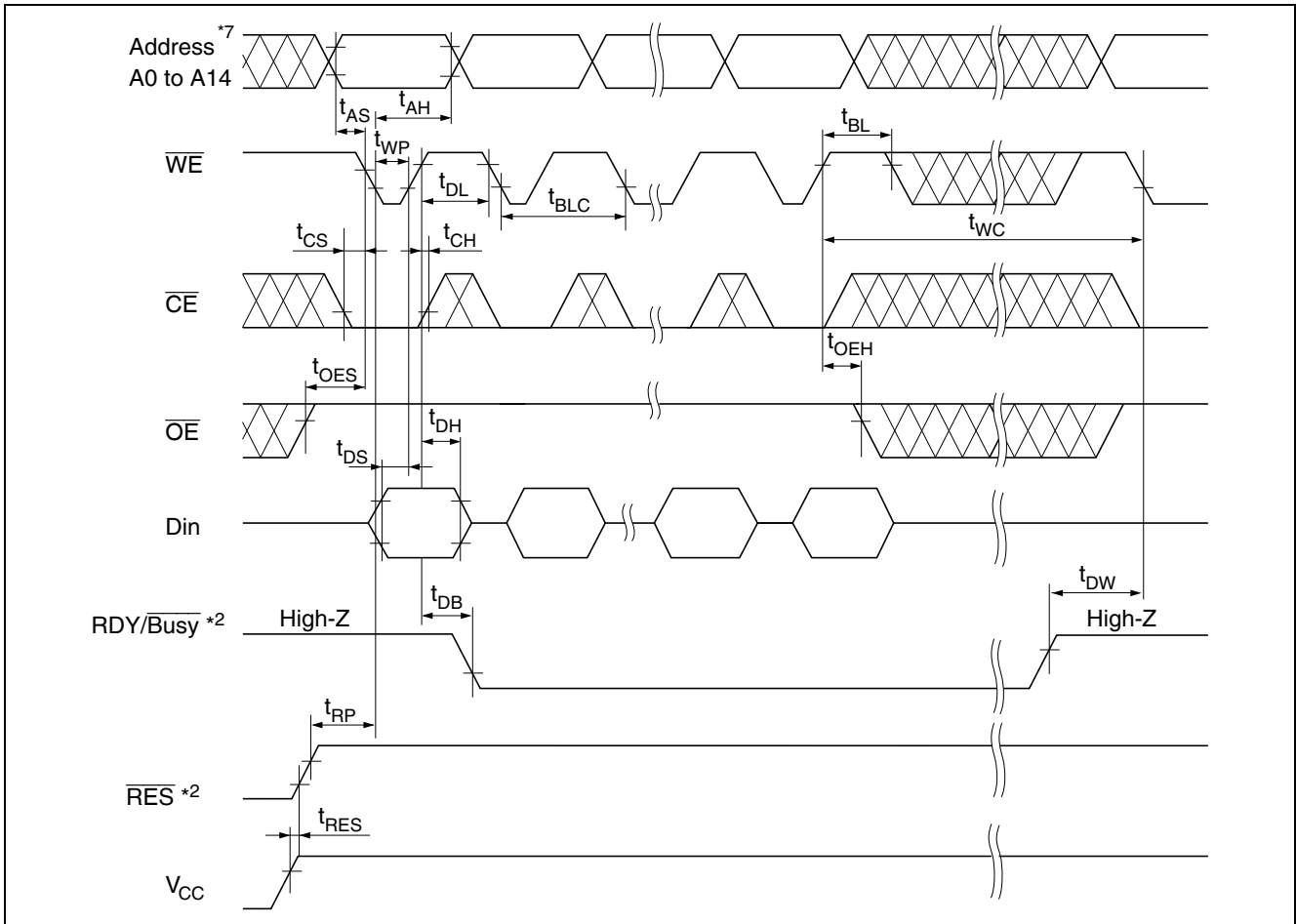
**Byte Write Timing Waveform (1) ( $\overline{WE}$  Controlled)**



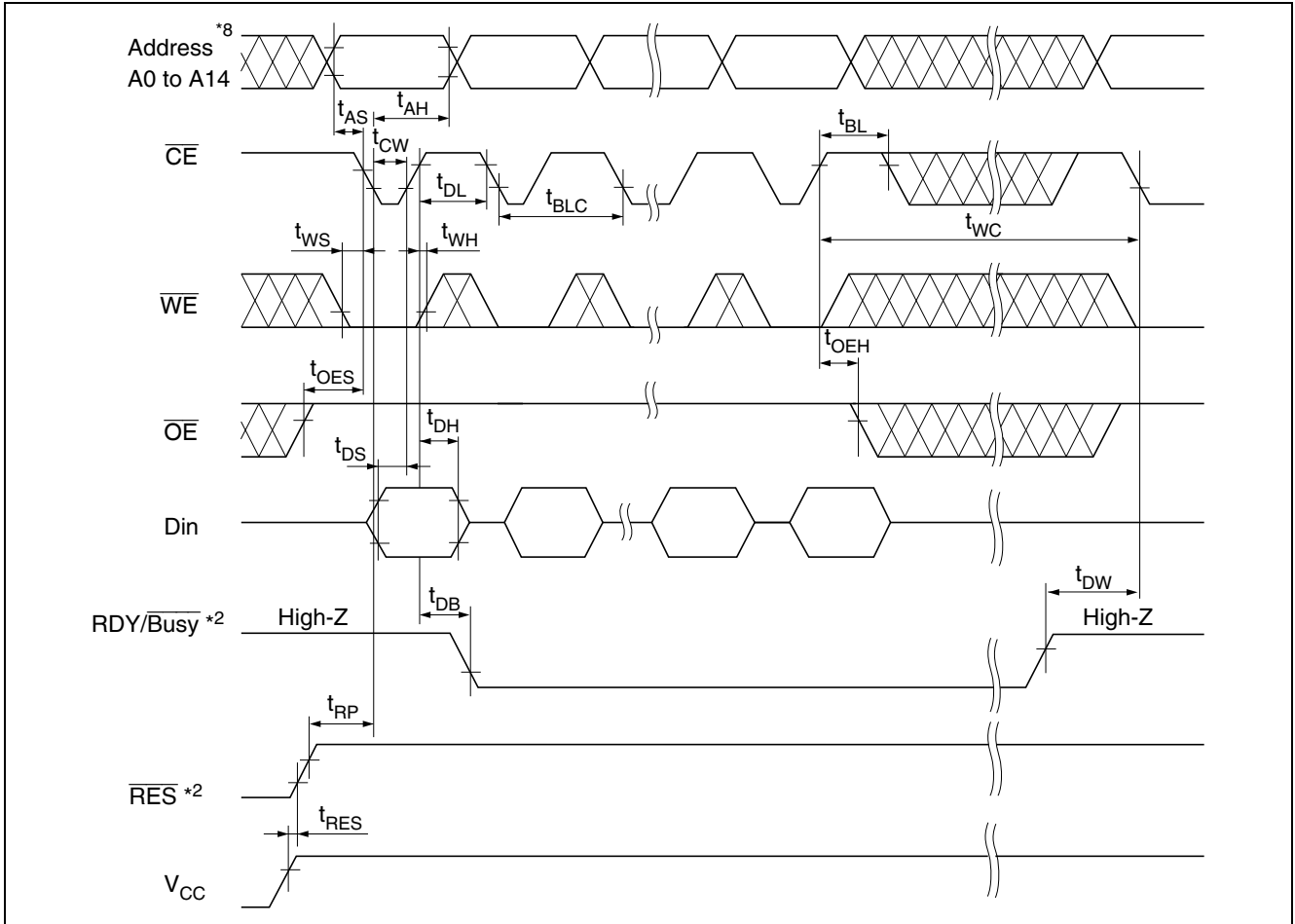
**Byte Write Timing Waveform (2) ( $\overline{\text{CE}}$  Controlled)**



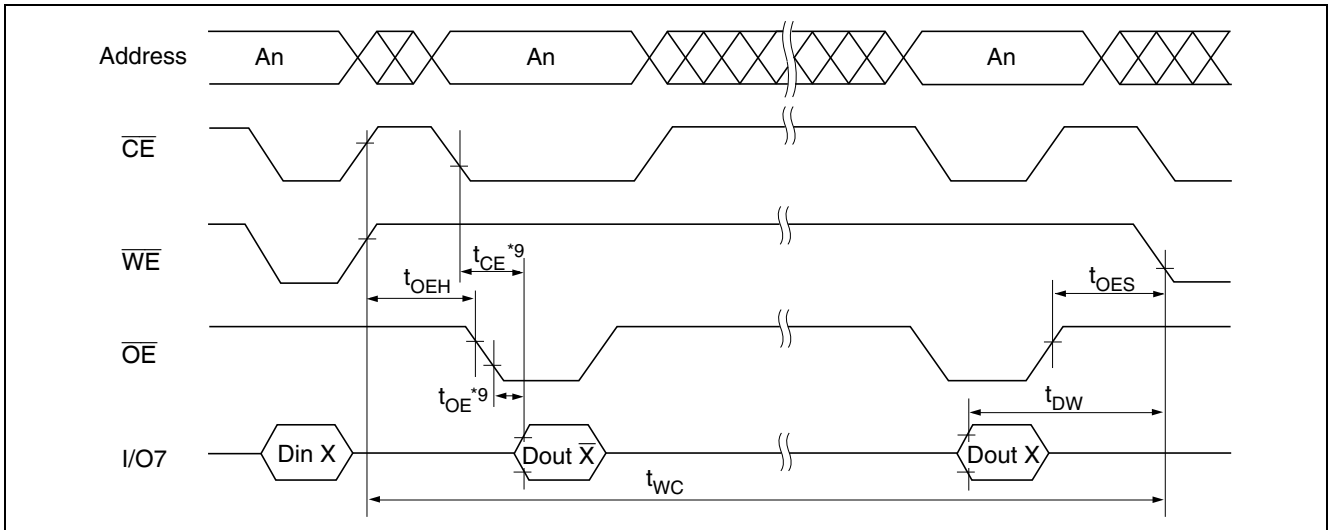
Page Write Timing Waveform (1) ( $\overline{WE}$  Controlled)



Page Write Timing Waveform (2) ( $\overline{\text{CE}}$  Controlled)



**Data Polling Timing Waveform**

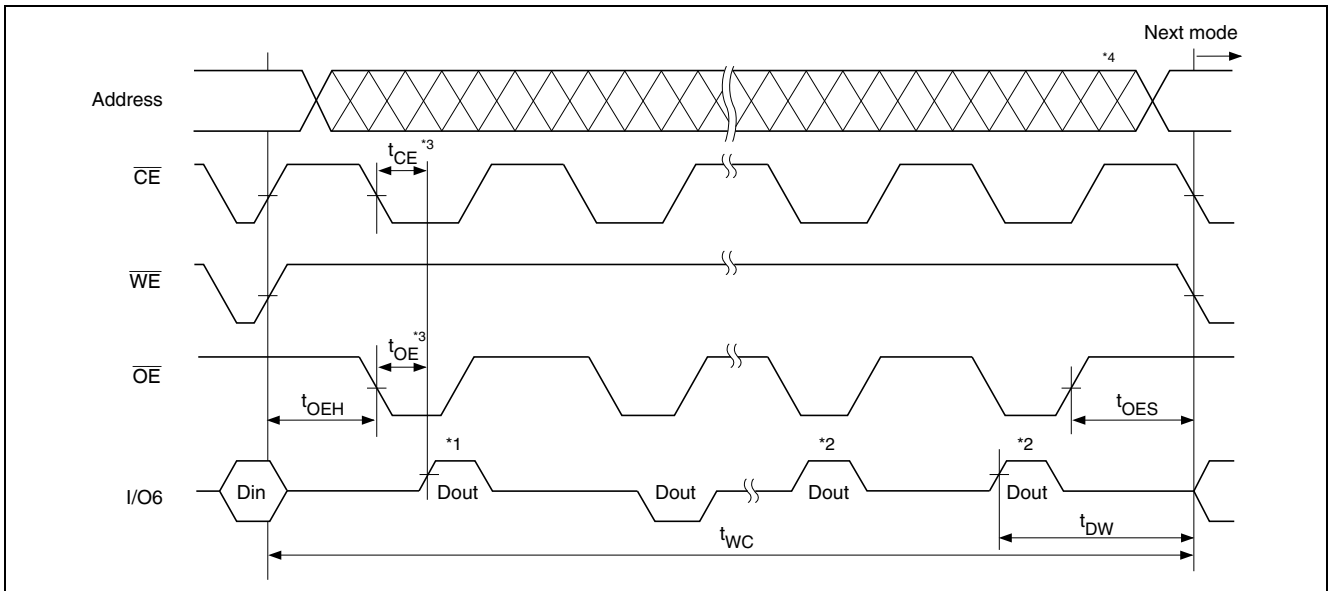


### Toggle bit

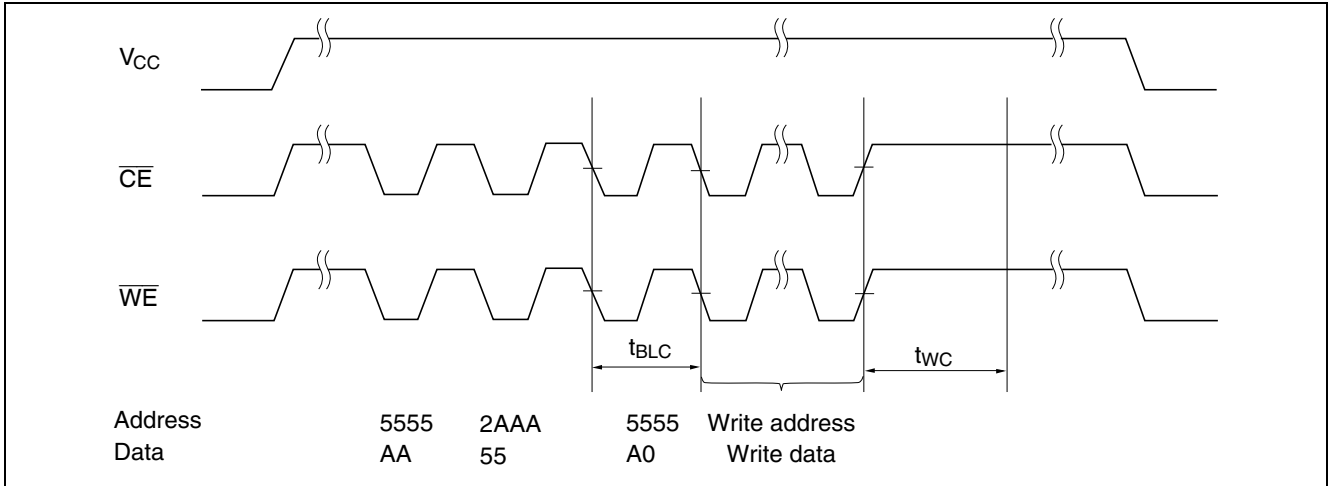
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (togglng) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

### Toggle bit Waveform

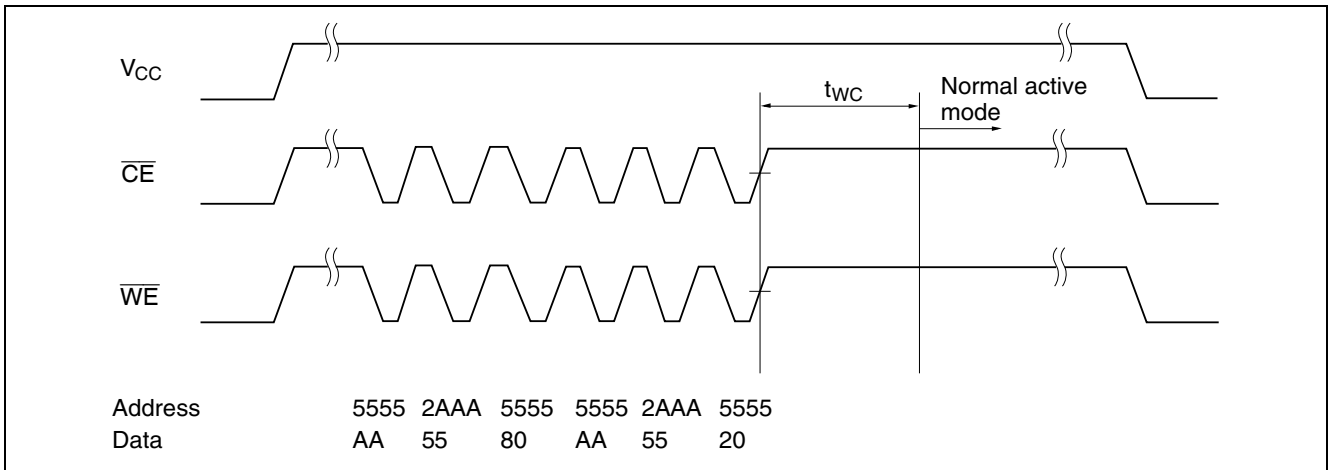
- Notes: 1. I/O6 beginning state is “1”.
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any address location can be used, but the address must be fixed.



**Software Data Protection Timing Waveform (1) (in protection mode)**



**Software Data Protection Timing Waveform (2) (in non-protection mode)**





## Functional Description

### Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30  $\mu$ s from the preceding falling edge of  $\overline{WE}$  or  $\overline{CE}$ . When  $\overline{CE}$  or  $\overline{WE}$  is high for 100  $\mu$ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

### Data Polling

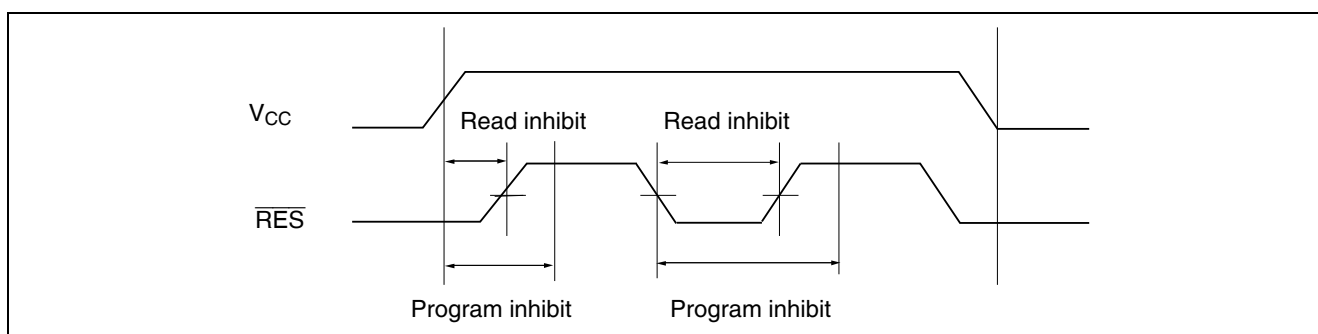
Data polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

### RDY/ $\overline{Busy}$ Signal (only the R1EV58256BxxR series)

RDY/ $\overline{Busy}$  signal also allows the status of the EEPROM to be determined. The RDY/ $\overline{Busy}$  signal has high impedance except in write cycle and is lowered to  $V_{OL}$  after the first write signal. At the end of a write cycle, the RDY/ $\overline{Busy}$  signal changes state to high impedance.

### $\overline{RES}$ Signal (only the R1EV58256BxxR series)

When  $\overline{RES}$  is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping  $\overline{RES}$  low when  $V_{CC}$  is switched.  $\overline{RES}$  should be high during read and programming because it doesn't provide a latch function.



### $\overline{WE}$ , $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , and data is latched by the rising edge of  $\overline{WE}$  or  $\overline{CE}$ .

### Write/Erase Endurance and Data Retention Time

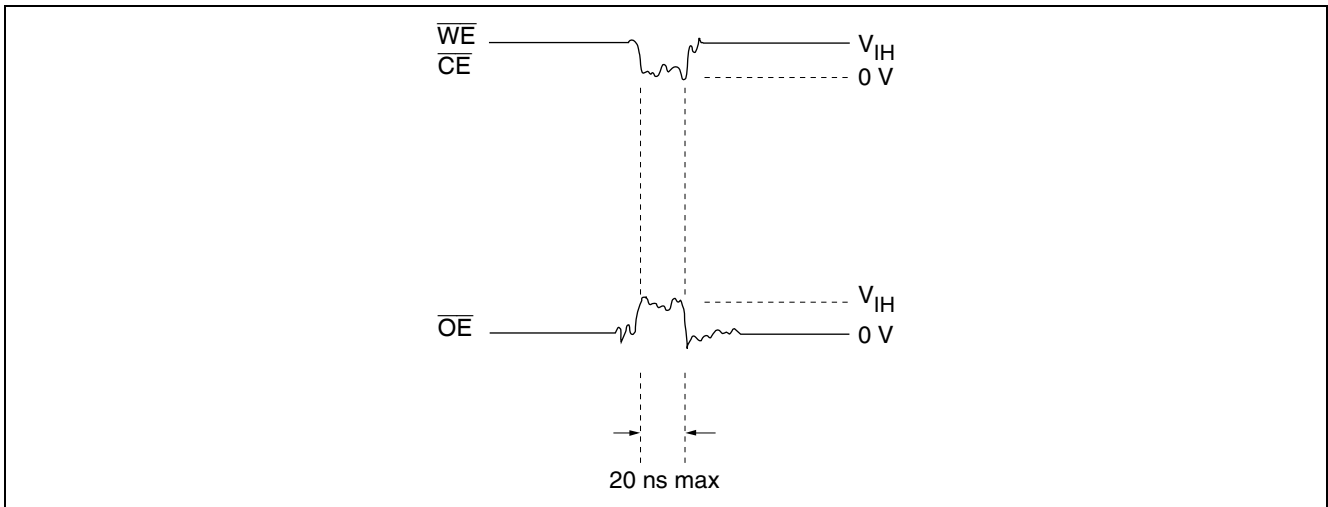
The endurance is  $10^5$  cycles (1% cumulative failure rate). The data retention time is more than 10 years.

## Data Protection

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less.

### 1. Data Protection against Noise on Control Pins ( $\overline{CE}$ , $\overline{OE}$ , $\overline{WE}$ ) during Operation

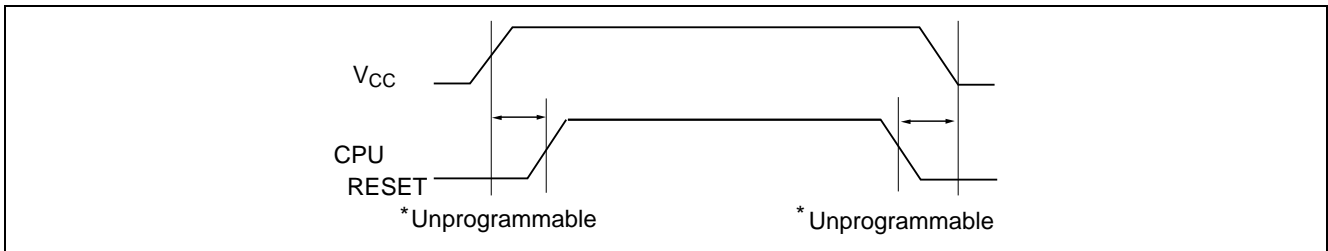
During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V<sub>CC</sub> On/Off

When V<sub>CC</sub> is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EPROM should be kept in unprogrammable state during V<sub>CC</sub> on/off by using CPU RESET signal.



2.1 Protection by  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

|                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|
| $\overline{CE}$ | V <sub>CC</sub> | x               | x               |
| $\overline{OE}$ | x               | V <sub>SS</sub> | x               |
| $\overline{WE}$ | x               | x               | V <sub>CC</sub> |

x: Don't care.

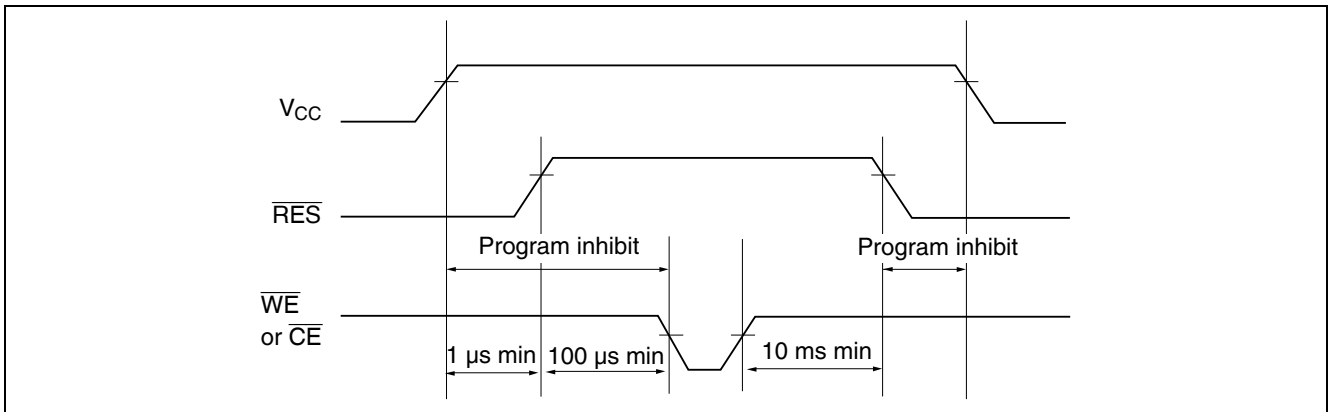
V<sub>CC</sub>: Pull-up to V<sub>CC</sub> level.

V<sub>SS</sub>: Pull-down to V<sub>SS</sub> level.

2.2 Protection by  $\overline{RES}$  (only the R1EV58256BxxR series)

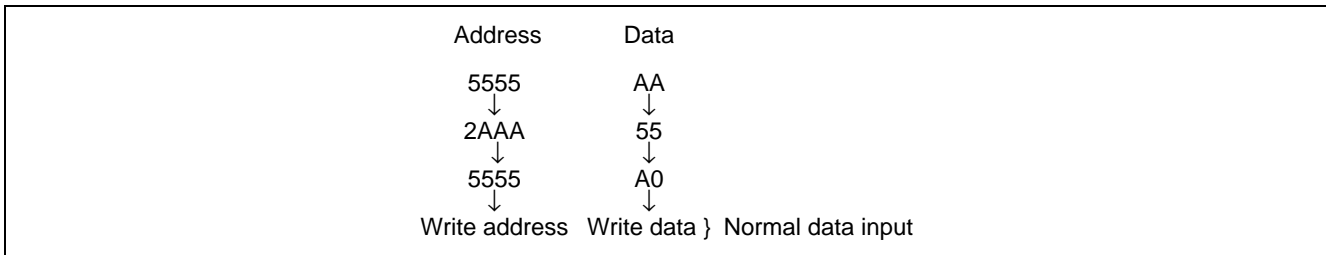
The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's  $\overline{RES}$  pin.  $\overline{RES}$  should be kept V<sub>SS</sub> level during V<sub>CC</sub> on/off.

The EEPROM breaks off programming operation when  $\overline{RES}$  becomes low, programming operation doesn't finish correctly in case that  $\overline{RES}$  falls low during programming operation.  $\overline{RES}$  should be kept high for 10 ms after the last data input.

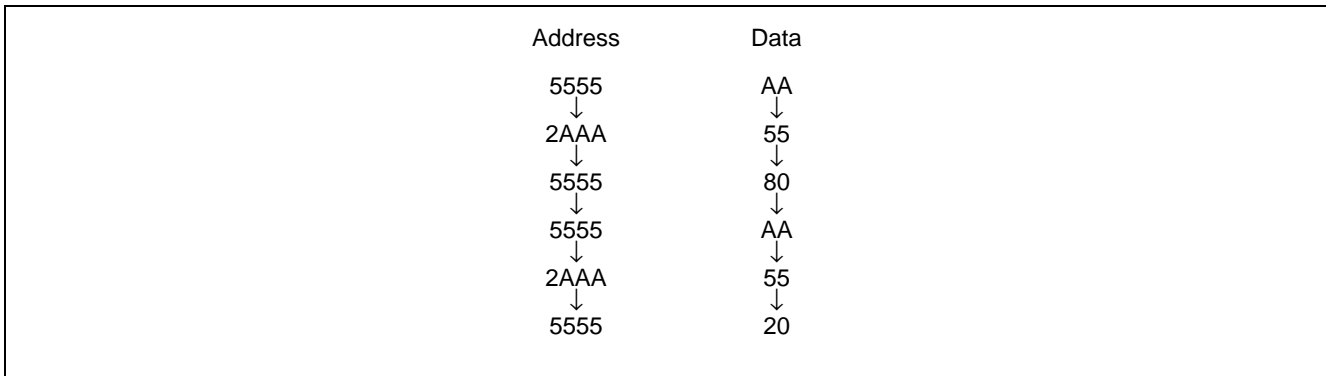


3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



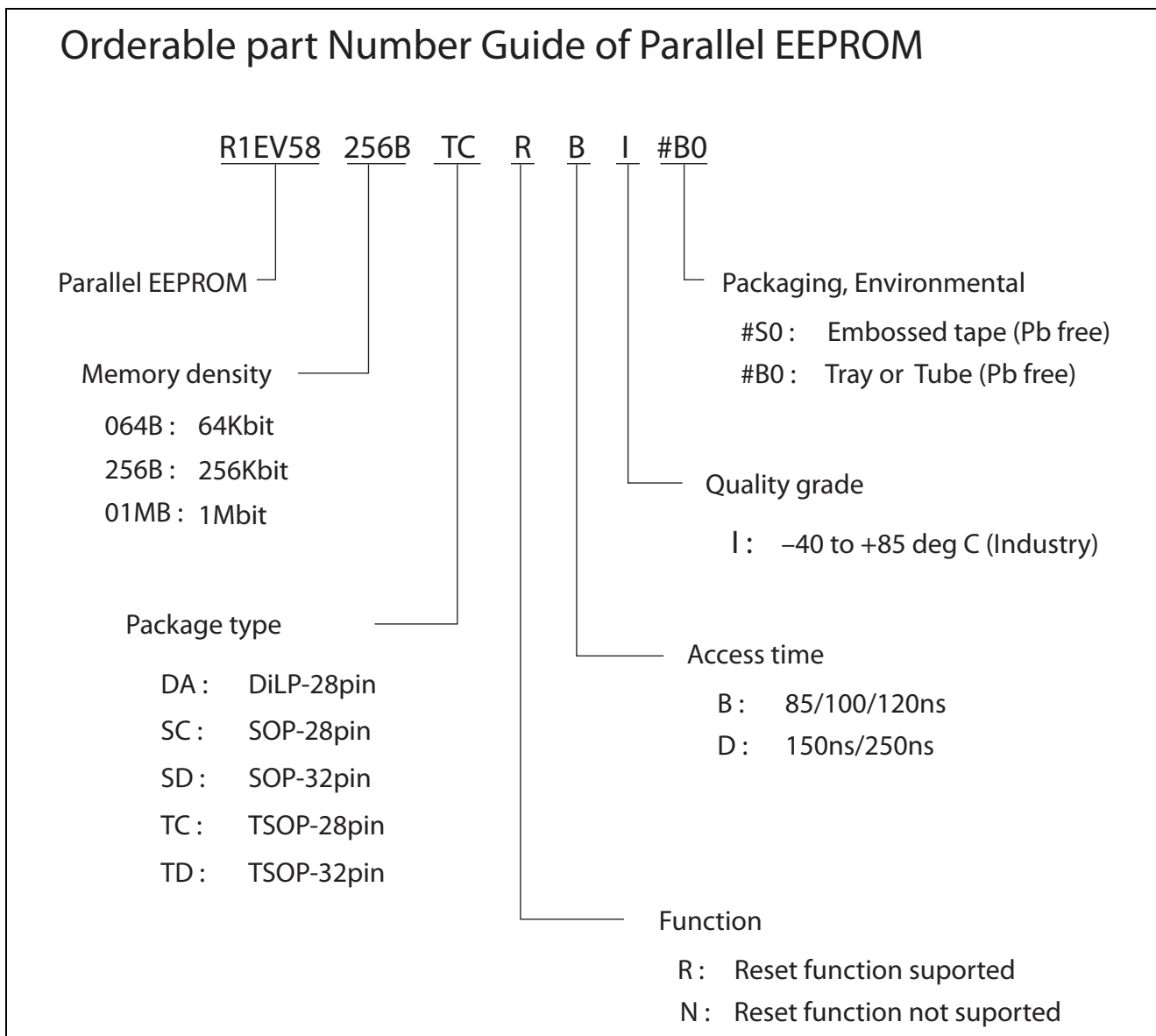
The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can not be written.



The software data protection is not enabled at the shipment.

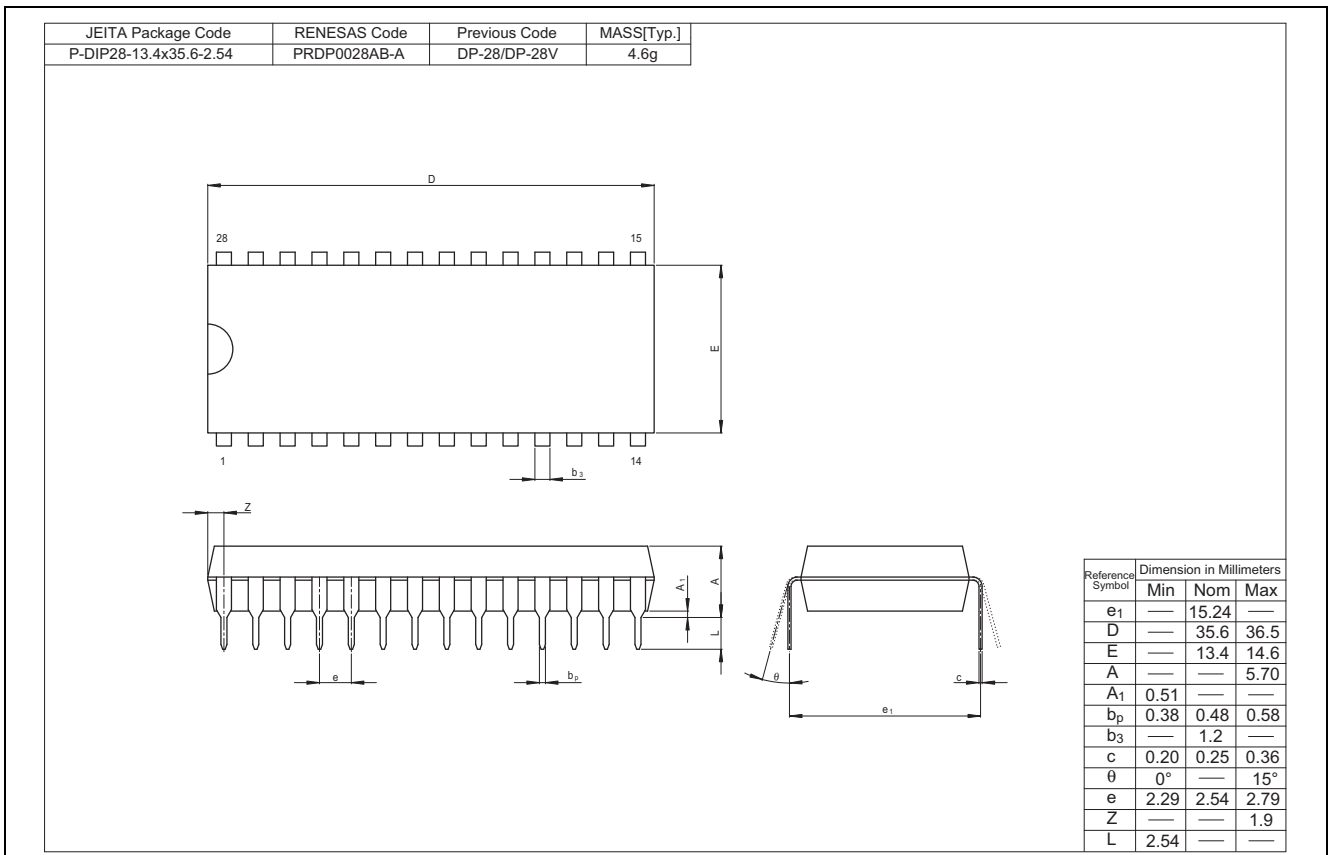
Note: There are some differences between Renesas Electronics' and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Renesas Electronics' sales offices.

### Orderable part Number Guide

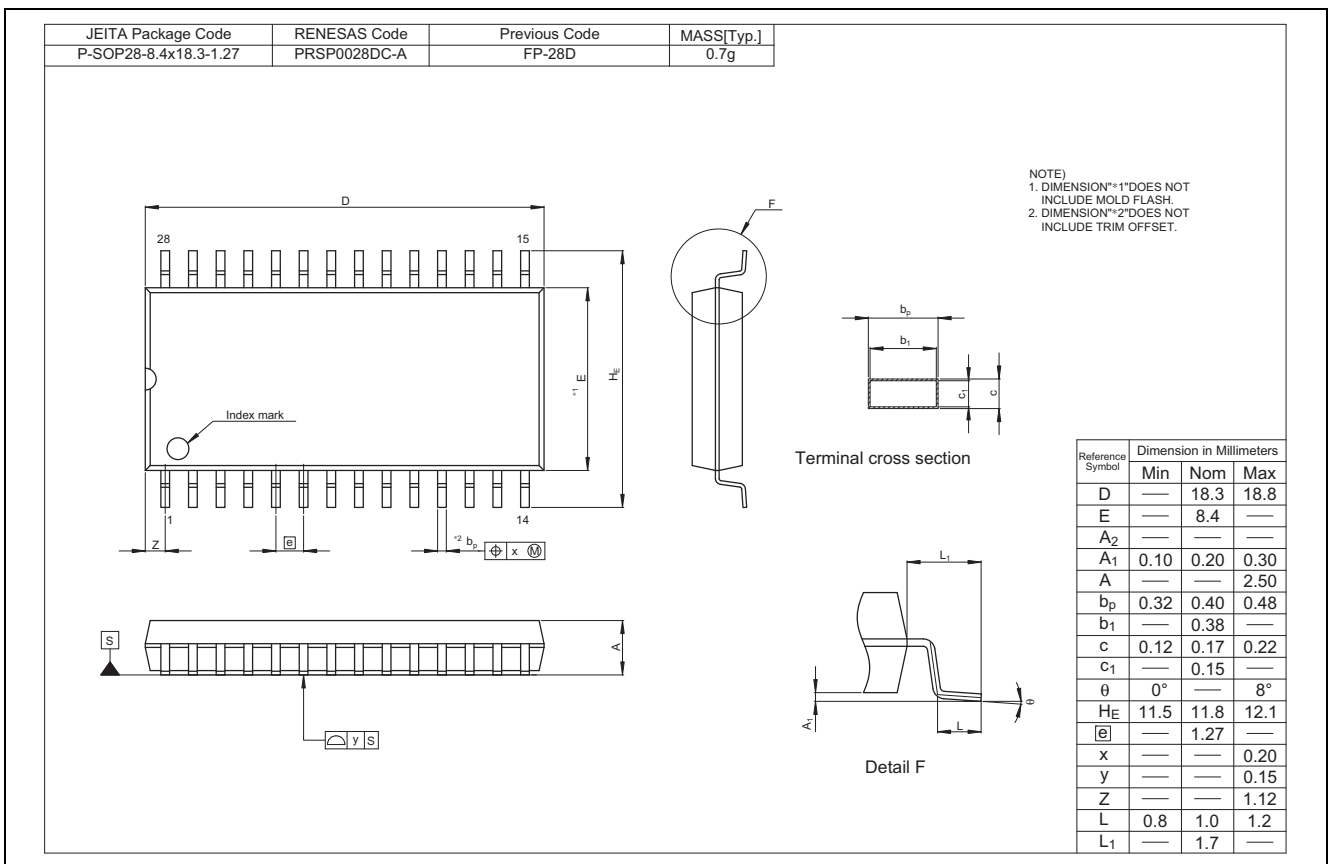


### Package Dimensions

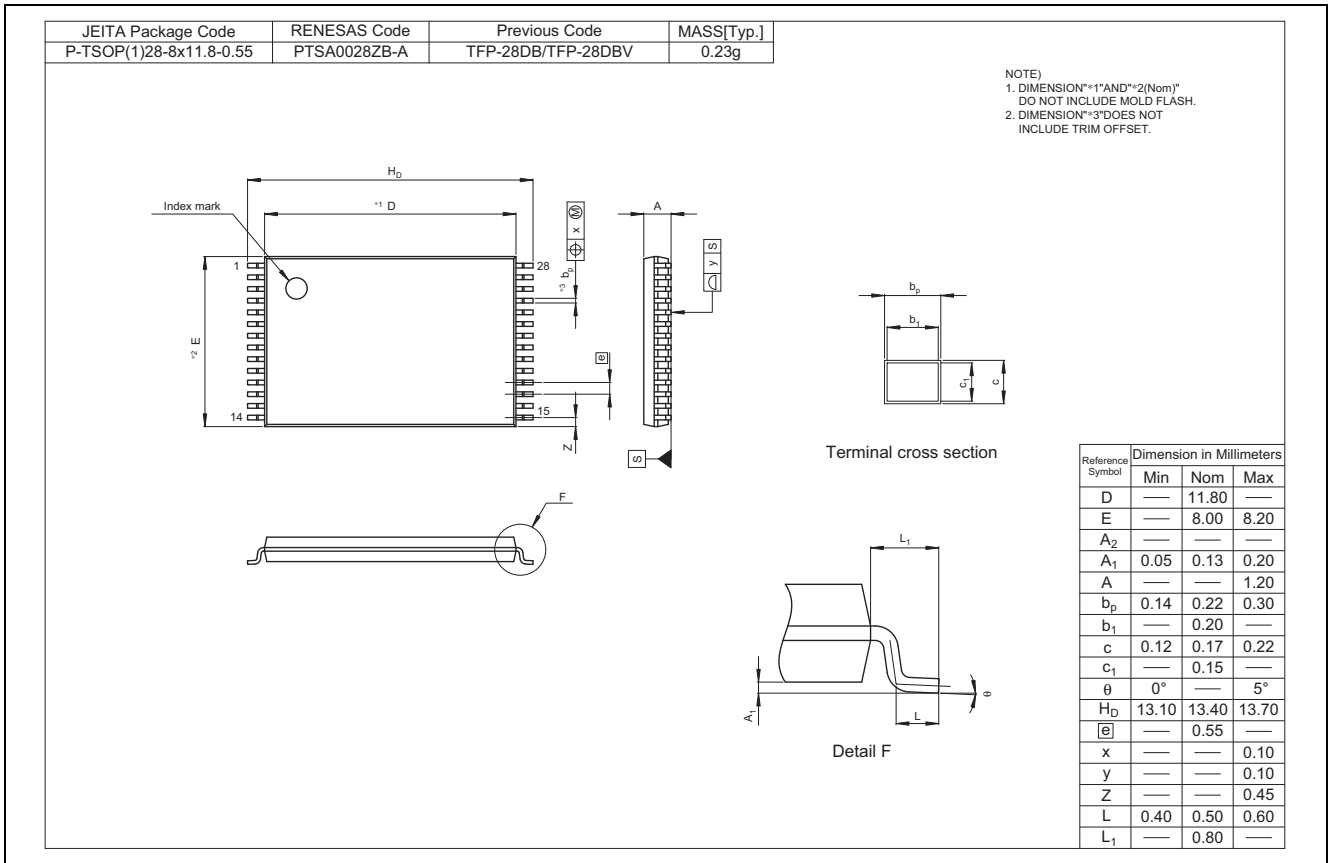
#### R1EV58256BDA Series (PRDP0028AB-A / Previous Code:DP-28DV)



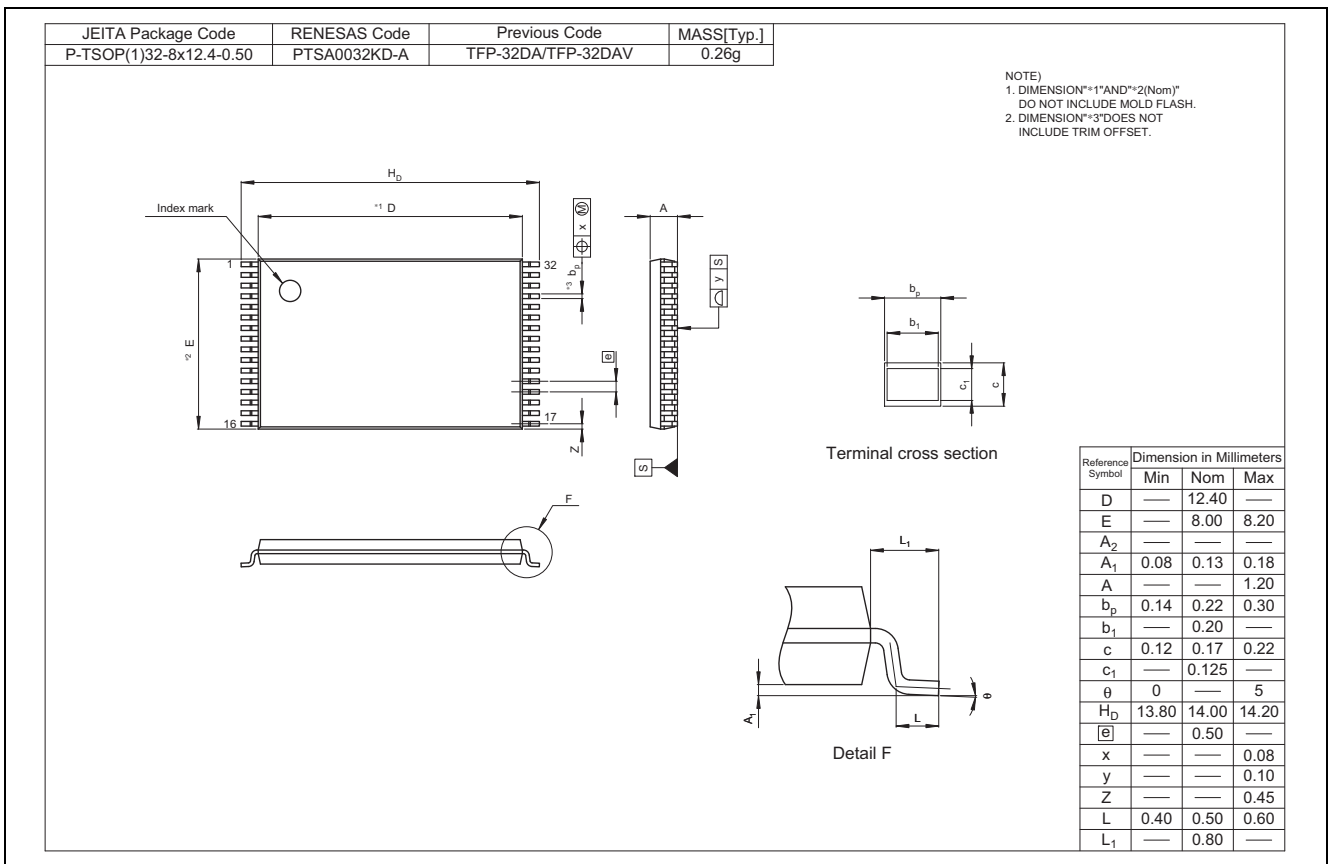
#### R1EV58256BSC Series (PRSP0028DC-A / Previous Code:FP-28DV)



**R1EV58256BTC Series (PTSA0028ZB-A / Previous Code : TFP-28DBV)**



**R1EV58256BTD Series (PTSA0032KD-A / Previous Code: TFP-32DAV)**



## Revision History

## R1EV58256BxxNSeries/R1EV58256BxxRSeries Data Sheet

| Rev. | Date         | Description |   |
|------|--------------|-------------|---|
|      |              | Page        | Summary   |
| 0.01 | Oct 17, 2013 | —           | Initial issue   |
| 0.02 | Oct 18, 2013 | 2           | Ordering Information: Addition of 85ns and 120ns for Access time.   |
|      |              | 5           | AC Characteristics: Deletion of 100ns spec for Read Cycle.  |
|      |              | 21          | Orderable part Number Guide: Deletion of A and C for access time.   |
| 0.03 | Nov 05, 2013 | 4           | Recommended DC Operating Conditions: Change $V_{IL(max)} = 0.6V$ to $0.8V$ .<br>Note 2: $V_{CC} = 3.6$ to $5.5 V$ is $2.4 V \rightarrow V_{CC} = 3.6$ to $5.5 V$ is $2.2 V$ |
| 1.00 | Jun 09, 2014 | —           | Delete preliminary  |
| 2.00 | May 12, 2016 | 4           | DC Operating Conditions: Addition of Note 5.  |
|      |              | 6           | AC Characteristics: Addition of Max. 30us for $\overline{WE}$ pulse width (tWP)<br>AC Characteristics: Addition of Max. 30us for $\overline{CE}$ pulse width (tCW)          |
|      |              | 8           | AC Characteristics: Addition of Max. 30us for $\overline{WE}$ pulse width (tWP)<br>AC Characteristics: Addition of Max. 30us for $\overline{CE}$ pulse width (tCW)          |
| 2.01 | Apr. 01,2020 | 2           | Revised ordering Information  |
|      |              | 5           | Operating VCC current:<br>Change "Cycle = 1 ns" to "Cycle = 1 $\mu$ s", "Cycle = 120 $\mu$ s" to "Cycle = 120ns"  |
|      |              | Last page   | Updated the Notice to the latest version  |



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(Rev.4.0-1 November 2017)

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