Description

The P9221-R3 is a high efficiency 15W magnetic induction wireless power receiver with in-band, bi-directional data communication with no additional circuitry. The communication channel can be used for proprietary device authentication and secure system data transfer.

The P9221-R3 integrates a 32-bit ARM® Cortex® -M0 processor*, low-RDS(ON) synchronous rectifier, and ultra-low dropout regulator making it ideal for high-efficiency, space-constrained receiver applications. The device features a programmable output voltage, current limitation, and foreign-object detection (FOD) settings. An I2C serial interface allows reading information such as voltage, current, and fault conditions. The device also features a patented over-voltage protection scheme eliminating the need for additional capacitors, which can minimize the external component count and cost. Combined with the P9242-R3 transmitter, the P9221-R3 forms a complete wireless power system solution for 15W applications with bi-directional communication.

The P9221-R3 is provided in a 52-WLCSP package (2.64 × 3.94 mm, 0.4mm pitch), and it is rated for a 0 to 85°C ambient operating temperature range.

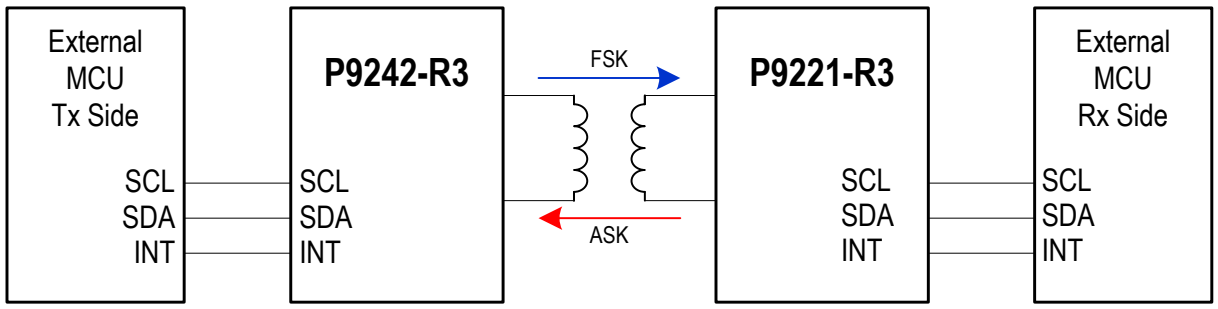
Features

- Supports bi-directional data communication
- Enables authentication and system data transfer
- Single-chip solution supporting applications with up to 15W
- Patented over-voltage protection clamp eliminating external capacitors
- 87% peak DC-to-DC efficiency when combined with the IDT P9242-R3
- Programmable output voltage and current limit
- Embedded 32-bit ARM® Cortex®-M0 processor
- Dedicated remote temperature sensing
- Standard device compliant with WPC-1.2 specification
- Supports I2C interface
- 0 to +85°C ambient operating temperature range
- WLCSP 2.64 × 3.94 mm, 52-WLCSP package

Typical Applications

- Industrial equipment
- Consumer electronics
- Medical equipment

Typical Application Circuit



* ARM® and Cortex® are trademarks of ARM, LTD.

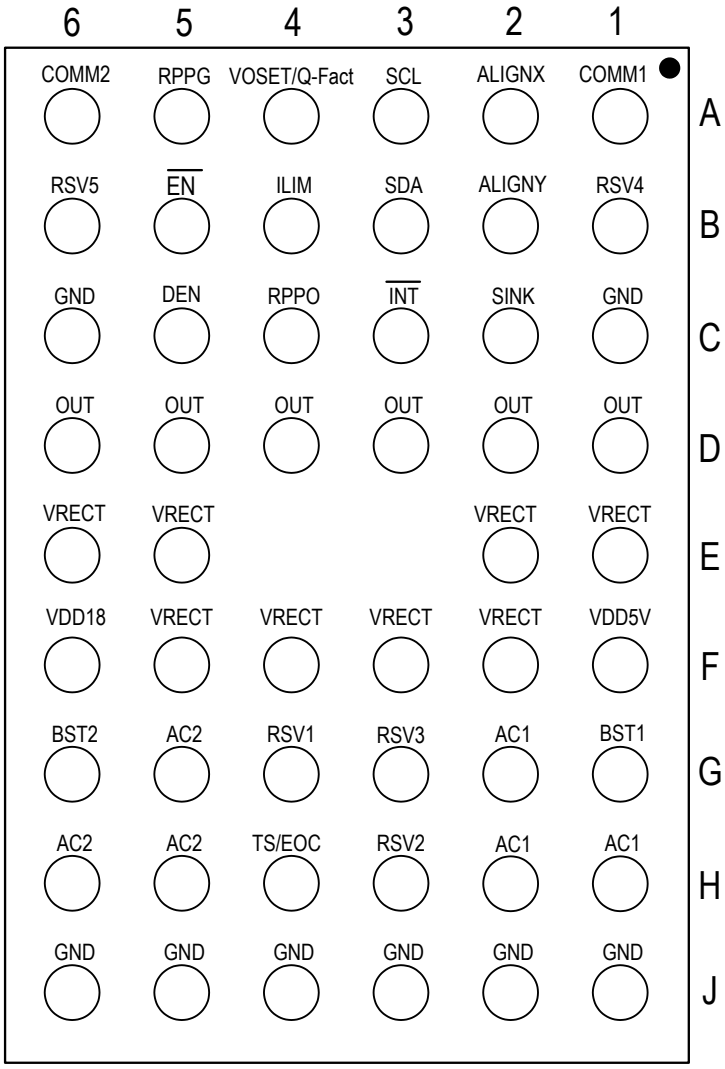
Contents

List of Figures

List of Tables

1. Pin Assignments

Figure 1. Pin Assignments – Bottom View



Bottom View

2. Pin Descriptions

Table 1. Pin Descriptions

Pins	Name	Type	Function
A1	COMM1	Output	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC1 to COMM1.
A2	ALIGNX	Input	AC input for coil alignment guide. If not used, connect this pin to GND through a 10kΩ resistor.
A3	SCL	Input	Serial clock line. Open-drain pin. Connect this pin to a 5.1kΩ resistor to the VDD18 pin.
A4	VOSET/ Q-Fact	Input	Programming pin for setting the output voltage and Q-factor. For VOSET, connect this pin to the center tap of a resistor divider to set the output voltage. For more information, refer to section 8.2 for different output voltage settings. Also see section 8.2 for adjusting the Q-factor value.
A5	RPPG	Input	Received power packet gain (RPPG) calibration pin for foreign object detection (FOD) tuning. Connect this pin to the center tap of a resistor divider to set the gain of the FOD. The FOD is disabled by connecting the RPPG and RPPO pins to GND. Do not leave this pin floating.
A6	COMM2	Output	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC2 to COMM2.
B1	RSV4	–	Reserved for internal use. Do not connect.
B2	ALIGNY	Input	AC input for coil alignment guide. If not used, connect to GND through a 10kΩ resistor.
B3	SDA	Input/Output	Serial data line. Open-drain pin. Connect a 5.1kΩ resistor to VDD18 pin.
B4	ILIM	Input	Programmable over-current limit pin. Connect this pin to the center tap of a resistor divider to set the current limit. For more information about the current limit function, see section 8.5.
B5	$\overline{EN}$	Input	Active-LOW enable pin. Pulling this pin to logic HIGH forces the device into Shut Down Mode. When connected to logic LOW, the device is enabled. Do not leave this pin floating.
B6	RSV5	–	Reserved for internal use. Do not connect.
C1, C6, J1, J2, J3, J4, J5, J6	GND	GND	Ground.
C2	SINK	Output	Open-drain output for controlling the rectifier clamp. Connect a 36Ω resistor from this pin to the VRECT pin.
C3	$\overline{INT}$	Output	Interrupt flag pin. This is an open-drain output that signals fault interrupts. It is pulled LOW if any of these faults exist: an over-voltage is detected, an over-current condition is detected, the die temperature exceeds 140°C, or an external over-temperature condition is detected on the TS/EOC pin. $\overline{INT}$ is also pulled LOW, if the device receives user data from a P9242-R3. It is also asserted LOW when $\overline{EN}$ is HIGH. Connect $\overline{INT}$ to VDD18 through a 10kΩ resistor. See section 8.6 for additional conditions affecting the interrupt flag.
C4	RPPO	Input	Received power packet offset (RPPO) calibration pin for FOD tuning. Connect this pin to the center tap of the resistor divider to set the offset of the FOD. The FOD is disabled by connecting the RPPG and RPPO pins to GND. Do not leave this pin floating.

Pins	Name	Type	Function
C5	DEN	Input	Reserved. A10kΩ resistor must be connected between the DEN pin and the VDD18 pin.
D1, D2, D3, D4, D5, D6	OUT	Output	Regulated output voltage pin. Connect two 10µF capacitors from this pin to GND. The default voltage is set to 12V when the VOSET/Q-Fact pin is pulled up to the VDD18 pin through a 10kΩ resister. For more information about the VOSET function, see section 8.2.
E1, E2, E5, E6, F2, F3, F4, F5	VRECT	Output	Output voltage of the synchronous rectifier bridge. Connect three 10µF capacitors and a 0.1µF capacitor in parallel to GND. The rectifier voltage dynamically changes as the load changes. For more information, see the typical waveforms in section 6.
F1	VDD5V	Output	Internal 5V regulator output voltage for internal use. Connect a 1µF capacitor from this pin to ground. Do not load the pin.
F6	VDD18	Output	Internal 1.8V regulator output voltage. Connect a 1µF capacitor from this pin to ground. Do not load the pin.
G1	BST1	Output	Boost capacitor for driving the high-side switch of the internal rectifier. Connect a 15nF capacitor from the AC1 pin to BST1.
G2, H1, H2,	AC1	Input	AC input power. Connect these pins to the resonant capacitance C_S (C1, C2, C3, and C5 in Figure 28).
G3	RSV3	Input	Reserved pin. This pin must be connected to the OUT pin. Do not leave this pin floating.
G4	RSV1	–	Reserved for internal use. Do not connect.
G5, H5, H6	AC2	Input	AC input power. Connect these pins to the Rx coil (L1).
G6	BST2	Output	Boost capacitor for driving the high-side switch of the internal rectifier. Connect a 15nF capacitor from the AC2 pin to BST2.
H3	RSV2	–	Reserved pin. This pin must be connected to the OUT pin. Do not leave this pin floating.
H4	TS/EOC	Input	End-of-Charge (EOC) signal and remote temperature (TS) sensing for over-temperature shutdown. For remote temperature sensing, connect to a negative temperature coefficient (NTC) thermistor network. If not used, connect this pin to VDD18 pin through a 10kΩ resistor. For EOC, connecting the pin to ground will send the End Power Transfer (EPT) packet to the transmitter to terminate the power. For more information, refer to section 8.9.

3. Absolute Maximum Ratings

Stresses greater than those listed as absolute maximum ratings in Table 2 could cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods might affect reliability.

Table 2. Absolute Maximum Ratings

Pins [a], [b]	Parameter	Conditions	Minimum [c]	Maximum [c]	Units
AC1 [d], AC2 [d], COMM1, COMM2	Absolute Maximum Pin Voltage		-0.3	20	V
$\overline{EN}$	Absolute Maximum Pin Voltage		-0.3	28	V
SINK, VRECT	Absolute Maximum Pin Voltage		-0.3	24	V
DEN, ILIM, RPPG, RPPO, VDD18, VOSET/Q-Fact	Absolute Maximum Pin Voltage		-0.3	2	V
ALIGNX, ALIGNY, $\overline{INT}$, SCL, SDA, TS/EOC, VDD5V	Absolute Maximum Pin Voltage		-0.3	6	V
BST1	Absolute Maximum Pin Voltage		-0.3	AC1 + 6	V
BST2	Absolute Maximum Pin Voltage		-0.3	AC2 + 6	V
OUT	Absolute Maximum Pin Voltage		-0.3	14.4	V
SINK	Maximum Current on Pin		–	1	A
COMM1, COMM2	Maximum RMS Current on Pin		–	500	mA
AC1, AC2	Maximum RMS Current from Pin		–	2	A

[a] Absolute maximum ratings are not provided for reserved pins (RSV1, RSV2, RSV3, RSV4, RSV5, and DEN). These pins are not used in the application.

[b] For the test conditions for the absolute maximum ratings specifications, the P9221-R3 characterization for the operating ambient temperature (T_{AMB}) specification (see Table 4) has been performed down to -10°C only. Design simulation indicates normal operation down to -45°C. Limited bench functionality tests indicate normal operation down to -40°C.

[c] All voltages are referred to ground unless otherwise noted.

[d] During synchronous rectifier dead time, the voltage on the AC1 and AC2 pins is developed by the current across the internal power FET's body diodes, and it might be lower than -0.3 V. This is a normal behavior and does not negatively impact the functionality or reliability of the product.

Table 3. ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins except RSV1, RSV2, RSV3, RSV4, and RSV5 pins	2	kV
	RSV1, RSV2, RSV3, RSV4, and RSV5 pins	1	kV
CDM	All pins	500	V

4. Thermal Characteristics

Table 4. Package Thermal Information

Note: This thermal rating was calculated on a JEDEC 51 standard 4-layer board with dimensions 76.2 x 114.3 mm in still air conditions.

Symbol	Description	WLCSP Rating 8 Thermal Balls	Units
θ_{JA}	Thermal Resistance Junction to Ambient[a]	47	°C/W
θ_{JC}	Thermal Resistance Junction to Case	0.202	°C/W
θ_{JB}	Thermal Resistance Junction to Board	4.36	°C/W
T_J	Operating Junction Temperature[a]	-5 to +125	°C
T_{AMB}	Ambient Operating Temperature[a]	0 to +85	°C
T_{STOR}	Storage Temperature	-55 to +150	°C
T_{BUMP}	Maximum Soldering Temperature (Reflow, Pb-Free)	260	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_{AMB}) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown. Refer to section 13.1 for further details.

5. Electrical Characteristics

Table 5. Electrical Characteristics

Note: VRECT = 5.5V; C_{OUT} = 4.7µF, $\overline{EN}$ = LOW, unless otherwise noted. T_J = 0°C to 125°C; typical values are at 25°C.

Note: See important notes at the end of this table.

Symbol	Description	Conditions	Min	Typical	Max	Units
Under-Voltage Lock-Out (UVLO)						
V_{UVLO_Rising}	UVLO Rising	Rising voltage on VRECT		2.9	2.98	V
V_{UVLO_HYS}	UVLO Hysteresis	VRECT falling		200		mV
Over-Voltage Protection						
V_{OVP-DC}	DC Over-Voltage Protection	Rising voltage on VRECT		17		V
$V_{OVP-HYS}$	Over-Voltage Hysteresis			1		V
Quiescent Current						
I_{ACTIVE_SUPLY}	Supply Current	$\overline{EN}$ = Low, No load; VRECT = 12.3V		3.0		mA
I_{SHD}	Shut Down Mode Current	$\overline{EN}$ = High; VRECT = 12.3V		500		µA
VDD18 Voltage						
V_{VDD18}	VDD18 Pin Output Voltage[a]	I_{VDD18} = 10mA, C_{VDD18} = 1µF	1.62	1.8	1.98	V

Symbol	Description	Conditions	Min	Typical	Max	Units
VDD5V Voltage						
V_{VDD5V}	VDD5V Pin Output Voltage [a]	I_{VDD5V} = 10mA, C_{VDD5V} = 1µF	4.5	5	5.5	V
Low Drop-Out (LDO) Regulator						
I_{OUT_MAX}	Maximum Output Current			1.25		A
V_{OUT_12V}	12V Output Voltage	VOSET/Q-Fact > 1.5V, VRECT = 12.3V		12		V
V_{OUT_9V}	9V Output Voltage	0.7V < VOSET/Q-Fact < 1.2V, VRECT = 9.3V		9		V
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			67.5		kSa/s
Channel	Number of Channels			8		
$V_{IN,FS}$	Full-Scale Input Voltage			2.1		V
$\overline{EN}$ pin						
$V_{IH\_\overline{EN}}$	Input Threshold HIGH		1.4			V
$V_{IL\_\overline{EN}}$	Input Threshold LOW				0.25	V
$I_{IL\_\overline{EN}}$	Input Current LOW	$V_{\overline{EN}}$ = 0V	-1		1	µA
$I_{IH\_\overline{EN}}$	Input Current HIGH	$V_{\overline{EN}}$ = 5V		2.5		µA
VOSET/Q-Fact, ILIM, TS/EOC, RPPO, RPPG						
I_{IL}	Input Current LOW	V_{VOSET}, V_{ILIM}, V_{TS}, V_{RPPO}, V_{RPPG} = 0V	-1		1	µA
I_{IH}	Input Current HIGH	V_{VOSET}, V_{ILIM}, V_{TS}, V_{RPPO}, V_{RPPG} = 1.8V	-1		1	µA
ALIGNX, ALIGNY, and $\overline{INT}$ pins						
I_{LKG}	Input Leakage Current	V_{ALIGNX}, V_{ALIGNY}, $V_{\overline{INT}}$ = 0V and 5V	-1		1	µA
V_{OL}	Output Logic LOW	I_{OL} = 8mA			0.36	V
I2C Interface – SCL, SDA						
V_{IL}	Input Threshold LOW				0.7	V
V_{IH}	Input Threshold HIGH		1.4			V
I_{LKG}	Input Leakage Current	V_{SCL}, V_{SDA} = 0V and 5V	-1		1	µA
V_{OL}	Output Logic LOW	I_{OL} = 8mA			0.36	V
f_{SCL}	Clock Frequency				400	kHz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			µs

Symbol	Description	Conditions	Min	Typical	Max	Units
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for SCL and SDA			150		pF
C_I	SCL and SDA Input Capacitance			5		pF
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Rising[b]		140		°C
		Falling		120		°C

[a] Do not externally load. For internal biasing only.

[b] If the die temperature exceeds 130°C, the *Thermal_SHTDN_Status* flag is set to “1”and an End Power Transfer (EPT) packet is sent (see Table 14).

6. Typical Performance Characteristics

The following performance characteristics were taken using the P9242-R3 15W Wireless Power Transmitter at T_{AMB} = 25°C unless otherwise noted.

Figure 2. Efficiency vs. Output Load: V_{OUT} = 12V

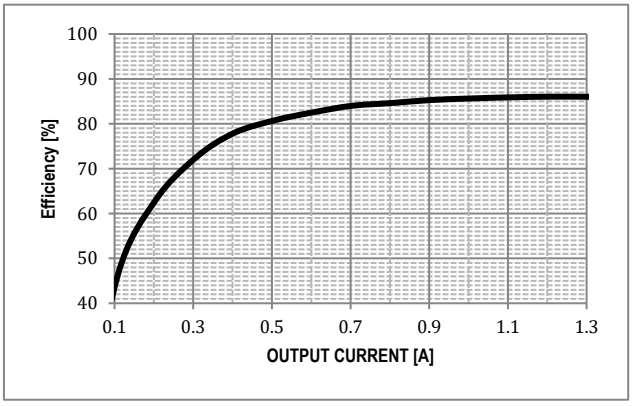


Figure 3. Load Reg. vs. Output Load: V_{OUT} = 12V

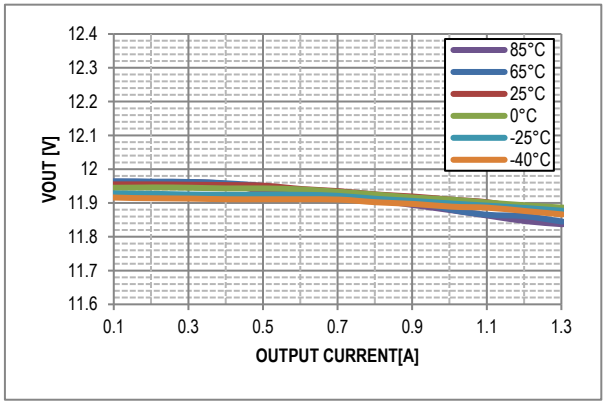


Figure 4. Efficiency vs. Output Load: V_{OUT} = 9V

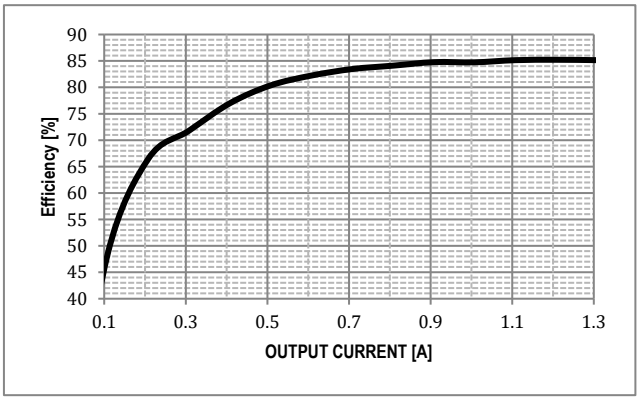


Figure 5. Load Reg. vs. Output Load: V_{OUT} = 9V

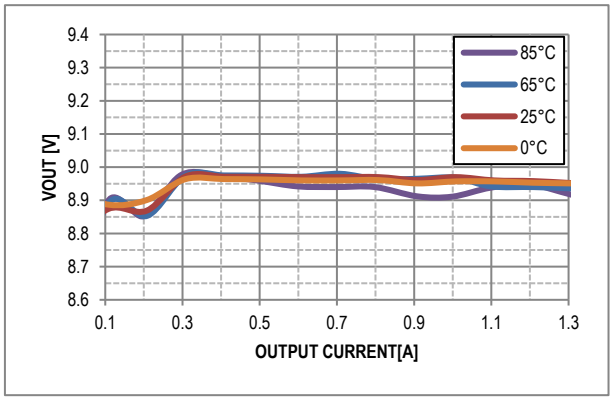


Figure 6. Efficiency vs. Output Load: V_{OUT} = 5V

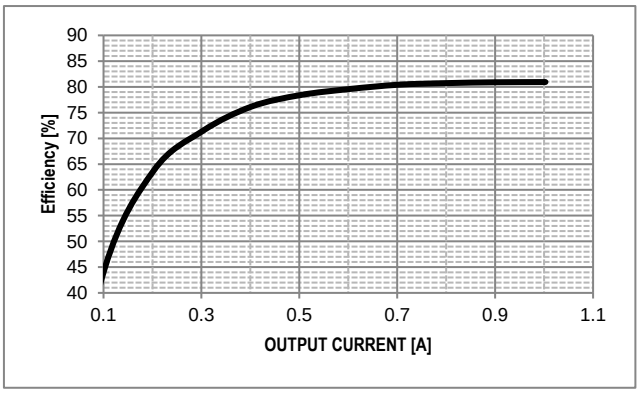


Figure 7. Load Reg. vs. Output Load: V_{OUT} = 5V

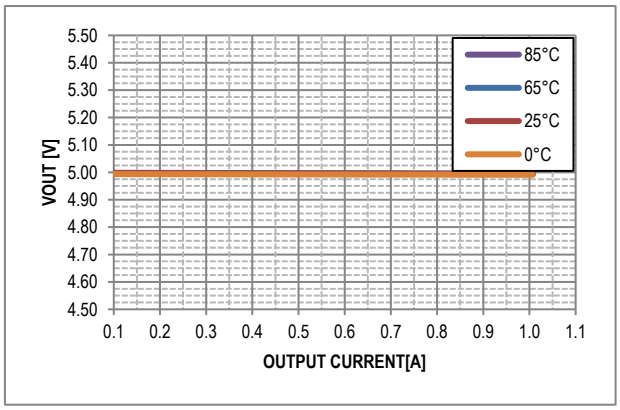


Figure 8. Rectifier Voltage vs. Load: V_{OUT} = 12V

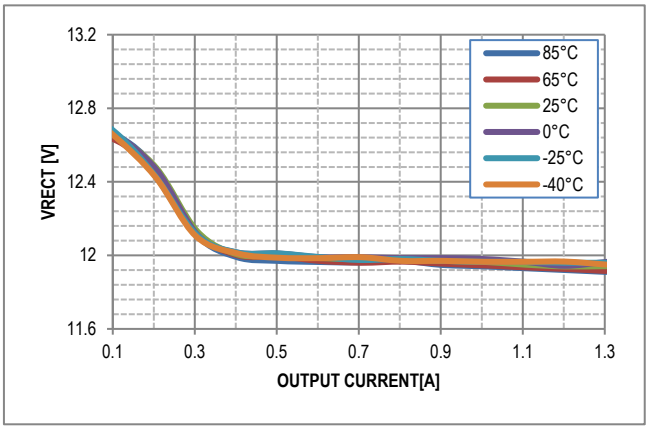


Figure 9. Rectifier Voltage vs. Load: V_{OUT} = 9V

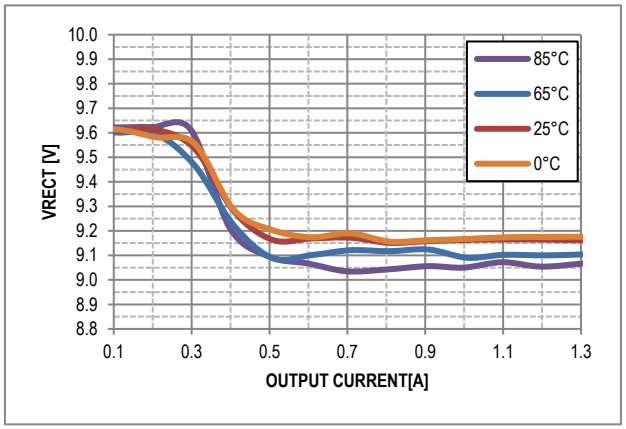


Figure 10. Rectifier Voltage vs. Load: V_{OUT} = 5V

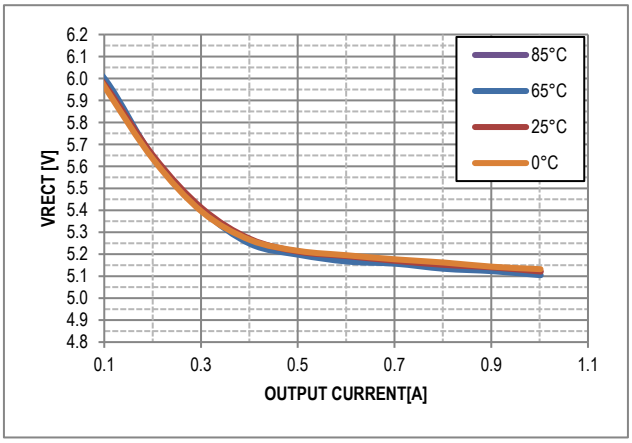


Figure 11. Current Limit vs. V_{ILIM}

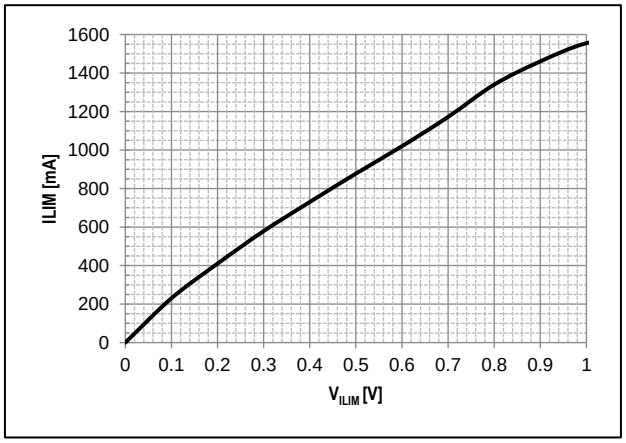


Figure 12. X and Y Misalignment

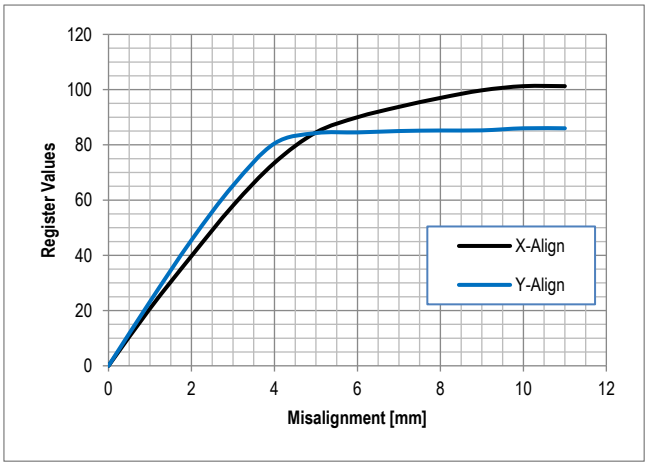


Figure 13. Max. Power vs. Misalignment: V_{OUT} = 12V

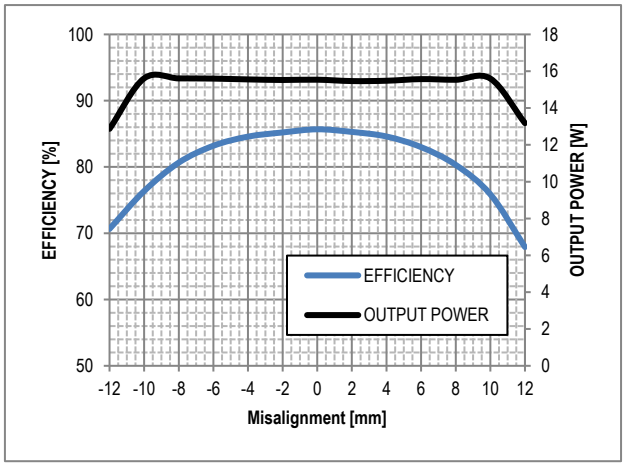


Figure 14. Enable Startup: V_{OUT} = 12V; I_{OUT} = 1.2A

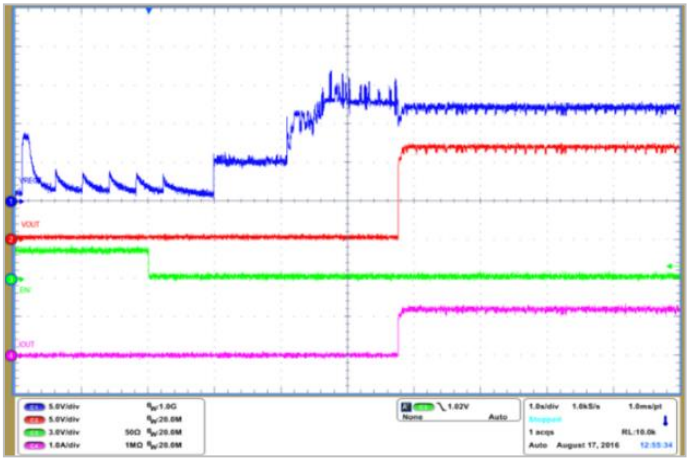


Figure 15. Transient Resp: V_{OUT} = 12V; I_{OUT} = 0 to 1.2A

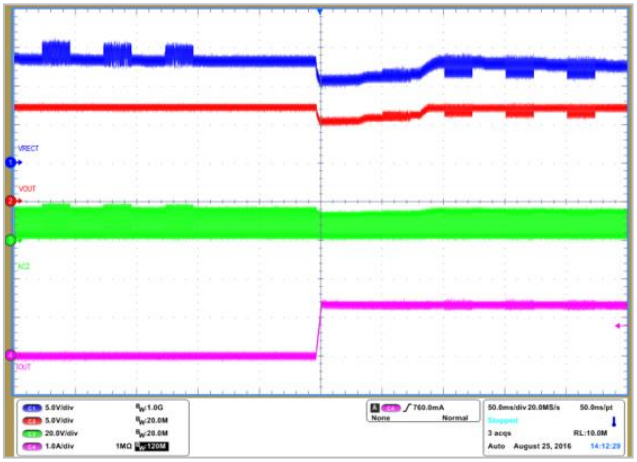
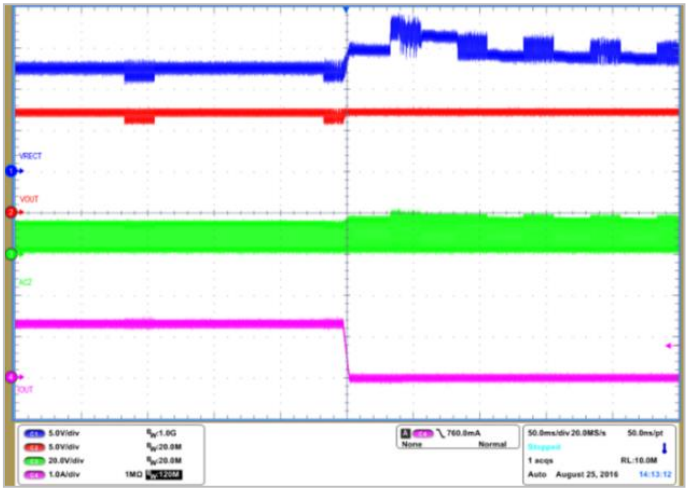
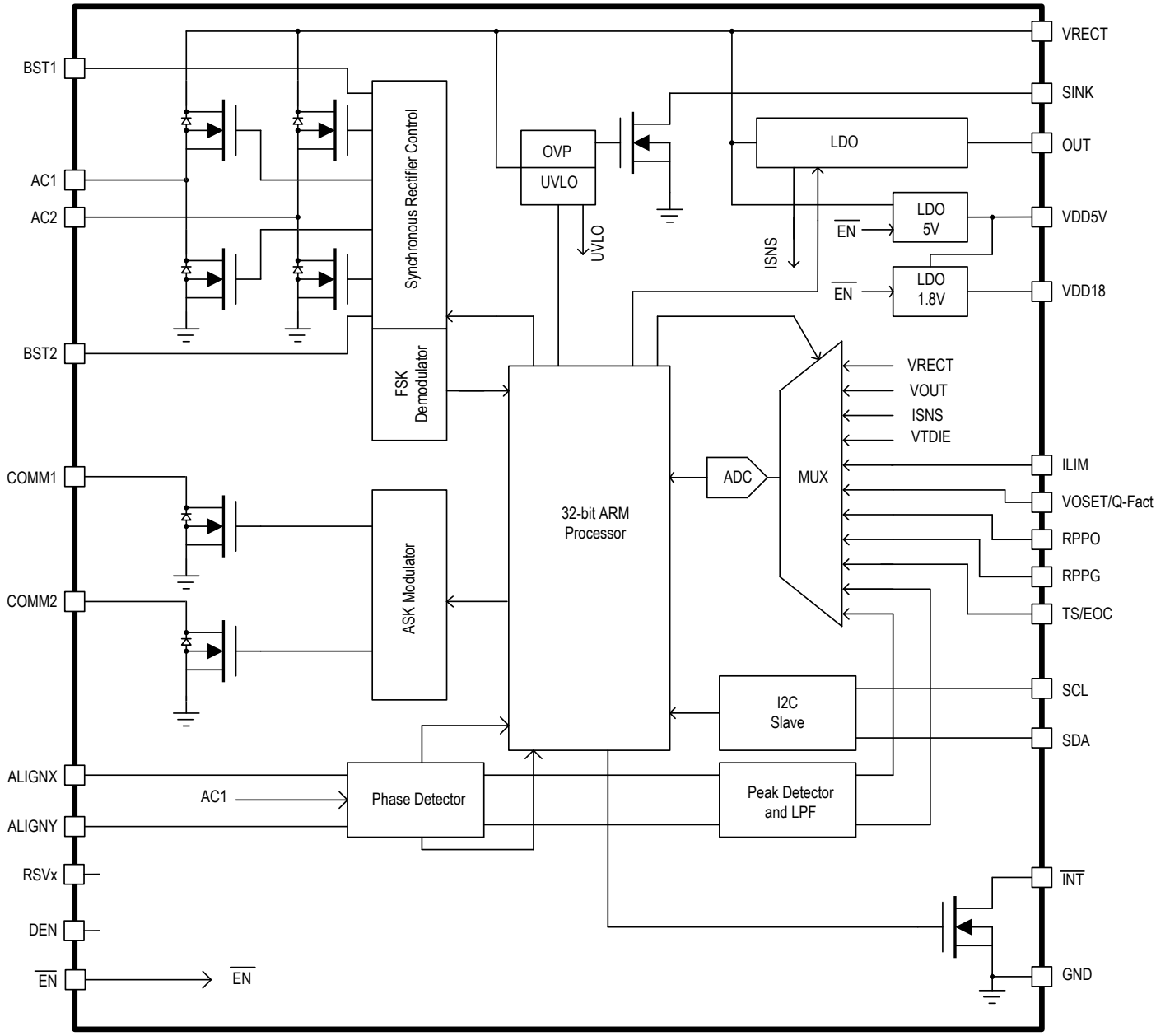


Figure 16. Transient Resp: V_{OUT} = 12V; I_{OUT} = 1.3A to 0



7. Functional Block Diagram

Figure 17. Functional Block Diagram



8. Theory of Operation

The P9221-R3 is a highly-integrated, wireless power receiver targeted for 15W applications. The device integrates a full-wave synchronous rectifier, low-dropout (LDO) linear regulator, and a 32-bit ARM® Cortex® -M0 processor to manage all the digital control required to comply with the WPC-1.2 communication protocol.

Using the near-field inductive power transfer, the receiver converts the AC signal to a DC voltage using the integrated synchronous rectifier. The capacitor connected to the output of the rectifier smooths the full-wave rectified voltage into a DC voltage. After the internal biasing circuit is enabled, the “Synchronous Rectifier Control” block operates the switches of the rectifier in various modes to maintain reliable connections and optimal efficiency.

The rectifier voltage and the output current are sampled periodically and digitized by the analog-to-digital converter (ADC). The digital equivalents of the voltage and current are supplied to the internal control logic, which determines whether the loading conditions on the VRECT pin indicate that a change in the operating point is required. If the load is heavy enough and brings the voltage at VRECT below its target, the transmitter is set to a lower frequency that is closer to resonance and to a higher output power. If the voltage at VRECT is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO’s load current increases. The internal temperature is continuously monitored to ensure proper operation.

In the event that the VRECT voltage increases above 13.5V, the control loop disables the LDO and sends error packets to the transmitter in an attempt to bring the rectifier voltage back to a safe operating voltage level while simultaneously clamping the incoming energy using the open-drain SINK pin for VRECT linear clamping. The clamp is released when the VRECT voltage falls below the V_{OVP-DC} minus $V_{OVP-HYS}$. Refer to Figure 17. The receiver utilizes IDT’s proprietary voltage clamping scheme, which limits the maximum voltage at the rectifier pin to 13.5V, reducing the voltage stress on the output capacitors while eliminating the need for over-voltage protection (OVP) capacitors. As a result, it provides a small application area, making it an industry-leading wireless power receiver for high power density applications. Combined with the P9242-R3 transmitter, the P9221-R3 is a complete wireless power system solution.

8.1 LDO – Low Dropout Regulators

The P9221-R3 has three low-dropout linear regulators. The main regulator is used to provide the power required by the battery charger where the output voltage can be set to either 9V or 12V. For more information about setting the output voltage, see section 8.2. It is important to connect a minimum of a 20µF ceramic capacitance to the OUT pin.

The other two regulators, VDD5V and VDD18, are to bias the internal circuitry of the receiver. The LDOs must have local 1µF ceramic capacitors placed as close as possible to the pins.

8.2 Setting the Output Voltage and Reference Q-factor Value – VOSET/Q-Fact

The output voltage on the P9221-R3 is programmed by connecting the center tap of the external resistors R34 and R33 to the VOSET/Q-Fact pin as shown in the application schematic in Figure 28. The output voltage can be set to 9V or 12V. The recommended settings for R33 and R34 are summarized in Table 6.

The default output voltage is set to 12V in the P9221-R3 Evaluation Board (R34 = 10kΩ; R33 = open). For applications where the transmitter is capable of delivering only 5W, the P9221-R3 will automatically switch to 5V output to ensure 5W power delivery. The 5W option can be disabled by changing the value of R33 as defined in Table 6. In this case, if the receiver is placed on a 5W transmitter, the receiver output pin will be high impedance.

The VOSET/Q-Fact pin also sets the Q-factor value by adjusting R34 and R33 as shown in Table 6. The default value is set to 103 on the P9221-R3 Evaluation Board. For development purposes, the Q-factor should be set to 20 to avoid prematurely triggering the Q-factor.

Table 6. Setting the Output Voltage and Reference Q-factor Value

Q Factor Value Setting	VOUT Setting(R34/R33 Values)							
	9V without 5V		9V with 5V		12V without 5V		12V with 5V	
	R34	R33	R34	R33	R34	R33	R34	R33
103	10kΩ	4.87kΩ	Open	10kΩ	10kΩ	21kΩ	10kΩ	Open
80	10kΩ	4.32kΩ	10kΩ	0.31kΩ	10kΩ	22.6kΩ	10kΩ	324kΩ
60	10kΩ	3.65kΩ	10kΩ	0.681kΩ	10kΩ	27.4kΩ	10kΩ	147kΩ
40	10kΩ	3.09kΩ	10kΩ	1.1kΩ	10kΩ	32.4kΩ	10kΩ	90.9kΩ
20	10kΩ	2.55kΩ	10kΩ	1.54kΩ	10kΩ	39.2kΩ	10kΩ	64.9kΩ

8.3 SINK Pin

The P9221-R3 has an internal automatic DC clamping to protect the device in the event of high voltage transients. The VRECT node must be connected to the SINK pin at all times using a 36Ω resistor with a greater than ¼W rating.

8.4 Rectifier Voltage – VRECT

The P9221-R3 uses a high-efficiency synchronous rectifier to convert the AC signal from the coil to a DC signal on the VRECT pin. During startup, the rectifier operates as a passive diode bridge. When the voltage on VRECT exceeds the under-voltage lock-out level (UVLO; see Table 5), the rectifier will switch into full synchronous bridge rectifier mode. 30µFcapacitance is recommended to minimize the output voltage ripple. Add an additional 0.1uF capacitor for decoupling.

8.5 Over-Current Limit – ILIM

The P9221-R3 has a programmable current limit function for protecting the device in the event of an over-current or short-circuit fault condition. When the output current exceeds the programmed threshold (see Figure 11), the P9221-R3 will limit the load current by reducing the output voltage. The current limit should be set to 120% of the target maximum output current. See the ILIM pin description in Table 1 for further information. The ILIM pin allows changing the over-current limit value without modification of the firmware by selecting the values of R38 and R22 as shown in Table 7.

Table 7. Setting the Over-Current Limit

Voltage on ILIM Pin [V]	R38 [kΩ]	R22 [kΩ]	Output Current [A]	Over-Current Limit [A]
Pull-up	10	Open	1.25	1.6
0.60	10	5.1	0.80	1
0.45	10	3.3	0.64	0.8
0.25	10	1.6	0.40	0.5

8.6 Interrupt Function – $\overline{\text{INT}}$

The P9221-R3 provides an open-drain, active-LOW interrupt output pin. It is asserted LOW when $\overline{\text{EN}}$ is HIGH or any of the following fault conditions have been triggered: the die temperature exceeds 140°C, the external thermistor measurement exceeds the threshold (see section 8.9), or an over-current (OC) or over-voltage (OV) condition is detected. The $\overline{\text{INT}}$ pin is also pulled LOW, if the device receives user data from a P9242-R3.

During normal operation, the $\overline{\text{INT}}$ pin is pulled HIGH. This pin can be connected to the interrupt pin of a microcontroller. The source of the trigger for the interrupt can be determined by reading the I2C *Interrupt Status* register (see Table 15).

8.7 Enable Pin – $\overline{\text{EN}}$

The P9221-R3 can be disabled by applying a logic HIGH to the $\overline{\text{EN}}$ pin. When the $\overline{\text{EN}}$ pin is pulled HIGH, the device is in Shut-Down Mode. Connecting the $\overline{\text{EN}}$ pin to logic LOW activates the device.

8.8 Thermal Protection

The P9221-R3 integrates thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the P9221-R3 if the die temperature exceeds 140°C.

8.9 External Temperature Sensing and End of Charge – TS/EOC

The P9221-R3 has a temperature sensor input that can be used to monitor an external temperature by using a thermistor. The built-in comparator's reference voltage is 0.6V and 0.1V in the P9221-R3, and it is used for monitoring the voltage level on the TS/EOC pin as described by Equation 1.

$$V_{TS} = V_{VDD18} \times \frac{NTC}{R+NTC} \qquad \textbf{Equation 1}$$

Where NTC is the thermistor's resistance and R is the pull-up resistor connected to VDD18 pin. The over–temperature shutdown is triggered when the TS/EOC pin voltage is between 0.6V and 0.1V; for more information, see Figure 28.

When the TS/EOC pin is less than 0.1V, the End of Charge (EOC) function is activated and the P9221-R3 will send the End Power Transfer (EPT) packet to the transmitter terminating the power delivery.

8.10 Alignment Guide – ALIGNX and ALIGNY

This feature is used to provide directional information regarding the transmit coil and receive coil alignment while the wireless charger is in normal operation mode. Sensing coils are placed on the wireless power receiver side between the power Rx coil and power Tx coil. Special design enables the sensing coils to output zero voltage when the alignment is optimum while misalignment between the transmitter and receiver coils will result in a voltage on the sensing coils. These signals are internally rectified, filtered, and passed through the ADC providing quantitative information on the amount of misalignment. The higher the signal is, the more the coils are misaligned.

Furthermore, the signal magnitude on ALIGNX and ALIGNY provides directional information by measuring the phase between the input power AC signal and horizontal and vertical alignment signals. Once the signal passes through the ADC, the alignment information is represented by two 8-bit signed numbers, which can be read from the *Align_X* and *Align_Y* registers defined in Table 24 and Table 25 respectively, which indicate the misalignment direction and magnitude.

The application processor can provide 2D visual graphics that indicate how much the power coils are misaligned in each direction and can recommend that the user move the device on the Tx pad for the best alignment to improve the power transferred and reduce the charging time.

8.11 Advanced Foreign Object Detection (FOD)

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of such parasitic metal objects are coins, keys, paper clips, etc. The amount of heating depends on the strength of the coupled magnetic field, as well as on the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduction in power-transfer efficiency. Moreover, if no appropriate measures are taken, the heating could make the foreign object extremely hot and unsafe to touch.

During the power transfer phase (see section 11.6), the receiver periodically communicates to the transmitter the amount of power received by means of a Received Power Packet (RPP). The transmitter will compare this power with the amount of power transmitted during the same time period. If there is a significant unexplained loss of power, then the transmitter will shut off power delivery because a possible foreign object might be absorbing too much energy.

For a WPC system to perform this function with sufficient accuracy, both the transmitter and receiver must account for and compensate for all of their known losses. Such losses could be due to resistive losses or nearby metals that are part of the transmitter or receiver, etc. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects because they cause an unknown loss. The WPC specification requires that a power receiver must report to the power transmitter its received power (P_{PR}) in an RPP. The maximum value of the received power accuracy P_{Δ} depends on the maximum power of the power receiver as defined in Table 8.

The power receiver must determine its P_{PR} with an accuracy of $\pm P_{\Delta}$, and report its received power as $P_{RECEIVED} = P_{PR} + P_{\Delta}$. This means that the reported received power is always greater than or equal to the transmitted power (P_{PT}) if there is no foreign object (FO) present on the interface surface.

Table 8. Maximum Estimated Power Loss

Maximum Power [W]	Maximum $P\Delta$ [mW]
15	750

The compensation algorithm includes values that are programmable via either the I2C interface or OTP (one-time programmable) bits. Programmability is necessary so that the calibration settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the transmit and receive coils, battery, shielding, and case materials under no-load to full-load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

See section 8.12 for details for adjusting or disabling the FOD for the P9221-R3 using the RPP0 and RPPG pins.

8.12 Received Power Packet Offset and Gain Calibration – RPPO and RPPG

The received power packet offset (RPPO) and received power packet gain (RPPG) calibrations utilize dedicated pins for tuning foreign object detection (FOD). These calibrations tune the received power packet via the voltage levels on the RPPO and RPPG pins, which are determined by the external resistors in divider networks on the 1.8V bias voltage. The voltage level on the RPPO pin is used to add offset in order to shift the Received Power Packet (RPP) globally, and the voltage level on the RPPG pin adjusts the slope gain of the Received Power Packet (RPP).

- The received power packet offset calibration can be tuned by varying the voltage on the RPPO pin from 0.1V to 2.1V corresponding to a power offset range from -1.56W to 2.34W.
- The received power packet gain can be tuned by varying the voltage on the RPPG pin from 0.1V to 2.1V corresponding to a gain setting in the range from 0.111 to 2.33.
- To disable the FOD, the RPP0 and RPPG must be connected to GND.

The RPP is adjusted according to Equation 2:

$$RPP\ [\text{mW}] = P_{measured}\ [mW] \times \frac{RPPG\ [\%]}{1755\ [\%]} + RPPO\ [\text{mW}] - 1755\ [\text{mW}] \qquad \textbf{Equation 2}$$

Where

RPP = Reported Received Power

$P_{measured}$ = measured power from output voltage and current

$$RPPO\ [\text{mW}] = \frac{V_{RPPO}\ [\text{V}]}{2.1\ [\text{V}]} \times 4095\ [\text{mW}] \qquad \textbf{Equation 3}$$

$$RPPG\ [\%] = \frac{V_{RPPG}\ [\text{V}]}{2.1\ [\text{V}]} \times 4095\ [\%] \qquad \textbf{Equation 4}$$

For example, if the voltage on the RPPO and RPPG pins is 0.9V then the RPP will have no offset or gain. The RPP will be exactly the same as the measured power in the receiver.

9. Communication Interface

9.1 Modulation/Communication

Wireless medium-power charging systems implementing the P9221-R3 as the receiver use two-way communication: receiver-to-transmitter and transmitter-to receiver.

Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's coil; the communication is purely digital and logic 1's and 0's ride on top of the power signal that exists between the two coils. Modulation is done with amplitude-shift keying (ASK) modulation using internal switches to connect external capacitors from AC1 and AC2 to ground (see Figure 17) with a bit rate of 2Kbps. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. The power transmitter detects this as a modulation of coil current/voltage to receive the packets. See sections 9.3 and 9.4 for details for ASK modulation.

9.2 Bit Encoding Scheme for FSK

Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The power receiver P9221-R3 can demodulate FSK data from the power signal frequency and use it in order to establish the handshaking protocol with the power transmitter.

The P9221-R3 implements FSK communication when used in conjunction with WPC-compliant transmitters, such as the P9242-R3. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) to the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles. Equation 5 should be used to compute the modulated frequency based on any given operating frequency. The P9221-R3 will only implement positive FSK polarity adjustments; in other words, the modulated frequency will always be higher than the operating frequency during FSK communication.

Communication packets are transmitted from transmitter to receiver with less than 1% positive frequency deviation following any receiver-to-transmitter communication packet. The frequency deviation is calculated using Equation 5.

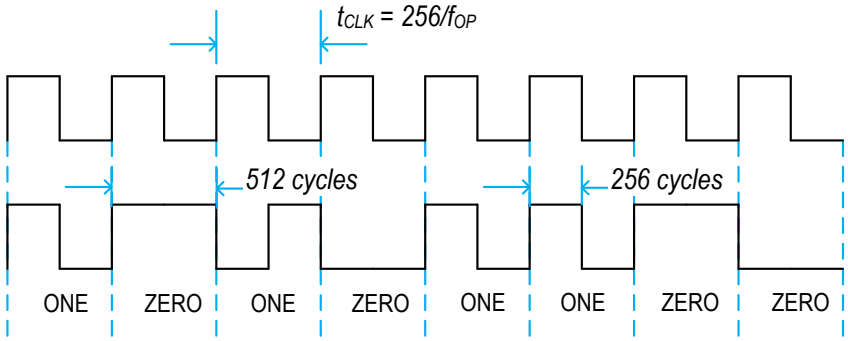
$$f_{MOD} = \frac{60000}{\frac{60000}{f_{OP}} - 3} \text{ [KHz]}$$

Equation 5

Where f_{MOD} is the changed frequency in the power signal frequency; f_{OP} is the base operating frequency of the power transfer; and 60000kHz is the internal oscillator responsible for counting the period of the power transfer signal.

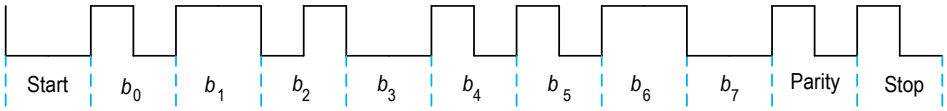
The FSK byte-encoding scheme and packet structure comply with the WPC specification revision 1.2. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit consists of 512 consecutive f_{MOD} cycles (or logic '0'). A logic '1' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic '0' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 18. Example of Differential Bi-phase Decoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 19:

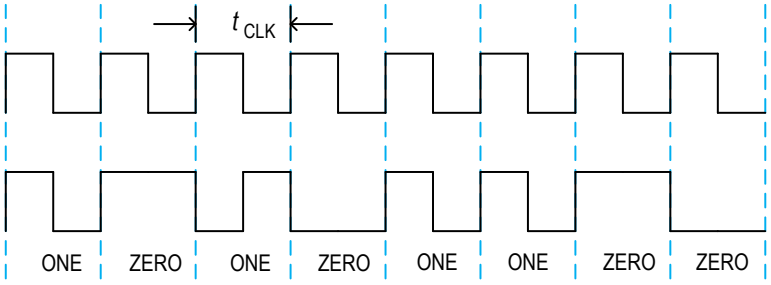
Figure 19. Example of Asynchronous Serial Byte Format for FSK



9.3 Bit Encoding Scheme for ASK

As required by the WPC, the P9221-R3 uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using one wider transition as shown below:

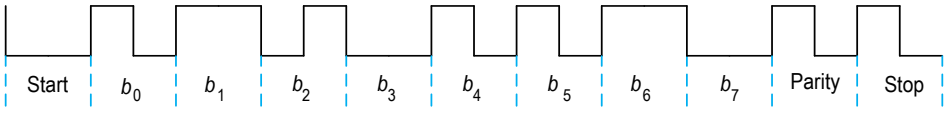
Figure 20. Bit Encoding Scheme



9.4 Byte Encoding for ASK

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 21. Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

Figure 21. Byte Encoding Scheme



9.5 Packet Structure

The P9221-R3 communicates with the base station via communication packets. Each communication packet has the following structure:

Figure 22. Communication Packet Structure

Preamble	Header	Message	Checksum

10. Bi-directional User Data Communication

In customer end systems, the transmitter and receiver boards need to have an external microcontroller (MCU) or leverage an existing application processor to orchestrate bi-directional communication. Using the I2C communication, the MCU on the receiver board needs to load the data into specific registers and trigger the communication. The P9221-R3 sends the data to the P9242-R3 using amplitude-shift keying (ASK) modulation. The P9242-R3 will receive the data and interrupt the MCU on the transmitter when the data is ready to be read. The external MCU on the transmitter follows the same procedure to send the data to the P9221-R3. When new data is available to be read, the P9221-R3 will interrupt the external MCU on the receiver board.

Bi-directional user data communication is enabled only in the power transfer phase for the WPC standard. The external MCU on the receiver board can read register $014A_{HEX}$ to determine whether the P9221-R3 is in the power transfer phase. Register $014A_{HEX}$ will be set to 5_{HEX} when the device is in the power transfer phase.

See Figure 25 for a state diagram that illustrates the procedure that the external MCU on the receiver board must follow to send the user data from the P9221-R3 to the P9242-R3 as described in section 10.1. See Figure 26 for a state diagram that illustrates the procedure the external MCU must follow to read the data sent by the P9242-R3 as described in section 10.2.

10.1 Transferring Data from the P9221-R3 to the P9242-R3

The external MCU on the receiver board should read bit 0 in register $004E_{HEX}$ to determine the status of the communication channel before initiating a new transfer. If the communication channel is free, bit 0 in register $004E_{HEX}$ is 0. If the communication channel is busy, bit 0 in register $004E_{HEX}$ is set to 1.

The P9221-R3 receiver supports sending up to 8 bytes of user data. The external MCU on the receiver should write the data that it will be sending to the transmitter into outgoing data registers (0089_{HEX} to 0090_{HEX}) and set the *Data Header* register (0088_{HEX}) accordingly. The *Data Header* register (see Table 29) indicates the number of bytes that need to be transmitted. For example, if the external MCU on the receiver intends to transfer 3 bytes of information, it should write 38_{HEX} to register 0088_{HEX} and write the user data into registers 0089_{HEX} to $008B_{HEX}$. The P9221-R3 will not transfer registers $008C_{HEX}$ to 0090_{HEX} when the header is set to 3 bytes. If the external MCU on the receiver will be sending 8 bytes of information, it should write 88_{HEX} to register 0088_{HEX} and write the data into registers 0089_{HEX} to 0090_{HEX}.

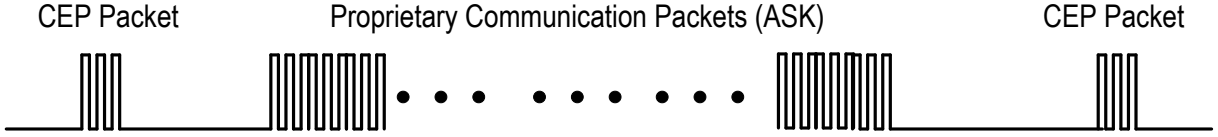
Table 9. Registers Used for Data Transmission from P9221-R3 to P9242-R3

Register	Register Address
Command Register	$004E_{HEX}$
Data Header Register	0088_{HEX}
Outgoing User Data Registers	0089_{HEX} to 0090_{HEX} (8 bytes)
WPC Power Transfer Phase Indicator	$014A_{HEX}$

The external MCU on the receiver should set bit 0 in the *Command* register $004E_{HEX}$ to 1 for triggering the communication after loading the user data into the outgoing data registers and setting the data header for the correct number of bytes. After receiving the communication trigger from the control register, the P9221-R3 reads the data header register and outgoing data registers and constructs a proprietary communication packet with a packet checksum. The communication packet is sent into the channel between two Control Error Packets (CEP) using ASK modulation.

Figure 23 shows the timing diagram for the user data transfer from the P9221-R3 to the P9242-R3.

Figure 23. Timing Diagram for a User Data Transfer from the P9221-R3 to the P9242-R3



The P9221-R3 transfers data into the channel at a speed of 2Kbps. However, the channel is usually busy transmitting WPC standard communication packets. There is a very small window in which the user data can transferred. Typically in the power transfer phase, the CEP packet is sent every 150msec. In one second, there will be only 6 to 7 time slots in which the P9221-R3 can send a maximum of 10 bytes (including the checksum and header) of user data in each slot. The maximum data transfer rate achieved between the P9221-R3 and the P9242-R3 is 560bps.

The P9221-R3 will reset bit 0 in the *Command* register $004E_{HEX}$ to 0 immediately after sending the data into the channel. The external MCU on the receiver can periodically check bit 0 in the P9221-R3 register $004E_{HEX}$ to get an acknowledgment of successful data transmission into the channel.

Note: The P9221-R3 gives WPC standard communication packets priority over user data packets. User data packets have the lowest priority; therefore during load transients, the P9221-R3 might skip sending user data packets and give priority to CEP and indicate the channel status as busy in register $004E_{HEX}$.

The P9221-R3 does not wait for acknowledgement from the P9242-R3 or keep track of successful delivery of the data to the P9242-R3. The P9221-R3 only functions as a messenger and relies upon the external MCUs on the receiver and transmitter boards to craft a lossless communication protocol by adding intelligence into data they are transferring.

Figure 24. Typical P9221-R3 to P9242-R3 Data Transfer using the WP15WBD-RK Evaluation Kit

Note: The WP15WBD-RK is the evaluation kit available for the P9221-R3 and P9242-R3, which implements the typical application schematic shown in Figure 28.

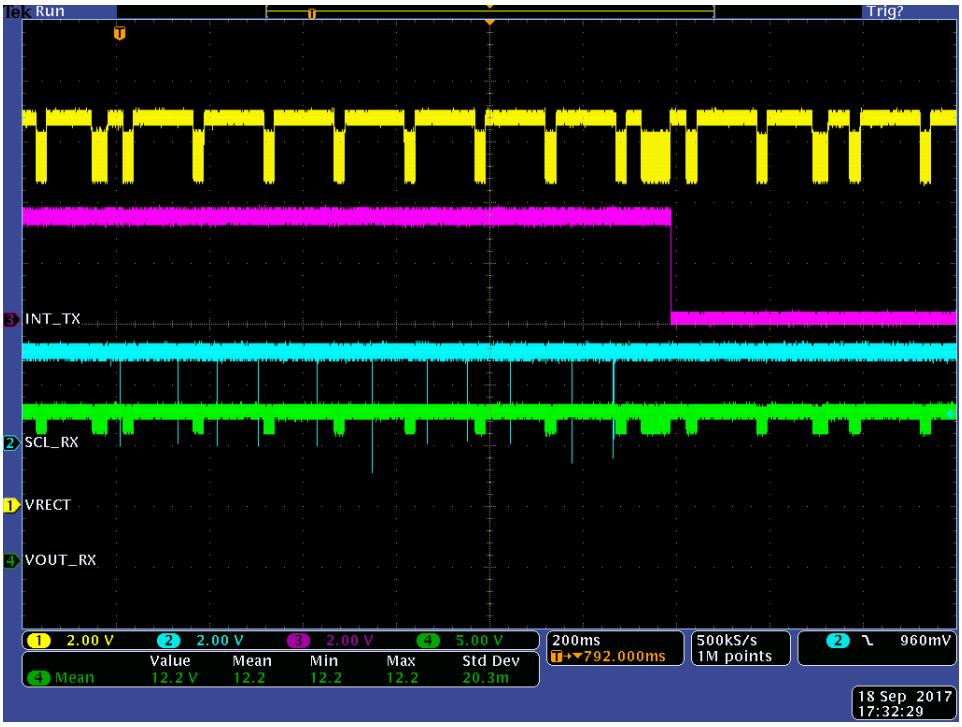
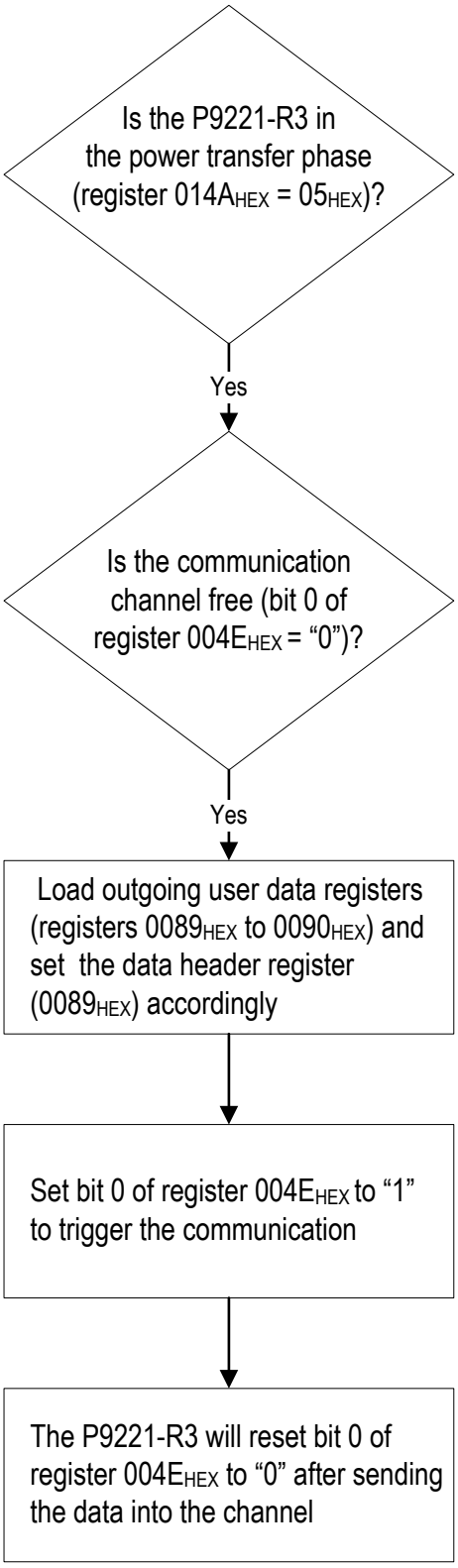


Figure 25. State Diagram for User Data Transmission from the P9221-R3 to the P9242-R3



10.2 Reading Data Sent from the P9242-R3 to the P9221-R3

The 9221-R3 can receive 2 bytes of information at a time. When the P9221-R3 receives the data from the P9242-R3, it will generate an interrupt to the external MCU on the receiver by pulling down the interrupt pin ($\overline{INT}$). Because interrupts can be generated for multiple reasons, the MCU can respond to the interrupt and read the data received flag in bit 4 in *Status* register 0034_{HEX} to confirm that the interrupt is generated because of new incoming data. The data received flag (bit 4 in register 0034_{HEX}) is set to 1 when there is new incoming data. After confirming that new data is available to read, the external MCU can read incoming user data registers 0058_{HEX} and 0059_{HEX}.

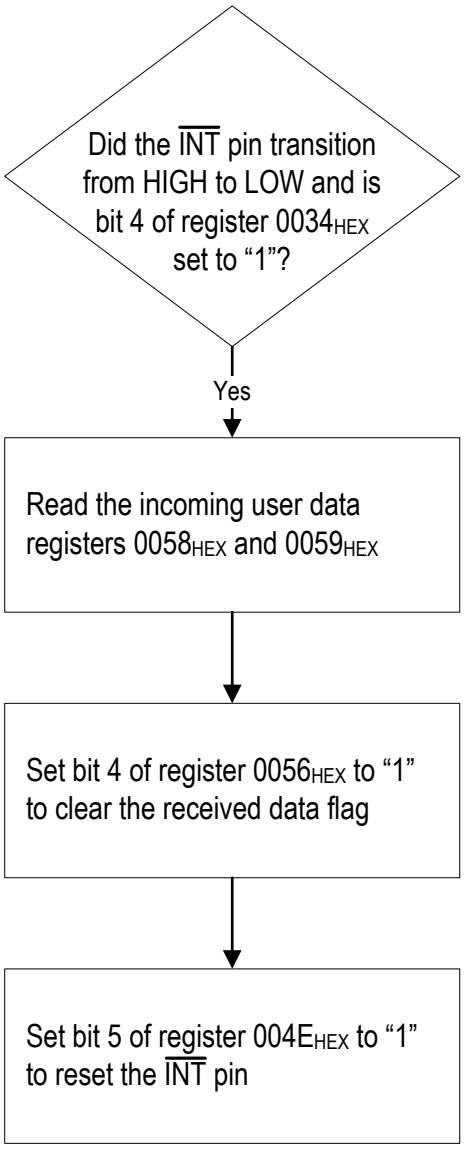
Table 10. Registers Used for Reading User Data from the P9242-R3

Register Name	Register Address
Status Register	0034_{HEX}
Command Register	$004E_{HEX}$
Clear Interrupts	0056_{HEX}
User Incoming Data	0058_{HEX} and 0059_{HEX}

After reading the data, the external MCU on the receiver should clear the interrupt by writing 1 to bit 5 in *Command* register $004E_{HEX}$ and clear the data received flag in bit 4 in *Status* register 0034_{HEX} by writing 1 to bit 4 in register 56_{HEX}. If the external MCU on the receiver does not handle interrupts, it should constantly poll bit 4 in register 0034_{HEX} to check whether there is any new incoming data.

If the external MCU on the receiver does not read the data soon after the interrupt is received, there is a risk that the data will become corrupted because of new incoming data. The P9221-R3 does not reject new incoming data because old data was not read by the MCU on the receiver. The user can implement a higher-level handshaking protocol between the external MCU on the transmitter and the receiver to avoid data corruption.

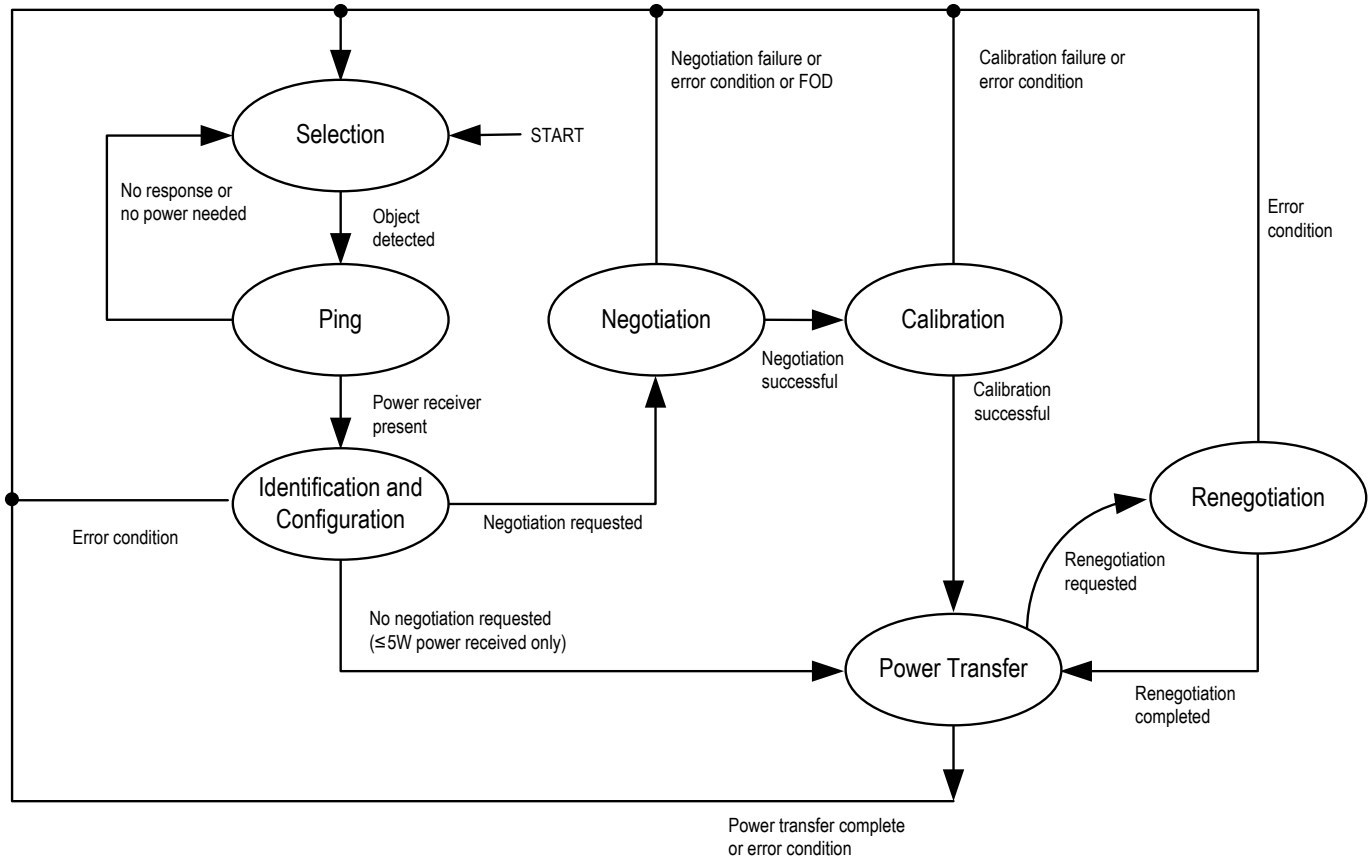
Figure 26. State Diagram for Reading User Data Received from the P9242-R3



11. WPC Mode Characteristics

The Extended Power Profile adds a negotiation phase, a calibration phase, and renegotiation phase to the basic system control functionality of the Baseline Power Profile, as shown in Figure 27.

Figure 27. WPC Power Transfer Phases Flowchart



11.1 Selection Phase or Startup

In the selection phase, the power transmitter determines if it will proceed to the ping phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a small measurement signal. This measurement signal should not wake up a power receiver that is positioned on the interface surface.

11.2 Ping Phase (Digital Ping)

In the ping phase, the power transmitter will transmit power and will detect the response from a possible power receiver. This response assures the power transmitter that it is dealing with a power receiver rather than some unknown object. When a mobile device containing the P9221-R3 is placed on a WPC “Qi” charging pad, it responds to the application of a power signal by rectifying this power signal. When the voltage on the VRECT pin is greater than the UVLO threshold, then the internal bandgaps, reference voltage, and internal voltage regulators (5V and 1.8V) are turned on and the microcontroller’s startup is initiated enabling the WPC communication protocol.

If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the identification and configuration phase of the power transfer, maintaining the power signal output.

11.3 Identification and Configuration Phase

The identification and configuration phase is the part of the protocol that the power transmitter executes in order to identify the power receiver and establish a default power transfer contract. This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information.

In this phase, the power receiver identifies itself and provides information for a default power transfer contract:

- It sends the configuration packet.
- If the power transmitter does not acknowledge the request (does not transmit FSK modulation), the power receiver will assume 5W output power.

11.4 Negotiation Phase

In the negotiation phase, the power receiver negotiates changes to the default power transfer contract. In addition, the power receiver verifies that the power transmitter has not detected a foreign object.

11.5 Calibration Phase

In the calibration phase, the power receiver provides information that the power transmitter can use to improve its ability to detect foreign objects during power transfer.

11.6 Power Transfer Phase

In this phase, the P9221-R3 controls the power transfer by means of the following control data packets:

- Control Error Packets (CEP)
- Received Power Packet (RPP, FOD-related)
- End Power Transfer (EPT) Packet

Once the “identification and configuration” phase is completed, the transmitter initiates the power transfer mode. The P9221-R3 control circuit measures the rectifier voltage and sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator and to send to the transmitter the actual received power packet for foreign object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the application, the P9221-R3 turns off the LDO and continuously sends EPT packets until the transmitter removes the power and the rectified voltage on the receiver side drops below the UVLO threshold.

12. Functional Registers

The following tables provide the address locations, field names, available operations (R or RW), default values, and functional descriptions of all the internally accessible registers contained within the P9221-R3. The default I2C slave address is 61_{HEX}. The address of each register has a two-byte structure. For example, the address of chip ID high byte read from 00_{HEX} and 01_{HEX}.

Table 11. Device Identification Register

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0000_{HEX} [7:0]	Part_number_L	R	20_{HEX}	Chip identification low byte.
0001_{HEX} [7:0]	Part_number_H	R	92_{HEX}	Chip identification high byte.

Table 12. Firmware Major Revision

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0004_{HEX} [7:0]	FW_Major_Rev_L	R	01_{HEX}	Major firmware revision low byte.
0005_{HEX} [7:0]	FW_Major_Rev_H	R	00_{HEX}	Major firmware revision high byte.

Table 13. Firmware Minor Revision

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0006_{HEX} [7:0]	FW_Minor_Rev_L	R	29_{HEX}	Minor firmware revision low byte.
0007_{HEX} [7:0]	FW_Minor_Rev_H	R	04_{HEX}	Minor firmware revision high byte.

Table 14. Status Registers

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0034_{HEX} [7]	Vout_Status	R	0_{BIN}	“0” output voltage is off. “1” output voltage is on.
0034_{HEX} [6]	Reserved	R	0_{BIN}	
0034_{HEX} [5]	Reserved	R	0_{BIN}	
0034_{HEX} [4]	User_Data_Received	R	0_{BIN}	“1” indicates that the P9221-R3 has received data from the P9242-R3. This bit must be reset after the application processor reads the user data. This bit can be reset by writing 20_{HEX} to the $004E_{HEX}$ register
0034_{HEX} [3]	Reserved	R	0_{BIN}	
0034_{HEX} [2]	Thermal_SHTDN_Status	R	0_{BIN}	“0” indicates no over-temperature condition exists. “1” indicates that the die temperature exceeds 130°C or the NTC reading is less than 0.6V. The P9221-R3 sends an End Power Transfer (EPT) packet to the transmitter.

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0034_{HEX} [1]	VRECT_OV_ Status	R	0_{BIN}	"1" indicates the rectifier voltage exceeds 20V for V_{OUT}=12V. In this case, the P9221-R3 sends an End Power Transfer (EPT) packet to the transmitter.
0034_{HEX} [0]	Current_Limit_Status	R	0_{BIN}	"1" indicates the current limit has been exceeded. In this case, the P9221-R3 sends an End Power Transfer (EPT) packet to the transmitter.
0035_{HEX} [7:0]	Reserved	R	00_{HEX}	

Table 15. Interrupt Status Registers

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0036_{HEX} [7]	INT_Vout_Status	R	0_{BIN}	"0" indicates the output voltage has not changed. "1" indicates the output voltage changed.
0036_{HEX} [6]	Reserved	R	0_{BIN}	
0036_{HEX} [5]	Reserved	R	0_{BIN}	
0036_{HEX} [4]	User_Data_Received_status	R	0_{BIN}	"1" indicates that the P9221-R3 has received data from the P9242-R3. This bit must be reset after the application processor reads the user data.
0036_{HEX} [3]	Reserved	R	0_{BIN}	
0036_{HEX} [2]	INT_OVER_TEMP_Status	R	0_{BIN}	"1" indicates an over-temperature condition exists.
0036_{HEX} [1]	INT_VRECT_OV_Status	R	0_{BIN}	"1" indicates a rectifier over-voltage condition exists.
0036_{HEX} [0]	INT_OC_Limit_Status	R	0	"1" indicates the current limit has been exceeded.
0037_{HEX} [7:0]	Reserved	R	00_{HEX}	

Note: If any bit in the *Interrupt Status* register 0036_{HEX} is "1" and the corresponding bit in the *Interrupt Enable* register 38_{HEX} is set to "1," the $\overline{INT}$ pin will be pulled down indicating an interrupt event has occurred.

Table 16. Interrupt Enable Registers

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0038_{HEX} [7]	Vout_Status_INT_EN	RW	0_{BIN}	"0" disables the *INT_Vout_Status* interrupt. "1" enables the interrupt.
0038_{HEX} [6]	Reserved	R	0_{BIN}	
0038_{HEX} [5]	Reserved	R	0_{BIN}	
0038_{HEX} [4]	User_Data_Received_EN	R	1_{BIN}	"0" disables the *User_Data_Received* interrupt. "1" enables the interrupt.
0038_{HEX} [3]	Reserved	R	1_{BIN}	
0038_{HEX} [2]	OVER_TEMP_INT_EN	R	1_{BIN}	"0" disables the *INT_OVER_TEMP* interrupt. "1" enables the interrupt.

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0038_{HEX} [1]	VRECT_OV_INT_EN	RW	1_{BIN}	“0” disables the *INT_VRECT_OV* interrupt. "1" enables the interrupt.
0038_{HEX} [0]	OC_Limit_Status_INT_EN	RW	1_{BIN}	“0” disables the *INT_OC_Limit_Status* interrupt. "1" enables the interrupt.
0039_{HEX} [7:0]	Reserved	RW	00_{HEX}	

Table 17. Battery Charge Status

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
$003A_{HEX}$ [7:0]	Batt_Charg_status	R/W	00_{HEX}	The application processor loads the battery charge status in this register. This value is sent to the transmitter when bit 4 of register $004E_{HEX}$ is set to “1.”[a]

[a] The firmware only forwards the data from the application processor to transmitter.

Table 18. End Power Transfer

The application processor initiates the End Power Transfer (EPT).

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
$003B_{HEX}$ [7:0]	EPT_Code	R/W	00_{HEX}	EPT_Code sent to transmitter.

Table 19. Read Register – Output Voltage

$$V_{OUT} = \frac{ADC\_VOUT * 6 * 2.1}{4095}$$

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
$003C_{HEX}$ [7:0]	ADC_VOUT [7:0]	R	00_{HEX}	8 LSB of VOUT ADC value.
$003D_{HEX}$ [7:4]	Reserved	R	0_{HEX}	Reserved.
$003D_{HEX}$ [3:0]	ADC_VOUT [11:8]	R	0_{HEX}	4 MSB of VOUT ADC value.

Table 20. Read Register – VRECT Voltage

$$VRECT = \frac{ADC\_VRECT * 10 * 2.1}{4095}$$

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0040_{HEX} [7:0]	ADC_VRECT [7:0]	R	–	8 LSB of VRECT ADC value.
0041_{HEX} [7:4]	Reserved	R	0_{HEX}	Reserved.
0041_{HEX} [3:0]	ADC_VRECT [11:8]	R	–	4 MSB of VRECT ADC value.

Table 21. Read Register – IOUT Current

$$I_{OUT} = \frac{RX\_IOUT * 2 * 2.1}{4095}$$

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0044_{HEX} [7:0]	RX_IOUT [7:0]	R_{HEX}	–	8 LSB of IOUT. Output current in mA.
0045_{HEX} [7:0]	RX_IOUT [15:8]	R_{HEX}	–	8 MSB of IOUT. Output current in mA.

Table 22. Read Register – Die Temperature

T_{DIE}=(*ADC_Die_Temp* — 1350) $\frac{83}{444}$ – 273 where *ADC_Die_Temp* = 12 bits from *ADC_Die_Temp_H* and *ADC_Die_Temp_L*

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0046_{HEX} [7:0]	ADC_Die_Temp_L	R	–	8 LSB of current die temperature in °C.
0047_{HEX} [7:4]	Reserved	R	0_{HEX}	Reserved.
0047_{HEX} [3:0]	ADC_Die_Temp_H	R	–	4 MSB of current die temperature in °C.

Table 23. Read Register – Operating Frequency

$$f_{OP} = \frac{64 * 6000}{OP\_FREQ\ [15:0]}$$

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0048_{HEX} [7:0]	OP_FREQ[15:8]	R	–	8 MSB of the AC signal frequency [kHz].
0049_{HEX} [7:0]	OP_FREQ[7:0]	R	–	8 LSB of the AC signal frequency [kHz].

Table 24. Alignment X Value Register

Note: Valid only in the presence of the alignment PCB coil. (See section 8.10 or the *P9221-R3 Evaluation Kit User Manual* for more information.)

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
$004B_{HEX}$ [7:0]	Align_X	R	–	8-bit signed integer representing alignment between Tx and Rx coil in the X-direction. The value is application-specific.

Table 25. Alignment Y Value Register

Note: Valid only in the presence of the alignment PCB coil. (See section 8.10 or the *P9221-R3 Evaluation Kit User Manual* for more information.)

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
$004C_{HEX}$ [7:0]	Align_Y	R	–	8-bit signed integer representing alignment between Tx and Rx coil in the Y-direction. The value is application-specific.

Table 26. Command Register

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
$004E_{HEX}$ [7:6]	Reserved	R	0_{BIN}	Reserved.
$004E_{HEX}$ [5]	Reset_Interrupt_Pin	RW	0_{BIN}	If the application processor sets this bit to "1," the P9221-R3 resets the interrupt pin. The P9221-R3 will reset the bit to “0” after resetting the interrupt pin.
$004E_{HEX}$ [4]	Send_Battery_Charge Status_packet	R	0_{BIN}	If the application processor sets this bit to "1," then the P9221-R3 sends the charge status packet once (from the *Batt_Charge_status* register; see Table 17) and then sets this bit to “0.”
$004E_{HEX}$ [3]	Send_End_Power_Transfer	RW	0_{BIN}	If the application processor sets this bit to "1," the P9221-R3 sends the End Power Transfer packet (defined in the *EPT_Code* register in Table 18) to the transmitter and then sets this bit to "0."
$004E_{HEX}$ [2]	Reserved	R	0_{BIN}	Reserved.
$004E_{HEX}$ [1]	Toggle_LDO_On-OFF	RW	0_{BIN}	If the application processor sets this bit to "1," the P9221-R3 toggles the LDO output once (from on to off or from off to on), and then sets this bit to “0.”
$004E_{HEX}$ [0]	Communication_trigger	RW	0_{BIN}	If the communication channel is free, this bit is set to “0.” The application processor sets this bit to "1" to trigger the communication. The P9221-R3 will reset this bit to “0” immediately after sending the data into the channel.

Table 27. Clear Interrupt Bits

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0056_{HEX} [7]	Clear_Vout_Changed_Bit	RW	0_{BIN}	“1” clears the *INT_Vout_Status* bit in the register 0036_{HEX}. Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing “1” to bit 5 of register $004E_{HEX}$.
0056_{HEX} [6]	Reserved	RW	0_{BIN}	
0056_{HEX} [5]	Reserved	RW	0_{BIN}	
0056_{HEX} [4]	Clear_User_Data_Received _Bit	RW	0_{BIN}	“1” clears the *User_Data_Received_status* bit in register 0036_{HEX}. Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing“1” to bit 5 of register $004E_{HEX}$.
0056_{HEX} [3]	Reserved	RW	0_{BIN}	
0056_{HEX} [2]	Clear_Over_Temperature_ Bit	RW	0_{BIN}	“1” clears the *INT_OVER_TEMP_Status* bit in register 0036_{HEX}. Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing“1” to bit 5 of register $004E_{HEX}$.

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0056_{HEX} [1]	Clear_Over_Voltage_Bit	RW	0_{BIN}	"1" clears the *INT_VRECT_OV_Status* bit in register 0036_{HEX}. Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing "1" to bit 5 of register $004E_{HEX}$.
0056_{HEX} [0]	Clear_Over_Current_Bit	RW	0_{BIN}	"1" clears the *INT_OC_Limit_Status* bit in register 0036_{HEX}. Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing "1" to bit 5 of register $004E_{HEX}$.

Table 28. Incoming User Data Registers

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0058_{HEX}	Incoming_User_Data 0	RW	00_{HEX}	The application processor reads this register to get the data P9221-R3 received from the P9242-R3.
0059_{HEX}	Incoming_User_Data 1	RW	00_{HEX}	The application processor reads this register to get the data P9221-R3 received from the P9242-R3.

Table 29. Data Header Register

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0088_{HEX}	Data_Header_Register	RW	00_{HEX}	The application processor sets this register to following values: 18_{HEX} = when sending 1 byte of user data 28_{HEX} = when sending 2 bytes of user data 38_{HEX} = when sending 3 byte of user data 48_{HEX} = when sending 4 bytes of user data 58_{HEX} = when sending 5 bytes of user data 68_{HEX} = when sending 6 bytes of user data 78_{HEX} = when sending 7 bytes of user data 84_{HEX} = when sending 8 bytes of user data

Table 30. Outgoing User Data Registers

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0089_{HEX}	Outgoing_User_Data_0	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.
$008A_{HEX}$	Outgoing_User_Data_1	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.
$008B_{HEX}$	Outgoing_User_Data_2	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.
$008C_{HEX}$	Outgoing_User_Data_3	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.
$008D_{HEX}$	Outgoing_User_Data_4	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.
$008E_{HEX}$	Outgoing_User_Data_5	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.
$008F_{HEX}$	Outgoing_User_Data_6	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.
0090_{HEX}	Outgoing_User_Data_7	RW	00_{HEX}	The application processor writes into this register the data it will be sending to the P9242-R3.

Table 31. WPC Power Transfer Phase Indicator Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$014A_{HEX}$	System_State	R	00_{HEX}	0_{DEC} = Selection Phase 1_{DEC} = Identification Phase 2_{DEC} = Configuration Phase 3_{DEC} = Post-Configuration Phase 4_{DEC} = Negotiation Phase 5_{DEC} = Power Transfer Phase 6_{DEC} = Reserved 7_{DEC} = Renegotiation Transfer Phase 8_{DEC} = Error Phase

13. Application Information

13.1 Power Dissipation and Thermal Requirements

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components must be taken into consideration.

The P9221-R3 package has a maximum power dissipation of approximately 1.72W, which is governed by the number of thermal vias between the package and the printed circuit board. The die's maximum power dissipation is specified by the junction temperature and the package thermal resistance. The WLCSP package has a typical θ_{JA} of 47°C/W with 8 thermal vias and 77°C/W with no thermal vias. Maximizing the thermal vias is highly recommended.

The ambient temperature surrounding the P9221-R3 will also have an effect on the thermal limits of the printed circuit board (PCB). The main factors influencing thermal resistance (θ_{JA}) are the PCB characteristics and thermal vias. For example, in a typical still-air environment, a significant amount of the heat generated is absorbed by the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and therefore the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

As a first step, the maximum power dissipation for a given situation should be calculated using Equation 6:

$$P_{D(MAX)} = \frac{\left(T_{J(MAX)} - T_{AMB}\right)}{\theta_{JA}}$$

Equation 6

Where $P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_{AMB} = Ambient temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the P9221-R3 device is 125°C. The thermal resistance of the 52-WLCSP package (AHG52) is nominally θ_{JA}=47°C/W with 8 thermal vias. Operation is specified to a maximum steady-state ambient temperature (T_{AMB}) of 85°C. Therefore, the maximum recommended power dissipation is given by Equation 7.

$$P_{D(MAX)} = \frac{(125°C - 85°C)}{47°C/W} \cong 0.85 \text{ Watt}$$

Equation 7

All the above-mentioned thermal resistances were determined with the P9221-R3 mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

13.2 Recommended Coils

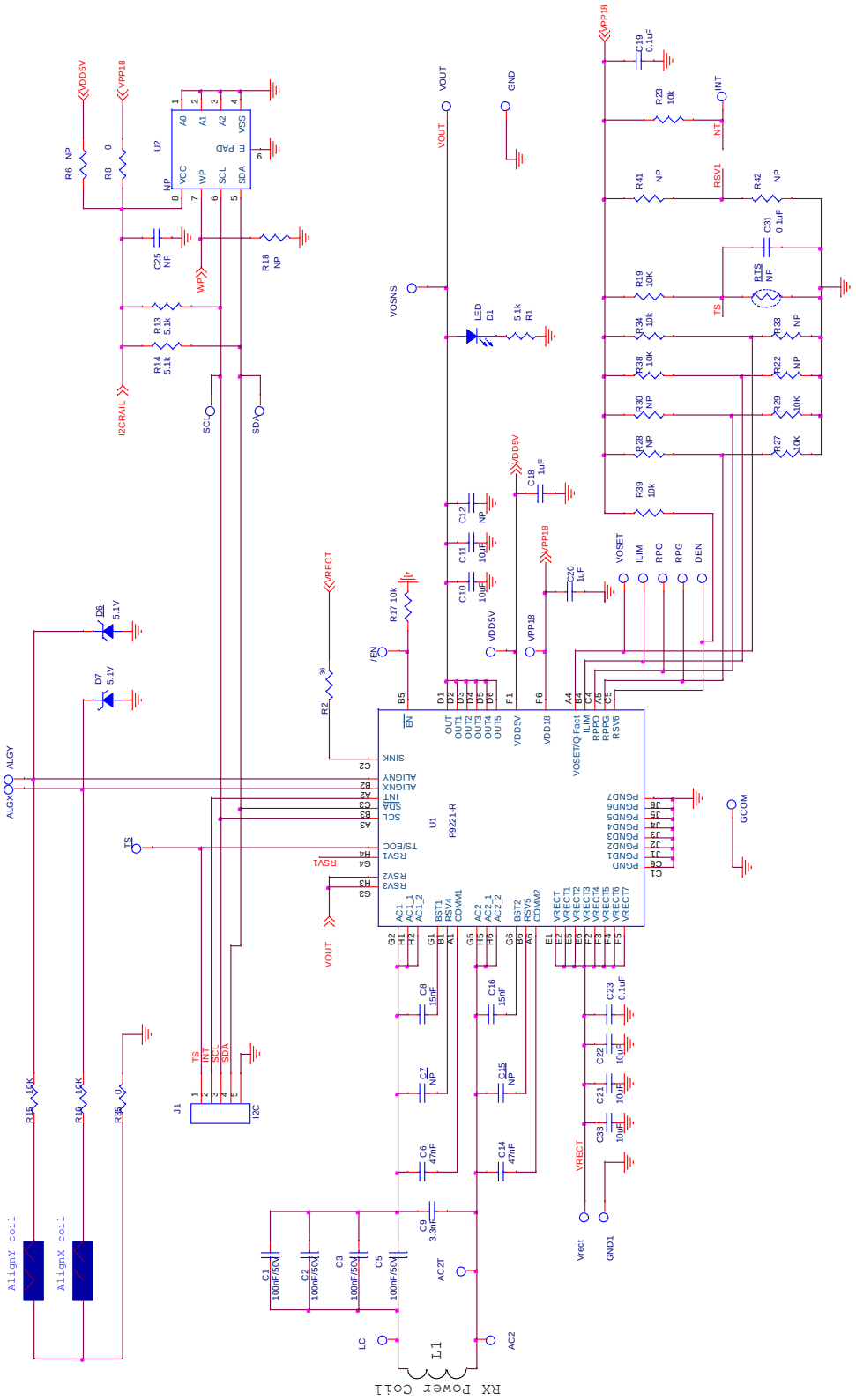
The following coils are recommended with the P9221-R3 receiver for 15W applications for optimum performance. The recommended vendor coils have been tested and verified as shown in Table 32.

Table 32. Recommended Coil Manufacturers

Output Power	Vendor	Part number	Inductance at 100kHz	ACR at 20°C	Series Resonant Capacitance
15W	AMOTECH	ASC-504060E00-S00	8.2µH	220mΩ	400nF
15W	TDK	WR424245-13K2-G	11.2µH	170mΩ	300nF
15W	SUNLORD	SWA50R40H06C02B	8.4µH	150mΩ	400nF
15W	WURTH	760308102207	8.0µH	80mΩ	400nF

13.3 Typical Application Schematic

Figure 28. Typical Application Schematic – P9221-R3 Evaluation Board Revision 2.2



13.4 Bill of Materials (BOM)

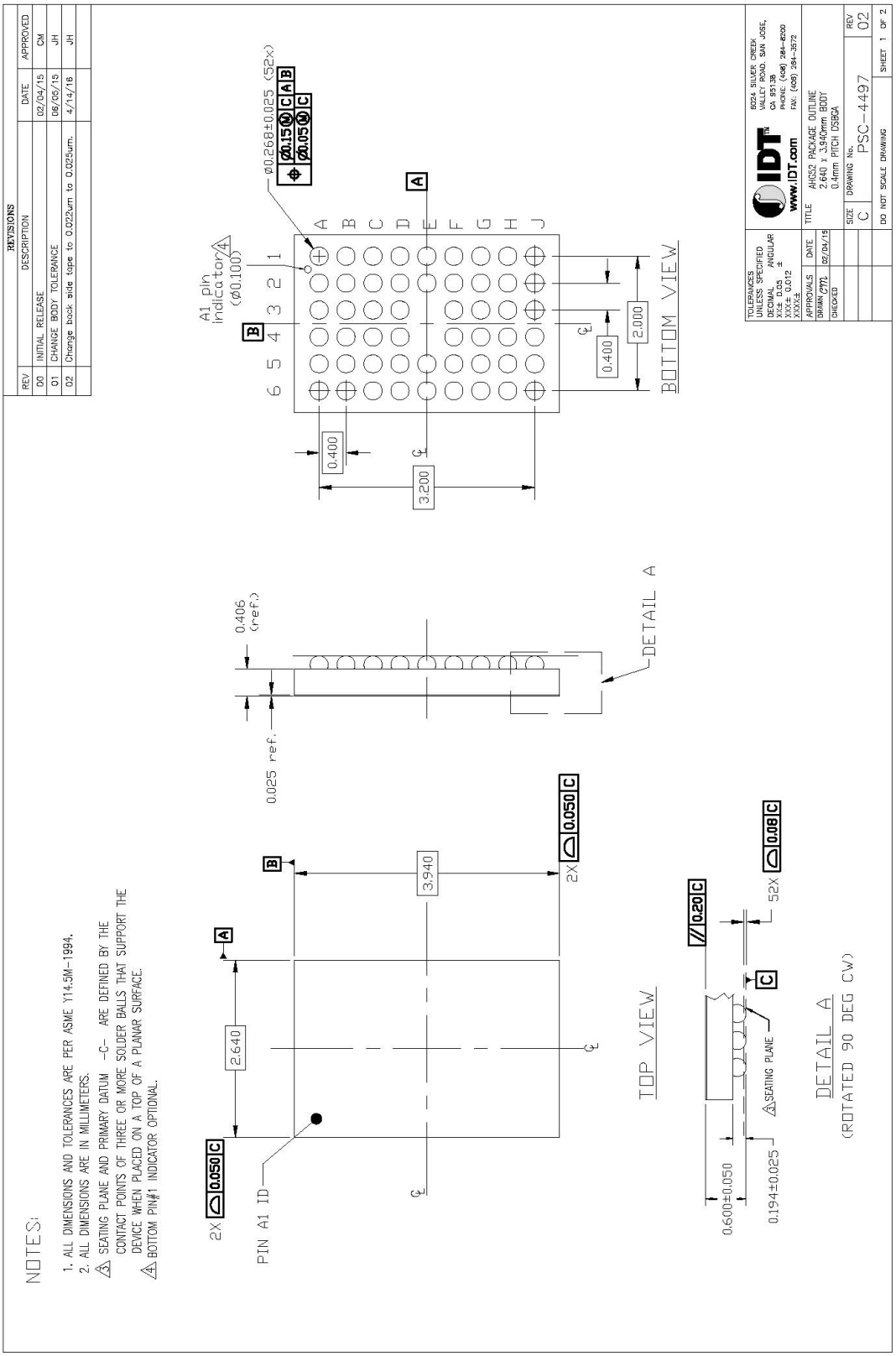
Table 33. P9221-R3 MM Evaluation Kit V2.2 Bill of Materials

Item	Reference	Quantity	Value	Description	Part number	PCB Footprint
1	AC2T, VDD5V, VPP18, VOSET, TS, SDA, SCL, RPO, RPG, INT, ILIM, GCOM, DEN, ALGY, ALGX, /EN	16	PTH_TP	Test Pad		10MIL_35PAD
2	AC2, LC	2	NP	TEST POINT		test_pt_sm_135x70
3	C1, C2, C3, C5	4	100nF	CAP CER 0.1µF 50V X5R 0402	GRM155R61H104KE19D	0402
4	C6, C14	2	47nF	CAP CER 0.047µF 50V X7R 0402	C1005X7R1H473K050BB	0402
5	C7, C15	2	NP	CAP CER 0.047µF 50V X7R 0402	C1005X7R1H473K050BB	0402
6	C8, C16	2	15nF	CAP CER 0.015µF 50V X7R 0402	GRM155R71H153KA12J	0402
7	C9	1	3.3nF	CAP CER 3300PF 50V X7R 0402	CL05B332KB5NNNC	0402
8	C10, C11, C21, C22, C33	5	10µF	CAP CER 10µF 25V X5R 0603	CL10A106MA8NRNC	0603
9	C12	1	NP	CAP CER 10µF 25V X5R 0603	CL10A106MA8NRNC	0603
10	C18,C20	2	1µF	CAP CER 1µF 10V X5R 0402	GRM155R61A105KE15D	0402
11	C19,C31	2	0.1µF	CAP CER 0.1µF 10V X5R 0201	C0603X5R1A104K030BC	0201
12	C23	1	0.1µF	CAP CER 0.1µF 25V X5R 0201	CL03A104KA3NNNC	0201
13	C25	1	NP	CAP CER 0.1µF 10V X5R 0201	C0603X5R1A104K030BC	0201
14	D1	1	LED	LED GREEN CLEAR 0603 SMD	150 060 GS7 500 0	0603_diode
15	D6,D7	2	5.1V	DIODE ZENER 5.1V 100MW 0201	CZRZ5V1B-HF	0201
16	GND1, VRECT, VOUT, VOSNS, GND	5	Test Point	TEST POINT PC MINIATURE SMT	5015	test_pt_sm_135x70
17	J1	1	I2C	HEADER_1X5_0P1PITCH60P42D	68002-205HLF	header_1x5_0p1Pitch60p42d
18	RTS	1	NP			NTC2
19	R1, R13, R14	3	5.1kΩ	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	0402
20	R2	1	36Ω	RES SMD 36 OHM 5% 1/2W 0805	ERJ-P06J360V	805
21	R6	1	NP	RES SMD 0.0OHM JUMPER	ERJ-2GE0R00X	0402

Item	Reference	Quantity	Value	Description	Part number	PCB Footprint
22	R8	1	0Ω	RES SMD 0.0OHM JUMPER 1/10W 0402	ERJ-2GE0R00X	0402
23	R15, R16	2	10KΩ	RES SMD 10K OHM 1% 1/10W 0603	RC0603FR-0710KL	0603
24	R17, R19, R23, R27, R29, R34, R38, R39	8	10kΩ	RES SMD 10K OHM 5% 1/16W 0402	CRCW040210K0JNED IF	0402
25	R18, R22, R28, R30, R33, R41, R42	7	NP	RES SMD 10K OHM 5% 1/16W 0402	CRCW040210K0JNED IF	0402
26	R35	1	0Ω	RES SMD 0.0OHM 1/10W 0603	MCR03EZPJ000	0603
27	U1	1	P9221-R3	MP Wireless power receiver	P9221-R3	csp52_2p64x3p94_0p4mm
28	U2	1	NP	IC EEPROM 128KBIT 400KHZ 8TDFN	24AA128T-I/MNY	TDFN08

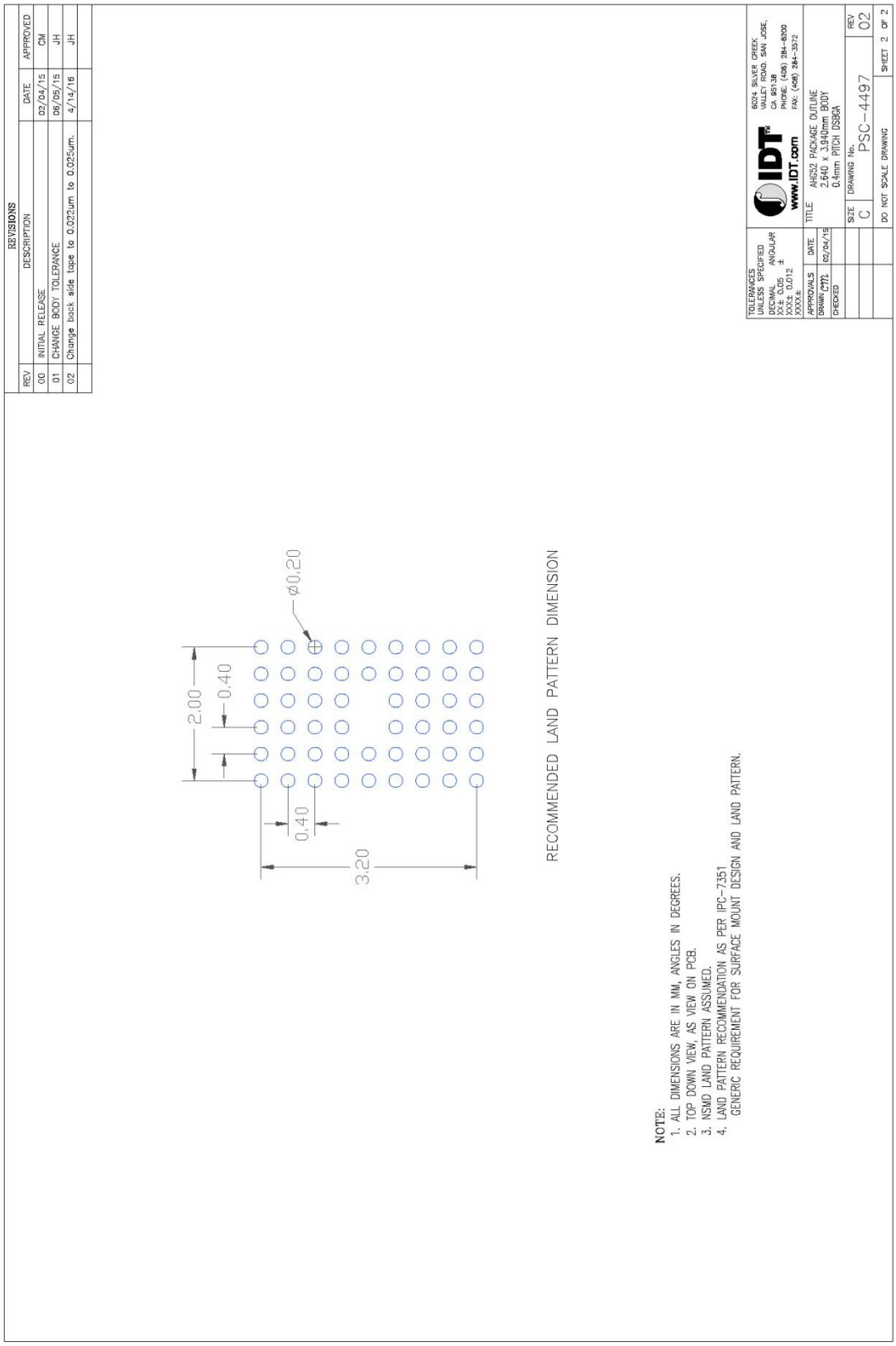
14. Package Drawings

Figure 29. Package Outline Drawing (AHG52)



15. Recommended Land Pattern

Figure 30. 52-WLCSP (AHG52) Land Pattern

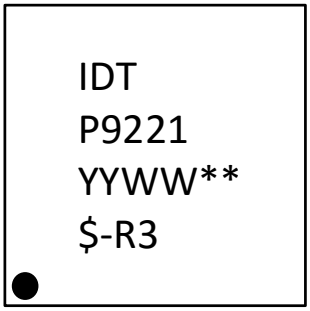


16. Special Notes: 52-WLCSP (AHG52) Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The humidity indicator card (HIC) for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

17. Marking Diagram



1. Line 1 company name.
2. Truncated part number.
3. “YYWW” is the last digit of the year and week that the part was assembled.
   ** is the lot sequential code.
4. “$” denotes mark code, -R3 is part of the device part number

18. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Ambient Temperature
P9221-R3AHGI8	P9221-R3 Wireless Power Receiver for 15W Applications, 2.64 × 3.94 mm 52-WLCSP (AHG52)	MSL1	Reel	0°C to +85°C
WP15WBD-RK	Bi-Directional Communication Evaluation Kit including the P9242-R3-EVK Transmitter Evaluation Board, P9221-R3-EVK Receiver Evaluation Board, two USB-to-I2C dongles, and a 12V/2A AC adapter.			

19. Revision History

Revision Date	Description of Change
October 20, 2017	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.