Features

- 4.5V to 6.9V input operating voltage range, supporting:
  - USB or AC adapter
  - USB dedicated charger port (DCP) detection
- WPC-1.2.2 compliant for A5 or A11-type coils
- Integrated, high-efficiency power stage with low $R_{DS(ON)}$
- Integrated foreign object detection & current sense
- Excellent EMI performance eliminates need for EMI filter
- Supports up to 8W power transfer to the receiver
- Demodulates and Decodes Communication Packets from WPC-compliant Receivers
- I^2C Interface for EEPROM access
- Programmable input over-voltage protection
- Programmable soft start
- Current limit and over-temperature protection
- -40° to +85°C temperature range
- 7 x 7 mm 56-VFQFPN package

Applications

- Furniture
- PC peripherals
- Rugged electronic gear
- Small appliances
- Battery-powered electronics

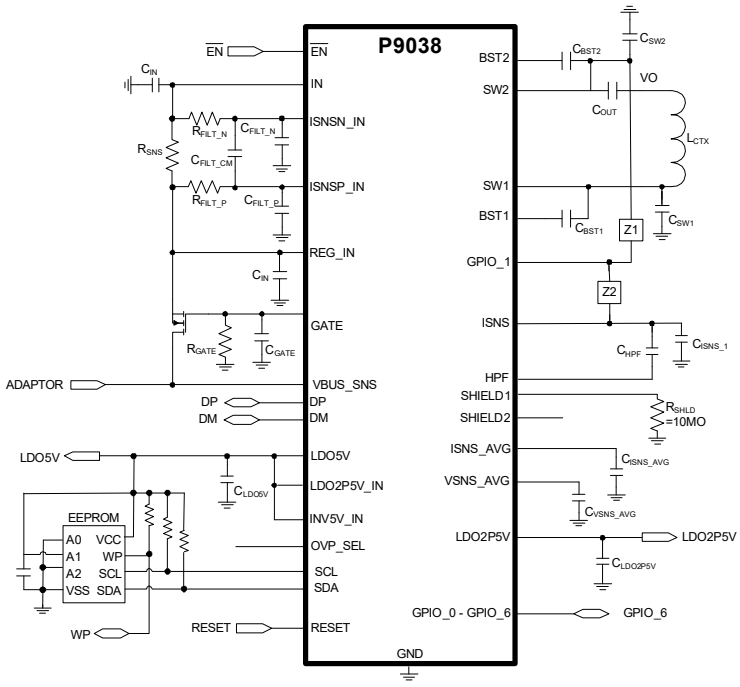
Description

The P9038 is a WPC-compliant Wireless Power Transmitter for A5 and A11 designs operating from 5V supplies conforming with WPC Specification 1.2.2. Operating in the WPC-compliant mode, the integrated full-bridge inverter supports 8W power transfer utilizing the P902x Receiver family, and ensures efficient switching with EMI/RFI emissions that are better than the requirements of the WPC specification.

To safeguard the device and the system under fault conditions, the P9038 offers resistor programmable Foreign Object Detection, built-in Over-Current protection, and programmable Over-Voltage / Over-Temperature protection. This transmitter is extremely easy to use and provides a complete WPC-compliant solution with minimum external parts count, requiring significantly less board space and lower total solution cost than competing products.

The P9038 is available in a compact 7 x 7 mm VFQFPN package, and it is rated for -40° to +85°C temperature range.

Typical Application Circuit



Note : External EEPROM is mandatory

Absolute Maximum Ratings

Stresses above the ratings listed below (Table 1 and Table 2) can cause permanent damage to the P9038. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 1: Absolute Maximum Ratings Summary. (All voltages are referred to ground.)

Pins	Rating	Units
VBUS_SNS	-0.3 to 27	V
$\overline{EN}$, IN, REG_IN, SW1, SW2, ISNSN_IN, ISNSP_IN	-0.3 to 12.5	V
GPIO_6:0, SCL, SDA, RESET, DP, DM, NC, NC1, NC2, NC3, SHIELD2, LDO5V, LDO2P5V_IN, INV5V_IN, VFOD_SNS, ISNS, HPF, OVP_SEL, ISNS_V	-0.3 to 5.5	V
BST1, BST2	-0.3 to SW+6	V
GATE	-0.3 to REG_IN+6	V
GND, REFGND, PGND1, PGND2	±0.3	V
SHIELD1	-0.3 to 8	V
LDO2P5V	-0.3 to 2.75	V

Table 2: Package Thermal Information[1,2,3]

Symbol	Description	Rating (VFQFPN)	Units
Θ_{JA}	Thermal Resistance Junction to Ambient	25.5	°C/W
Θ_{JC}	Thermal Resistance Junction to Case	8.6	°C/W
Θ_{JB}	Thermal Resistance Junction to Board	2.4	°C/W
T_J	Operating Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

NOTES:

1. The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \Theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.
2. This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.
3. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3: ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins	±2000	V
CDM	All pins	±500	V

Electrical Specifications Table

Table 4: Device Characteristics

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IN} = 40µF, Coil = A11, C_S = 400nF, T_A = -40° to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Input Supplies & UVLO						
V_{BUS}	Input Operating Range	VBUS_MIN to OVP_Max	4.5		6.9	V
I_{IN_REGIN}[2]	Standby Input Current (no ping)	After power-up sequence complete. No coil, no switching at SW1, SW2, LDO5V, LDO2P5V. REG_IN = 6.9V		8	12	mA
	Standby Input Current (pinging)	After power-up sequence complete. Average including pinging.		15		mA
	Sleep Mode Input Current	$\overline{EN}$= REG_IN = 6.9V			600	uA
$I_{IN_VBUS_SNS}$	VBUS_SNS Input Current	VBUS_SNS = 6.9V			1	mA
V_{REGIN_UVLO}	REGIN Under-Voltage Protection Trip Points	Rising			4.1	V
		Falling	3.4			V
		Hysteresis	150			mV
Full Bridge PWM Generators						
F_{SW}	Switching Frequency		110		205	kHz
F_{SW} LSB	Switching Frequency Step Size			12.5		ns
Duty[4]	Duty Cycle	V_{REG} = 4.5V-6.9V	10	50	90	%
Full Bridge Inverter						
$I_{HS_OCP_RNG}$	Over-Current Protection Trip Point Range	V_{IN} = 5V, cycle-by-cycle protection, programmable range	3		15	A
$I_{HS_OCP_ACC}$	Over-Current Protection Trip Point Accuracy	V_{IN} = 5V, OCP Setting = 5A	-20		20	%
Input OVP, Inrush Control, and Current Limit						
V_{BUS_OVP}	V_{BUS} Over-Voltage Protection Trip Point	V_{BUS} rising, OVP_SEL pin grounded	6.7	7.15		V
		V_{BUS} rising, OVP_SEL pin 220k 5% to GND	5.8	6.3		V
		V_{BUS} rising, OVP_SEL pin floating	7.3	7.85		V
		Hysteresis	200			mV
V_{REG_OVP}	REG_IN Over-Voltage Protection Trip Point	V_{REG_IN} rising	9.3		9.8	V
T_{GATE_RISE}	GATE Voltage Rise Time	V_{BUS} = 5V, Gate cap = 4nF V_{GATE} = 1V to V_{IN}+4V		3.6		ms
D_{GATE_FALL}	Delay from input OVP to GATE Voltage Pull-down	V_{GATE} Pull down Time, Gate cap = 4nF V_{GATE} = V_{IN}+4V to V_{IN}		400		ns
I_{GATE_LKG}	GATE Leakage	VBUS_SNS = 0V, REG_IN = 5V, V_{GATE} = 10V	-1		+1	µA

Symbol	Description	Conditions	Min	Typ	Max	Units
Input Average Current Sense						
$ISEN_{IR}$	Input Range	ISNSP_IN, ISNSN_IN	REGIN -0.3V	-	REGIN +0.15V	V
$ISEN_{ACC}$	Current Sense Accuracy	V_{REGIN} = 4.5 to 7.2V, I_{SENSR} = 1.5A, Note 1		+/- 3		%
LDO2P5V[3]						
V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}
V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}
I_{OUT_MAX}	I_{OUT_MAX}	I_{OUT_MAX}	I_{OUT_MAX}	I_{OUT_MAX}	I_{OUT_MAX}	I_{OUT_MAX}
LDO5V[3]						
V_{IN}	Input Voltage		4.5		6.9	V
V_{OUT}	Output Voltage	I_{LOAD} = 10mA, REG_IN = 5.5		5		V
I_{OUT_MAX}	Maximum Output Current				10	mA
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Threshold Rising		140		°C
		Threshold Falling		110		°C
$\overline{EN}$						
V_{IH}			1.1			V
V_{IL}					0.3	V
$I_{\overline{EN}}$	$\overline{EN}$ Input Current	$V_{\overline{EN}}$ = 6.9V			25	µA
General Purpose Inputs / Outputs (GPIO) [5]						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
V_{OH}	Output Logic High	I_{OH} = -8mA	4			V
V_{OL}	Output Logic Low	I_{OL} = 8mA			0.5	V
RESET						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
DP/DM CHARGER DETECTION						
V_{DP_SRC} V_{DM_SRC}	DP and DM Voltage Source			0.6		V
	DP and DM Voltage Source Output Source Current	V_{DP} or V_{DM} between 0.5V and 0.7V	250			µA
	DP and DM Voltage Source Output Sink Current	V_{DP} or V_{DM} at 2.2V			500	µA
IDP_SINK IDM_SINK	Current Sink		25	100	175	µA
IDP_SRC	Current Source		7		13	µA

Symbol	Description	Conditions	Min	Typ	Max	Units
VDAT_REF	Data Detect Voltage		0.25		0.4	V
VDP/DM_LGCHI	Logic High		2.0			V
VDP/DM_LGCLO	Logic Low				0.8	V
RDP_DWN	Pull-down Resistance		14.25	19.5	24.8	kΩ
CI	Input Capacitance	Dm pin, Switch Open		4.5	5	pF
		Dp pin, Switch Open		4.5	5	pF
IILK	Input Leakage	Dm pin, Switch Open V = 5.0	-1		+1	µA
		Dp pin, Switch Open V = 5.0	-1		+1	µA
SCL, SDA (I^2C Interface)						
f_{SCL_MSTR1}	f_{SCL_MSTR1}	f_{SCL_MSTR1}	f_{SCL_MSTR1}	f_{SCL_MSTR1}	f_{SCL_MSTR1}	f_{SCL_MSTR1}
f_{SCL_MSTR2}	f_{SCL_MSTR2}	f_{SCL_MSTR2}	f_{SCL_MSTR2}	f_{SCL_MSTR2}	f_{SCL_MSTR2}	f_{SCL_MSTR2}
f_{SCL_SLV}	Clock Frequency	P9038 as Slave	0		400	kHz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time	I^2C-bus Devices	10			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU:STA}$	Set-up Time for Repeated START Condition		100			ns
t_{BUF}	Bus Free Time between STOP and START Condition		1.3			µs
C_B	Capacitive Load for each Bus Line				100	pF
C_{BIN}	SCL, SDA Input Capacitance[5]			5		pF
V_{IL}	Input Threshold Low				0.4	V
V_{IH}	Input Threshold High		1.4			V
I_{LKG}	Input Leakage Current	V = 0V & 5V	-1.0		1.0	µA
V_{OL}	Output Logic Low (SDA)	I = 2mA			0.25	V

NOTES:

1. 10mΩ, 1% or better sense resistor is required to meet the FOD specification
2. This current is the sum of the input currents for REG_IN, IN, ISNSP_IN, ISNSN_IN, and EN_B.
3. 3.For internal use - do not externally load.
4. Guaranteed by Design.
5. Any of the GPIO pins is capable of sourcing 8mA. The GPIO connected to the ADC have a max operating input voltage of 2.4V to prevent saturation of the ADC.

Typical Performance Characteristics

Figure 1. System Efficiency vs. Load Circuit

V_{IN} = 5V, V_{OUT} = 5.3V, Spacer = 3.7mm, Cs = 247nF, T_A = 25°C
Measured using the P9025AC-R-EVK V1.0 (receiver) and P9038-EVK V1.0 (transmitter) reference boards.

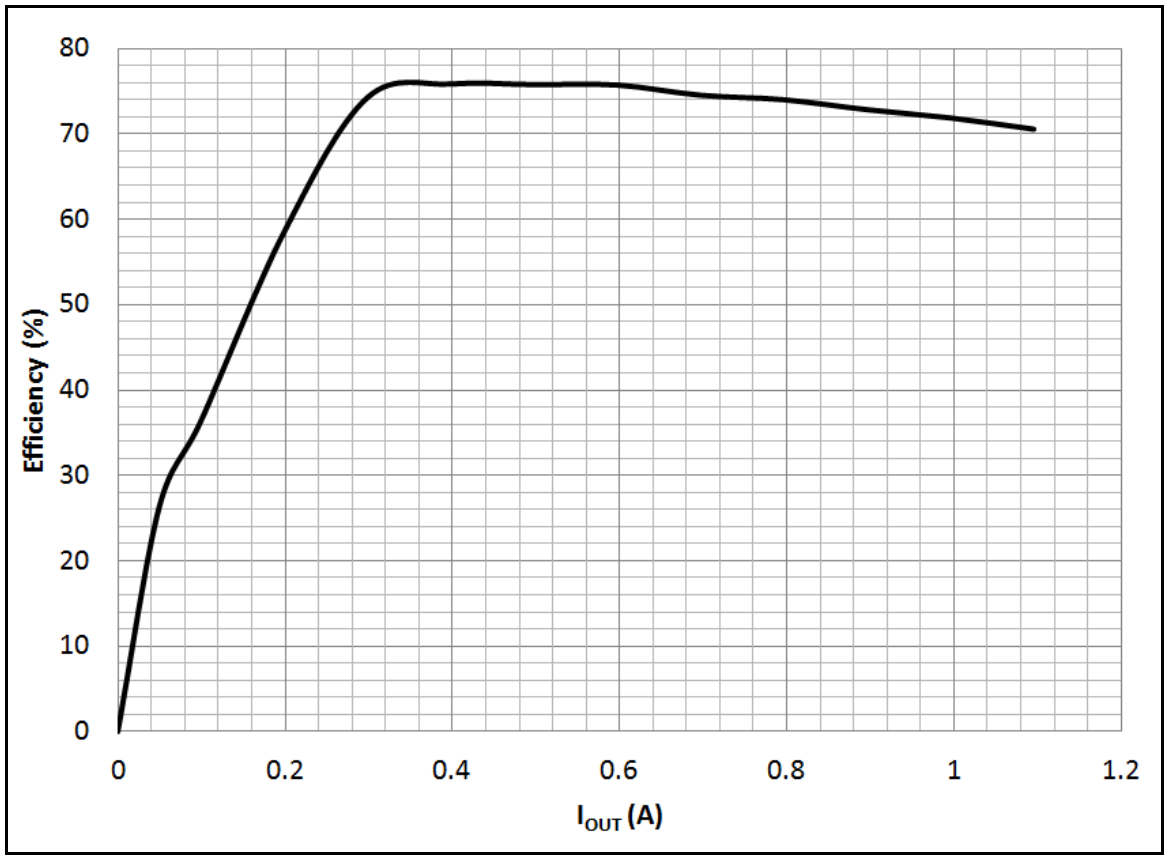
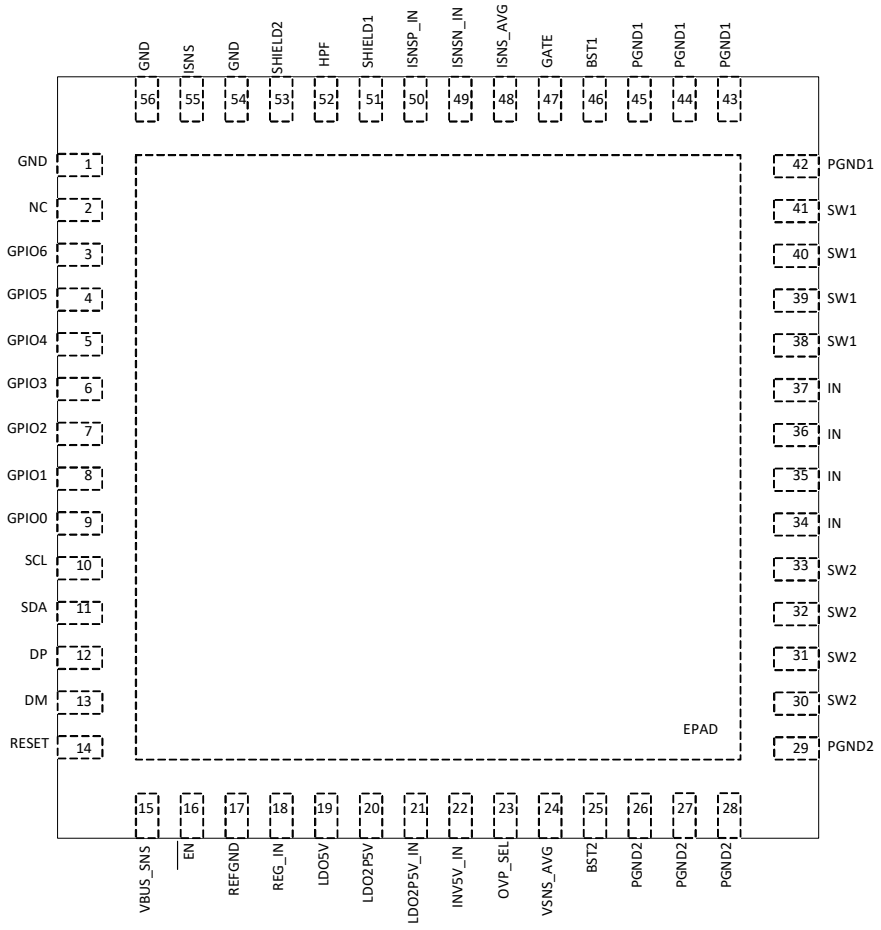


Table 5: P9038 No Load vs Receiver I_{OUT} = 1A, T_A = 25°C

Input Voltage	Temp (°C) No Load	Temp (°C) 1A Load	Temp. Change
4.5V	34.7	37.2	2.5
5.0V	34.9	37.4	2.5
5.5V	35.2	38.5	3.3

Pin Configuration

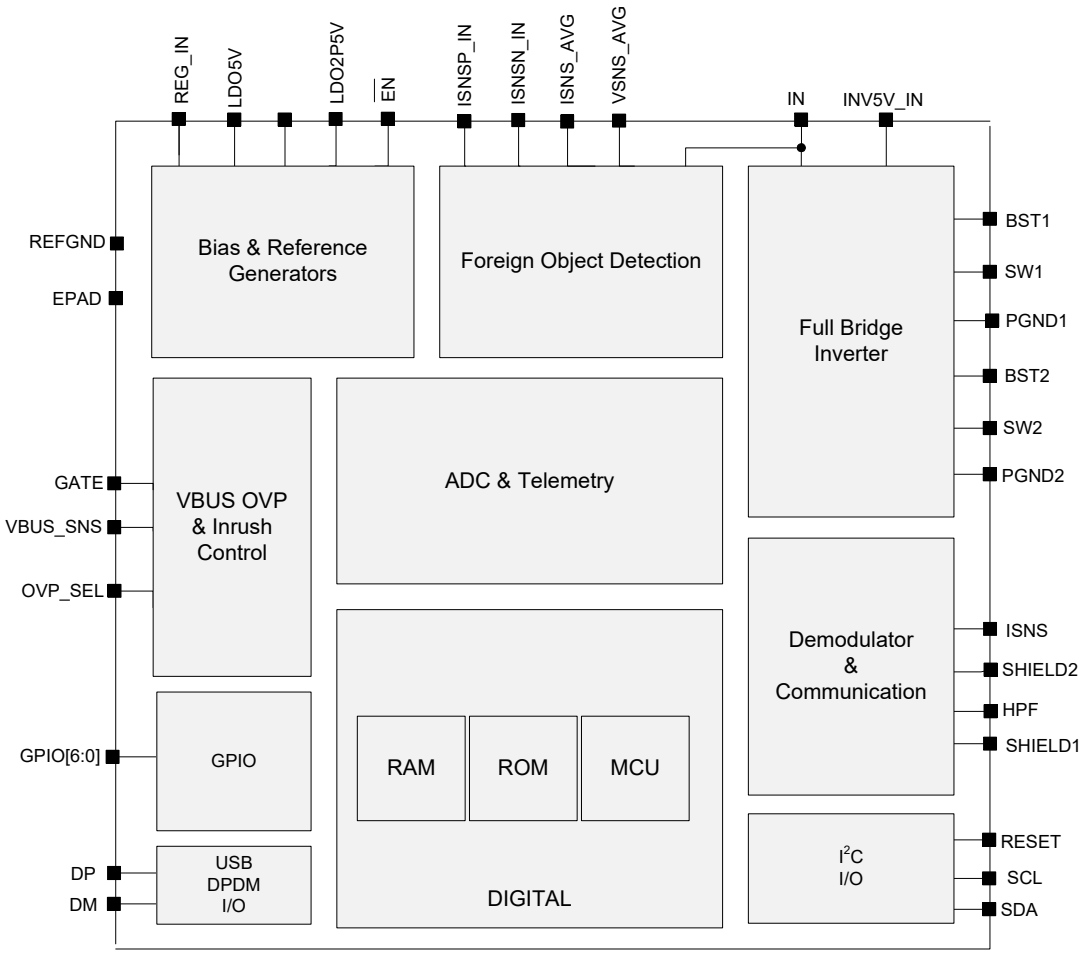


Pin Descriptions

Pin #	Name	Type	Function
1	GND	I	Signal Ground Connection.
2	NC	–	Do not connect. Internally connected.
3	GPIO6	I/O	General Purpose Input/Output.
4	GPIO5	I/O	General Purpose Input/Output.
5	GPIO4	I/O	General Purpose Input/Output.
6	GPIO3	I/O	General Purpose Input/Output.
7	GPIO2	I/O	General Purpose Input/Output.
8	GPIO1	I/O	General Purpose Input/Output.
9	GPIO0	I/O	General Purpose Input/Output.
10	SCL	I	I^2C Clock.
11	SDA	I/O	I^2C Data.
12	DP	I/O	USB Data Positive Input. If not used, the pin can be floating.
13	DM	I/O	USB Data Negative Input. If not used, the pin can be floating.
14	RESET	I	Active-high Reset Pin. Connect a 47KΩ to GND or tie directly to GND if not used.
15	VBUS_SNS	I	VBUS OVP sense point & provides bias for OVP circuitry.

Pin #	Name	Type	Function
16	$\overline{EN}$	I	Active-low Enable Pin. Connect a 47KΩ to GND or tie directly to GND if chip is always enabled.
17	REFGND	PWR	Signal Ground Connection. Connect to AGND.
18	REG_IN	I	Input Voltage for the internal 5V linear regulator. Connect a 1µF capacitor from this pin to GND.
19	LDO5V	O	5V LDO Output. Connect a 1µF Capacitor from this pin to GND.
20	LOD2P5V	O	2.5V LDO Output. Connect a 1µF Capacitor from this pin to GND.
21	LDO2P5_IN	PWR	Input Voltage for the internal 2.5V linear regulator. This pin must be connected to LDO5V (pin 19).
22	INV5V_IN	PWR	Input power to the internal driver circuitry. Connect a 1µF capacitor from this pin to GND.
23	OVP_SEL	I	Input over-voltage protection selection. When connected to GND, the nominal OVP threshold is set to 7.15V. When floating, 7.85V. Connecting the pin through a 220KΩ resistor to GND sets the OVP to 6.3V.
24	VSNS_AVG	I	Input voltage sense averaging pin. Connect a 6.8nF capacitor from this pin to AGND.
25	BST2	I	Bootstrap pin for SW2 Bridge Node. Connect a 0.1uF capacitor from this pin to SW2 pin.
26,27,28,29	PGND2	GND	Power Ground.
30,31,32,33	SW2	O	H-Bridge Switch Node 2.
34,35,36,37	IN	I	Power Supply Input Voltage. Connect two 22µF capacitors from the pins to GND.
38,39,40,41	SW1	O	H-Bridge Switch Node 1.
42,43,44,45	PGND1	GND	Power Ground.
46	BST1	I	Bootstrap pin for SW1 Bridge Node. Connect a 0.1uF capacitor from this pin to SW1 pin.
47	GATE	O	Output gate driver for the external FET. Connect a 6.8nF capacitor in parallel with 10MΩ from this pin to GND to configure soft-start.
48	ISNS_AVG	I	Input current sense averaging pin. Connect a 1nF capacitor from this pin to AGND.
49	ISNSN_IN	I	Input Current Sense amplifier inverting Input.
50	ISNSP_IN	I	Input Current Sense amplifier non-inverting Input.
51	SHIELD1	O	Shield output to guard DC voltage on HPF pin. Connect a 10MΩ resistor to GND.
52	HPF	I	High Pass Filter Input for Demodulator. Connect to an external high pass filter.
53	SHIELD2	O	Shield output to guard DC voltage on HPF pin. Leave this pin floating.
54	GND	I	Signal Ground Connection.
55	ISNS	O	Coil current sense output, connected to external demodulation circuit.
56	GND	I	Signal Ground Connection.
EP	EP	GND	Exposed Pad. Connect to GND.

Block Diagram



Description of the Wireless Power Charging System

A wireless charging system is comprised of a base station (transmitter) and a secondary coil (receiver) positioned against each other allowing power to be transferred magnetically. A WPC transmitter may be a free-positioning or magnetically-guided type. A free-positioning type of transmitter has an array of coils that gives limited spatial freedom to the end-user, whereas a magnetically-guided type of transmitter helps the end-user align the receiver to the transmitter with a magnetic attraction.

The amount of power transferred to the Wireless charging device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The communication is digital, and communication of 1's and 0's is achieved by the Rx modulating the amount of load on the receiver coil.

To conserve power, the transmitter places itself in a very-low-power sleep mode unless it detects the presence of a receiver. Once a receiver is detected, the transmitter exits sleep mode and begins the power transfer per the WPC specification.

Input Capacitors

Improper selection of the decoupling capacitor will degrade the electrical performance of the P9038. The REG_IN and IN_A to IN_D are the supply rails with nominal operating range of 4.5V to 6.9V powering the internal drivers and the full bridge inverter, respectively. At full load, the current through these pins are both high and fast switching.

Typically, three 10µF and one 0.1µF ceramic capacitor across the IN_A to IN_D pins are recommended. Similarly, for REG_IN, a 1µF in parallel with 0.1µF capacitors are sufficient.

Prior to selecting the capacitor, always examine the capacitor's DC voltage coefficient characteristics as the value of the capacitors will decrease due to capacitance-to-applied voltage characteristics of the commonly-used ceramic dielectrics. For example, a 22µF X7R 6.3V capacitor's value can actually be 6µF when operating at 5V, depending on the manufacturer. Typically, 10V- or 16V-rated capacitors are required. It is typically best to select these capacitors with a voltage rating from two to two and half times the expected applied voltage.

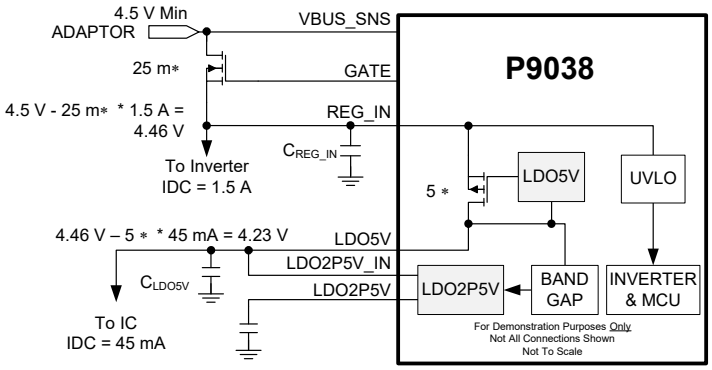
For optimum device performance, the decoupling capacitors must be mounted on the component side of the PCB, and also, located as physically close as possible to the related power pins and power ground (PGND).

LDO5V & LDO2P5V

The LDO5V and LDO2P5V are 5V and 2.5V linear regulators designed to power the internal circuitry. They can support maximum of 10mA and 5mA of load current, respectively. To stabilize the regulators, a 1µF capacitor from the output pin to GND must be connected.

The GATE pin and associated MOSFET shown in Figure 2 below provide protection to the P9038 from input over-voltage events and control current inrush. Both of these features are described in subsequent sections of this document.

Figure 2. Input Voltage Support Range (UVLO)



Full-bridge MOSFET Drive and MOSFET Current Sense

The P9038 incorporates an integrated full-bridge inverter. Each half-bridge contains a high-side current sense block that is used for control and for peak current protection. For EMI reduction purposes, the switching rising and falling rates of the internal MOSFETs are controlled.

Input Over-voltage Protection and In-rush Control

The P9038 offers additional protection in the event of input voltage transients and the programmable soft start time to minimize the inrush currents. The P9038 is powered from a VBUS input which may be subjected to voltages above 5.5V under normal operation. The P9038 is designed to support voltages as high as 27 V on this input. An external OVP MOSFET is used to isolate pins that would be damaged by a 27 V transient on the V_{BUS} input. The OVP MOSFET has a second function: limiting inrush current from the V_{BUS} line during startup. This is necessary due to the USB inrush specification and the large total effective capacitance (~40µF) on the REG_IN and IN pins of the IC.

The P9038 monitors the VBUS_SNS pin for over-voltage conditions and shuts off the OVP MOSFET to implement over-voltage protection. This OVP threshold can be configured via a single pin as shown in Table 6.

Table 6: V_{BUS} OVP Threshold Selection

OVP_SEL Pin Connection	OVP threshold
220kΩ to ground	6.3V
Grounded	7.15V
Floating	7.85V

A secondary over voltage protection with a 9.5V threshold is implemented on REG_IN for cases where the OVP MOSFET is not used. If the REG_IN threshold is exceeded, the P9038 is disabled until the REG_IN voltage drops below 8V.

Demodulation

Power transfer from the P9038 to a WPC-compliant wireless power receiver, such as P9025AC-R, is controlled by the receiver. Communication packets are superimposed on the power link between the two devices, and are demodulated by the P9038. Further information about the WPC communication protocol can be found at the WPC website. Communication can be made more robust by running traces from Shield1 and Shield2 along both sides of the HPF trace.

Analog-to-Digital Converter [ADC]

The ADC is the main functional block which the MCU uses for IC operation, including Foreign Object Detection. The ADC also digitizes several internal and external voltages and currents for overall system control and improved demodulation functionality.

USB DP/DM Functionality

The P9038 implements USB D+/D- detection derived from the BCS1.2 specification. This determines whether the USB power source is a Standard Port (such as from a computer) or a dedicated USB power supply Charger Port. When a Charger Port is detected, the P9038 will set its GPIO-5 pin to a logic-high state to indicate power is from a Charger Port. This information may be used for any purpose, but has no direct effect on the actual operation of the P9038.

Operation of the P9038 follows the commonly accepted practice in wireless charging to draw as much power as the source will allow. A Charger Port will provide its rated output, which is usually greater than the normal 500mA limit that could be typically expected from a Standard Port.

Foreign Object Detection and Input Over-current Protection

The P9038 makes precision measurements of the input voltage and input current, which are sampled by the internal ADC and processed in firmware for WPC 1.2.2 Foreign Object Detection [FOD] compliance. Two external pins, ISNS_AVG and VSNS_AVG, are provided for filtering the input current sense and input voltage sense signals respectively.

The input current sense signal is generated differentially from the ISNSP_IN and ISNSN_IN pins. This input current sense signal is filtered by an internal 50kΩ output resistor combined with an external capacitor on the ISNS_AVG pin.

Input voltage measurements are also filtered by an internal 33kΩ output resistor on the VSNS_AVG pin combined with an external capacitor on the VSNS_AVG pin. It is recommended to follow approximately the filter time constants used on the VSNS_AVG and ISNS_AVG signals as shown in the reference design to insure time alignment of the resulting measurements and accurate power calculation for FOD and other purposes.

External Chip Reset and $\overline{EN}$

The P9038 can be externally reset by pulling the RESET pin to a logic high (above the V_{IH} level).

The RESET pin is a dedicated high-impedance active-high digital input, and its effect is similar to the automatic power-up reset function. Because of the internal low voltage monitoring/ reset scheme, the use of the external RESET pin is not mandatory. When RESET is HIGH, the micro-controller's registers are set to the default configuration. When the RESET pin is released to a LOW, the micro-controller starts loading and executing the firmware from the program memory.

If the particular application requires the P9038 to be disabled, this can be accomplished with the $\overline{EN}$ pin.

When the $\overline{EN}$ pin is pulled high, the device is shuts off and placed in a very low current condition.When $\overline{EN}$ is connected to logic LOW, the device will become active, and the micro-controller starts loading and executing the firmware from the program memory.

The current into $\overline{EN}$ is approximately equal to:

$$I_{EN} = \frac{V_{EN} - 2}{300K}$$

or close to zero if $V_{(\overline{EN})}$ is less than 2V.

System Overview

For complete details of the WPC wireless power systems, refer to the WPC specifications and other materials at http://www.wirelesspowerconsortium.com.

The P9038 requires a minimum number of external components for proper operation. The provided reference design schematic and Bill-of-Materials component list enable a fully WPC “Qi Compliant” system. In addition to providing required LED indications, this system also provides optional buzzer indications (that could be used with an external piezoelectric buzzer device), and an thermistor over-temperature limit function and optional buzzer indications that are available to drive an external piezeoelectric buzzer device.

I²C Communication

The P9038 includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the P9038 will initially acts as an I²C Master for the purpose of downloading firmware from an external memory device, such as an EEPROM. The I²C Master mode on the P9038 does not support multi-master mode, and it is important for system designers to avoid any bus master conflict until the P9038 has finished any firmware uploading and has released control of the bus as I²C Master. After firmware downloaded from external memory is complete, and when the P9038 begins normal operation, the P9038 is configured by the standard firmware to be exclusively in I²C Slave mode.

For maximum flexibility, the P9038 tries to communicate with the first address on the EEPROM at 300kHz. If no acknowledge bit (ACK) is received, communication is attempted at the other addresses at 100kHz. If no EEPROM is present in the system, the P9038 will attempt to execute firmware from its internal ROM memory.

EEPROM

The P9038 EVK supports an external EEPROM memory chip, pre-programmed with a standard operating firmware that is automatically loaded when 5V power is applied. The P9038 uses I²C master address 0x52 to access the EEPROM. The P9038 slave address is 0x39.

External EEPROM is mandatory. Download the latest firmware from the P9038 product webpage and contact the EEPROM vendor to provide pre-programmed parts.

Overview of Standard GPIO Usage

There are 7 GPIOs on the P9038 transmitter IC. All GPIOs are configured as inputs during the power-on startup process. Firmware will then reconfigure the GPIO as follows:

- GPIO-0: This pin is not used in the standard firmware and is configured as active-low output during normal operation.
- GPIO-1: This pin is used to dynamically manage the optimum configuration of the external communication demodulation circuit.
- GPIO-2: This pin is connected to an external thermistor circuit which is used by P9038 to determine an external over-temperature condition
- GPIO-3: During power-on, this pin is sampled by the internal ADC to determine the resistor option setting for the LED mode. In normal operation, this pin is configured as an output to drive the Green LED indication functions (see Table 10).
- GPIO-4: During power-on, this pin is sampled by the internal ADC to determine the resistor option setting for adjusting the FOD offset value. In normal operation, this pin is configured as an output to drive the optional external piezoelectric buzzer function.
- GPIO-5: This pin is configured as an output to indicate the result of the USB D+/D- port type detection. If the USB port type is a Charger Port, then the output will be set to active-high. Otherwise, the output is set to active-low
- GPIO-6: This pin is configured as an output to drive the Red LED functions (see Table 7).

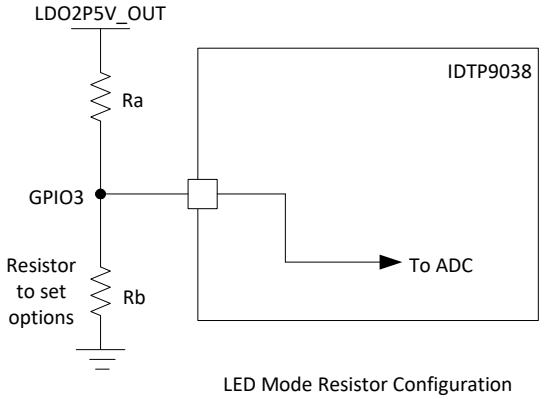
Table 7 lists how the red and green LEDs can be used to display information about the P9038's operating modes. This table also specifies how to configure the GPIO-3 optioning resistors to select the desired LED mode.

LED Functions

Depending upon the selected LED mode, one or two LEDs indicate the various functional states of the system including possible Fault conditions. Both single-LED and dual-LED indications are fully compliant with WPC requirements. Table 7 shows the various indications of all of the supported LED modes.

As shown in Figure 3 one or two resistors configure the desired LED option combinations in accordance with the values in Table 7. The DC voltage set in this way is measured one time during power-on to determine the LED configuration. To avoid inaccuracy of the resistor setting caused by the LED, the useful DC voltage range for all options except the highest value must be limited to not greater than 1Vdc.

Figure 3. P9038 LED Resistor Optioning



LED Mode Resistor Configuration

Table 7: P9038 LED Resistor Optioning[1,2]

LED Control Option	LED Select GPIO3 Voltage	Description	LED #/ Color	Operational Status				
				Standby	Transfer	Complete	Low-Power	Fault
1	Pull Down <=0.080V	Dual-LED, Standby - On Blink	LED1- Green	On	Blink 1Hz	On	Blink 2Hz	OFF
			LED2- Red	On	Off	Off	Off	Blink 4Hz
2	0.220V	Dual LED, Standby - On No-Blink	LED1- Green	On	On	Off	Blink 2Hz	OFF
			LED2- Red	On	Off	Off	Off	Blink 4Hz
3	0.370V	Single-LED, Standby OFF Blink	LED1- Green	Off	Blink 1Hz	On	Blink 2Hz	Blink 4Hz
			LED2- n/a	-	-	-	-	-
4	0.510V	Single-LED, Standby OFF No Blink	LED1- Green	Off	On	Off	Blink 2Hz	Blink 4Hz
			LED2- n/a	-	-	-	-	-
5	0.660V	Dual LED, Standby - Off No-Blink	LED1- Green	Off	On	Off	Blink 2Hz	Off
			LED2- Red	Off	Off	Off	Off	Blink 4Hz
6	0.810V	Dual LED, Standby - Off Red Indicate, No-Blink	LED1- Green	Off	Off	On	Off	Off
			LED2- Red	Off	On	Off	Blink 2Hz	Blink 4Hz
7	1.000V	Reserved	LED1- Green					
			LED2- Red					
8	1.100V	Reserved	LED1- Green					
			LED2- Red					
9	1.250V	Reserved	LED1- Green					
			LED2- Red					
10	Pull Up >=1.500V	Dual-LED, Standby - Off Blink	LED1- Green	Off	Blink 1Hz	On	Blink 2Hz	Off
			LED2- Red	Off	Off	Off	Off	Blink 4Hz

Note 1 - Voltage divider on GPIO3 should use 1% resistors with parallel impedance approximately 20k-50k.

"Low Power" is indicated in USB powered applications when USB does not provide sufficient DC power

"Low Power" Blink is approximately 80% on-time

Note 2 - LED Select voltage should be within ±3% of listed value.

Buzzer Function

An optional buzzer feature is supported on GPIO4 which is able to drive directly a piezoelectric type transducer without amplification. As shown on the reference schematic, a series current limiting resistor should be included if a buzzer device is included. The buzzer signal is approximately a 2kHz square wave, and it is recommended to use a buzzer with a 2kHz resonant frequency for best results.

Buzzer Action: Power Transfer Indication

The P9038 supports audible notification when the device operation successfully reaches the Power Transfer state. The duration of the Power Transfer indication sound is approximately 200ms.

Buzzer Action: Charge Complete Indication

The P9038 supports audible notification when the receiver sends a “Charge Complete” during the power transfer state. If “Charge Complete” is sent as the very first packet before being in the power transfer state, there is no buzzer indication for this case. The duration of the “Charge Complete” indication sound is approximately 200ms.

WPC TX-A5 and A11 Coils

The P9038 SW output pins are connected to a series-resonance circuit comprised of a WPC Type-A5 or A11 coil and a series resonant capacitor, as shown on the reference design schematic. The coil serves as the primary winding in a loosely-coupled transformer, the secondary of which is the coil connected to the power receiver

The power transmitter coil is mounted on a ferrite shield per the WPC specifications. Either a ground plane or grounded copper shielding can be added beneath the ferrite shield for a reduction in radiated electrical field emissions. The coil ground plane should be connected to the P9038 ground plane by a single trace.

Resonance Capacitors

The resonance capacitors must be C0G type dielectric and have a DC rating of at least 50V. The highest-efficiency combination is four 100nF in parallel to achieve the lowest ESR.

PCB Layout Considerations

For optimum device performance and lowest output phase noise, IDT recommends that customers copy the reference layout used in the P9038-R-EVK reference kit. More information and layout files can be found at: http://www.idt.com/P9038-R-EVK.

Additional layout guidelines can be found in application note, AN-894 P9038 Layout Guidelines. Users are encouraged to read this document prior to starting a board design.

Thermal Overload Protection

The P9038 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down and reset the P9038 if the die temperature exceeds 140°C. To enable the best performance, it is important to ensure that the heat generated by the P9038 is dissipated into the PCB and then carried away into the environment. The package exposed pad must be soldered to the PCB, with multiple vias evenly distributed under the exposed pad and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

Special Notes

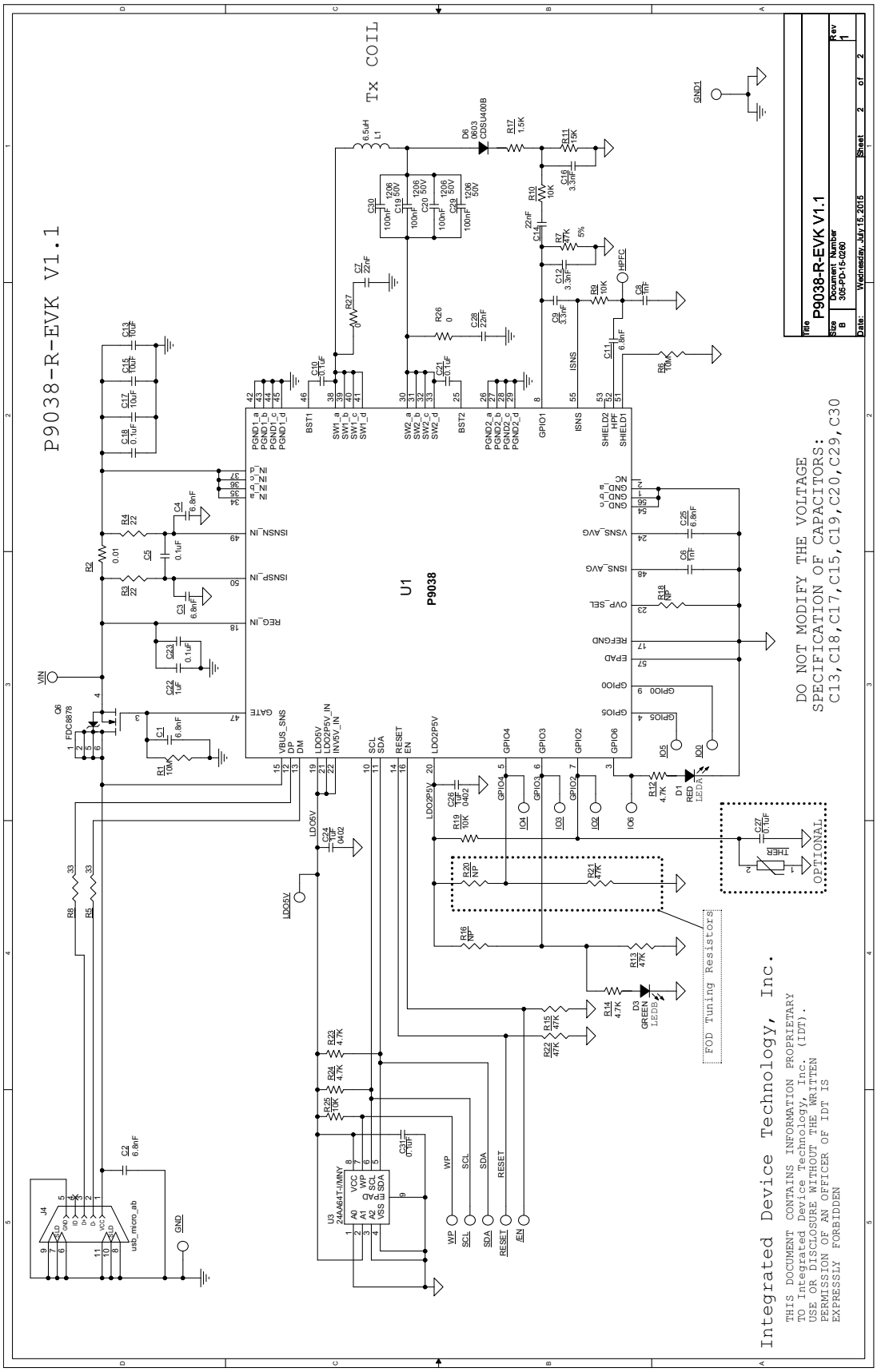
56-VFQFPN Package Assembly

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for minimum of 8 hours at 125°C within 24 hours of the assembly re-flow process.

Reference Schematic (P9038-R-EVK)

The reference schematic bill-of-materials can be found in the P9038-R-EVK reference board manual.

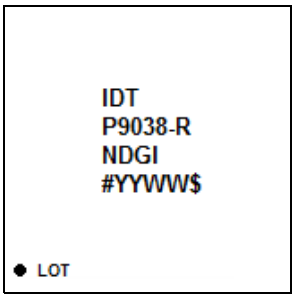


Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/ndndg56-package-outline-70-x-70-mm-body-epad-550mm-sq-040-mm-pitch-qfn

Marking Diagram



1. Lines 1 and 2 indicate the part number.
2. Line 3 indicates the following:
   - “#” denotes stepping.
   - “YY” is the last two digits of the year; “WW” is the work week number when the part was assembled.
   - “$” denotes the mark code.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
P9038-RNDGI	7 x 7 mm 56-VFQFPN	Tray	-40° to +85°C
P9038-RNDGI8	7 x 7 mm 56-VFQFPN	Tape and Reel	-40° to +85°C

Revision History

Date	Description of Change
July 26, 2018	- Added a note to “Typical Application Circuit” - Updated the second paragraph in “EEPROM” - Updated the “Package Outline Drawings”; however, no technical changes - Added “Marking Diagram”
August 1, 2016	Updated compatibility from WPC-1.1.2 to WPC-1.2.2.
August 19, 2015	Initial release.

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