

NP60N06PDK

60 V – 60 A – N-channel Power MOS FET

R07DS1296EJ0200 May 24, 2018

Application: Automotive

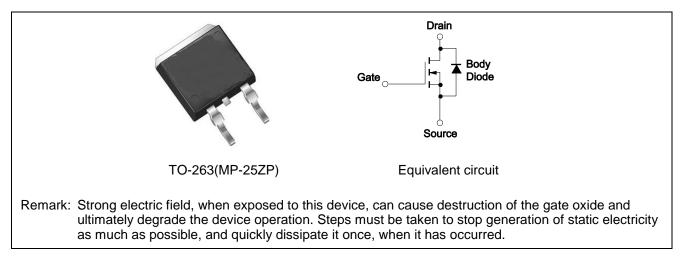
Description

NP60N06PDK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
- ---- $R_{DS(on)1} = 7.9 \text{ m}\Omega \text{ MAX}$. ($V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$)
- Low C_{iss} : $C_{iss} = 2400 \text{ pF TYP}$. ($V_{DS} = 25 \text{ V}$)
- Designed for automotive application and AEC-Q101 qualified

Outline



Ordering Information

Part No.	Lead Plating	Pac	Package		
NP60N06PDK-E1-AY *1	Pure Sn (Tin)	Topo 900 p/rool	Taping (E1 type)	TO-263(MP-25ZP)	
NP60N06PDK-E2-AY *1		Tape 800 p/reel	Taping (E2 type)	10-203(IMF-252F)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

RENESAS

Rev.2.00

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 V$)	V _{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) ($T_c = 25^{\circ}C$)	I _{D(DC)}	±60	A
Drain Current (pulse) *1*3	I _{D(pulse)}	±240	A
Total Power Dissipation ($T_C = 25^{\circ}C$)	P _{T1}	105	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	P _{T2}	1.8	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *2*3	I _{AR}	25	A
Repetitive Avalanche Energy *2*3	E _{AR}	63	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$ *3	1.43	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$ *3	83.3	°C/W

Notes: *1. T_C = 25°C, PW \leq 10 $\mu s,$ Duty Cycle \leq 1%

*2. R_G = 25
$$\Omega$$
, V_{GS} = 20 V \rightarrow 0 V

*3. Not subject of production test. Verified by design/characterization.



Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	V _{GS(th)}	1.5	2.1	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$
Forward Transfer Admittance *1	y _{fs}	30	54		S	$V_{DS} = 5 V, I_D = 30 A$
Drain to Source On-state	R _{DS(on)1}		6.4	7.9	mΩ	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$
Resistance *1	R _{DS(on)2}		7.0	12.0	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$
Input Capacitance *2	Ciss		2400	3600	pF	$V_{DS} = 25 V,$
Output Capacitance *2	Coss		230	350	pF	$V_{GS} = 0 V,$
Reverse Transfer Capacitance *2	C _{rss}		80	150	pF	f = 1 MHz
Turn-on Delay Time *2	t _{d(on)}		18	40	ns	$V_{DD} = 30 \text{ V}, \text{ I}_{D} = 30 \text{ A},$
Rise Time *2	tr		6	20	ns	Vgs = 10 V,
Turn-off Delay Time *2	t _{d(off)}		45	90	ns	R _G = 0 Ω
Fall Time *2	tr		3	10	ns	_
Total Gate Charge *2	Q _G		37	56	nC	$V_{DD} = 48 V,$
Gate to Source Charge	Q _{GS}		9		nC	V _{GS} = 10 V,
Gate to Drain Charge	Q _{GD}		8		nC	I _D = 60 A
Body Diode Forward Voltage *1	VF(S-D)		0.9	1.5	V	I _F = 60 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		32		ns	$I_F = 60 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Qrr		30		nC	di/dt = 100 A/µs

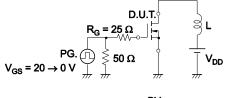
Electrical Characteristics (T_A = 25°C)

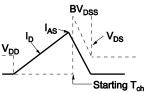
Note: *1. Pulsed test

Note: *2. Not subject of production test. Verified by design/characterization.

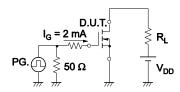
TEST CIRCUIT 1 AVALANCHE CAPABILITY

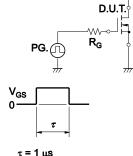
TEST CIRCUIT 2 SWITCHING TIME



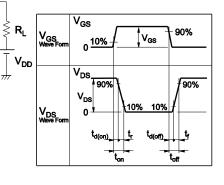


TEST CIRCUIT 3 GATE CHARGE



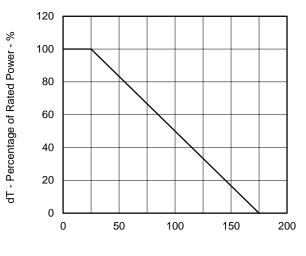






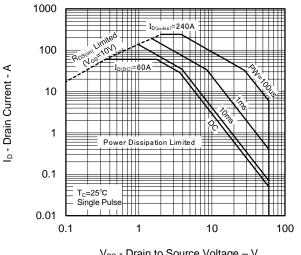
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

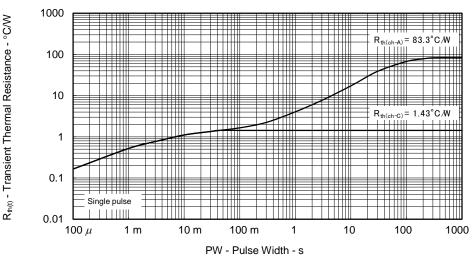


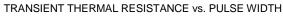
 T_{C} - Case Temperature - $^{\circ}C$





 V_{DS} - Drain to Source Voltage – V







TOTAL POWER DISSIPATION vs.

100

T_c - Case Temperature - °C

150

200

120

100

80

60

40

20

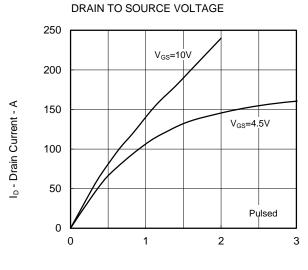
0

0

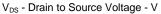
50

 $P_t - Total Power Dissipation - W$

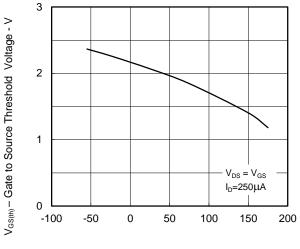
CASE TEMPERATURE



DRAIN CURRENT vs.

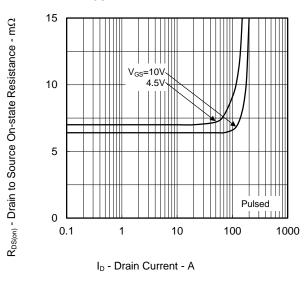


GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

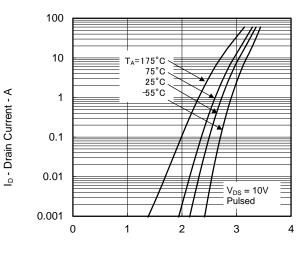


T_{ch} - Channel Temperature - °C

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

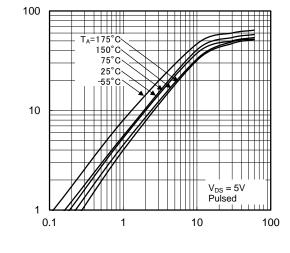


FORWARD TRANSFER CHARACTERISTICS

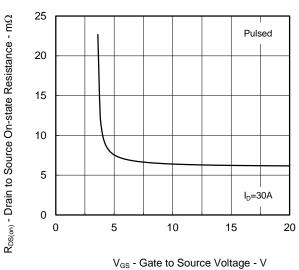


V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I_D - Drain Current - A

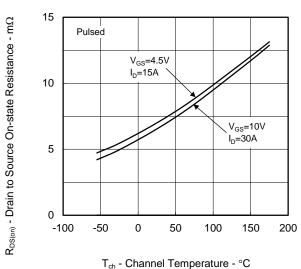


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

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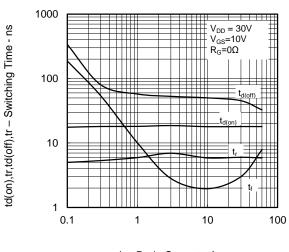


 $\mid y_{fs} \mid$ - Forward Transfer Admittance - S



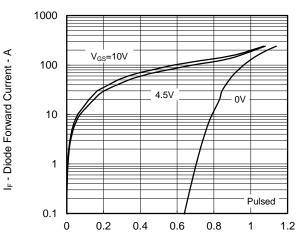
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

SWITCHING CHARACTERISTICS



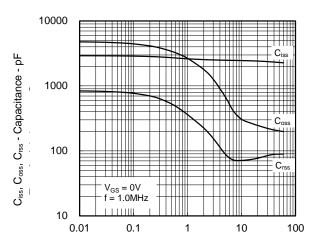
I_D - Drain Current - A

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



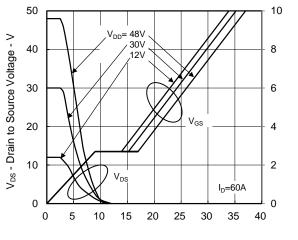
 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

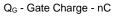
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



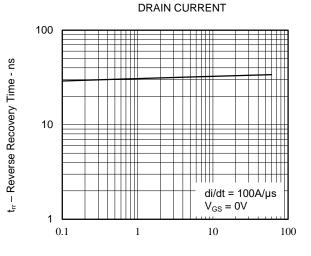








REVERSE RECOVERY TIME vs.

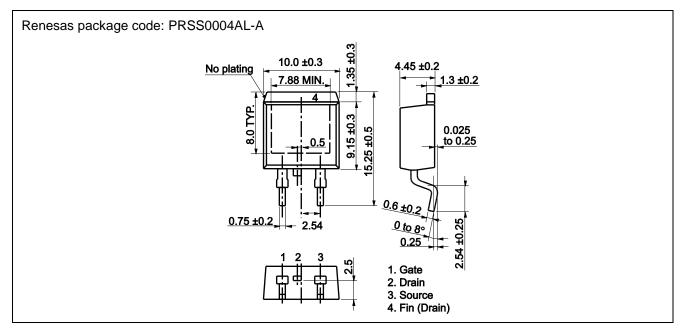


IF - Drain Current - A



Package Drawings (Unit: mm)

TO-263 (MP-25ZP) (Mass: 1.48 g TYP.)





Revision History

NP60N06PDK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Oct. 26, 2015	—	First Edition Issued	
1.01	Dec. 21, 2015	2	Modification of Repetitive Avalanche Energy(83mJ \rightarrow 63mJ)	
2.00	May 24 ,2018	2	Note 3 was added	
		3	Note 2 was added	

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