# NP36P06KDG

## -60V – -36A – P-channel Power MOS FET
## Application : Automotive

R07DS1524EJ0100
Rev.1.00
Jun. 24, 2022

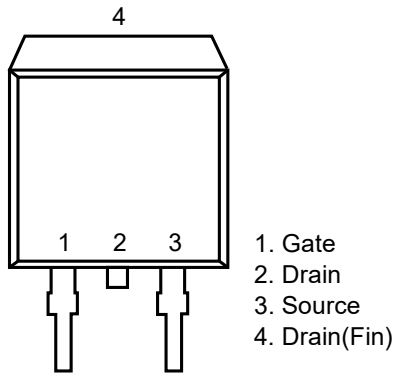
### Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

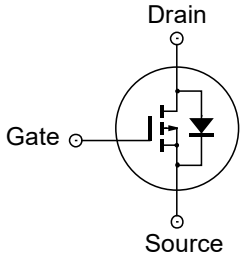
### Features

- Super low on-state resistance : $R_{DS(on)}$ = 29.5 mΩ Max. ( $V_{GS}$ = -10 V, $I_D$ = -18 A )
  $R_{DS(on)}$ = 37.5 mΩ Max. ( $V_{GS}$ = -4.5 V, $I_D$ = -18 A )
- Low input capacitance : Ciss = 3100 pF Typ.
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

### Outline




MP-25ZK (TO-263)




Equivalent circuit

### Absolute Maximum Ratings

($T_a$=25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | -60 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ∓20 | V |
| Drain Current (DC) ($T_c$ = 25 °C) | $I_{D(DC)}$ | ∓36 | A |
| Drain Current (pulse) | $I_{D(pulse)}$ Notes1 | ∓108 | A |
| Total Power Dissipation ($T_c$ = 25 °C) | $P_{T1}$ | 56 | W |
| Total Power Dissipation ($T_a$ = 25 °C) | $P_{T2}$ | 1.8 | W |
| Channel Temperature | $T_{ch}$ | 175 | °C |
| Storage Temperature | $T_{stg}$ | -55 to 175 | °C |
| Single Avalanche Current | $I_{AS}$ Notes2 | 23 | A |
| Single Avalanche Energy | $E_{AS}$ Notes2 | 54 | mJ |

Notes 1. PW ≤ 10 μs , Duty Cycle ≤ 1%
2. Starting $T_{ch}$=25℃ , $V_{DD}$ = -30V , $R_G$ = 25 Ω , $V_{GS}$ = -20 → 0V , L = 100μH

## Thermal Resistance

| | | | |
|---|---|---|---|
| Channel to Case Thermal Resistance | $R_{th(ch-c)}$ Notes3 | 2.68 | °C/W |
| Channel to Ambient Thermal Resistance | $R_{th(ch-a)}$ Notes3 | 83.3 | °C/W |

## Electrical Characteristics

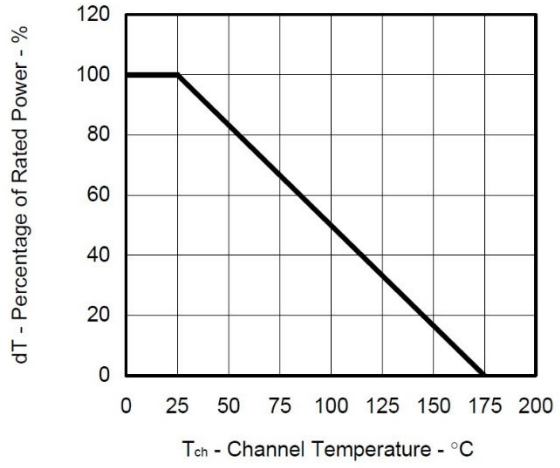
($T_a$=25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | — | -10 | μA | $V_{DS}$ = -60 V, $V_{GS}$ = 0 V |
| Gate Leakage Current | $I_{GSS}$ | — | — | ∓100 | nA | $V_{GS}$ = ∓ 20 V, $V_{DS}$ = 0 V |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | -1.0 | -1.6 | -2.5 | V | $V_{DS}$ = -10 V, $I_D$ = -1 mA |
| Forward Transfer Admittance | \| yfs \| Notes4 | 12 | 23 | — | S | $V_{DS}$ = -10 V, $I_D$ = -18 A |
| Drain to Source On-state Resistance | $R_{DS(on)1}$ Notes4 | — | 23.1 | 29.5 | mΩ | $V_{GS}$ = -10 V, $I_D$ = -18 A |
| | $R_{DS(on)2}$ Notes4 | — | 27.0 | 37.5 | mΩ | $V_{GS}$ = -4.5 V, $I_D$ = -18 A |
| Input Capacitance | $C_{iss}$ | — | 3100 | — | pF | $V_{DS}$ = -10 V |
| Output Capacitance | $C_{oss}$ | — | 350 | — | pF | $V_{GS}$ = 0 V |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 205 | — | pF | f = 1 MHz |
| Turn-on Delay Time | $t_{d(on)}$ | — | 8 | — | ns | $V_{DD}$ = -30 V |
| Rise Time | $t_r$ | — | 11 | — | ns | $I_D$ = -18 A |
| Turn-off Delay Time | $t_{d(off)}$ | — | 210 | — | ns | $V_{GS}$ = -10 V |
| Fall Time | $t_f$ | — | 110 | — | ns | $R_G$ = 0 Ω |
| Total Gate Charge | $Q_g$ | — | 54 | — | nC | $V_{DD}$ = -48 V |
| Gate to Source Charge | $Q_{gs}$ | — | 7 | — | nC | $V_{GS}$ = -10 V |
| Gate to Drain Charge | $Q_{gd}$ | — | 15 | — | nC | $I_D$ = -36 A |
| Body Diode Forward Voltage | $V_{F(S-D)}$ Notes4 | — | 0.98 | 1.5 | V | $I_F$ = -36 A, $V_{GS}$ = 0 V |
| Reverse Recovery Time | $t_{rr}$ | — | 43 | — | ns | $I_F$ = -36 A, $V_{GS}$ = 0 V |
| Reverse Recovery Charge | $Q_{rr}$ | — | 56 | — | nC | di/dt = -100 A/μs |

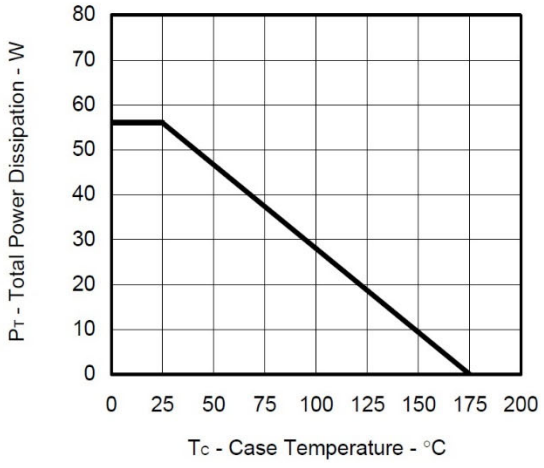
Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.
4. Pulse test.

## Typical Characteristics

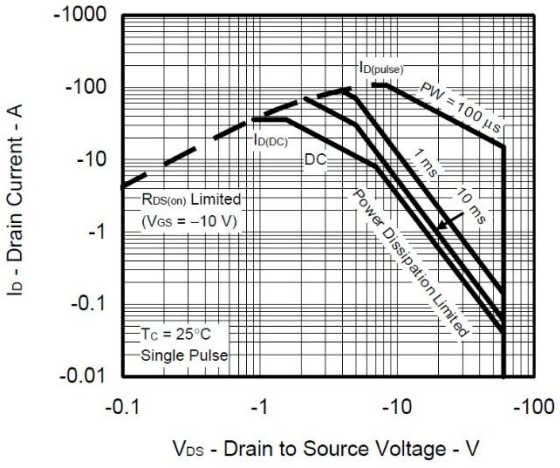
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



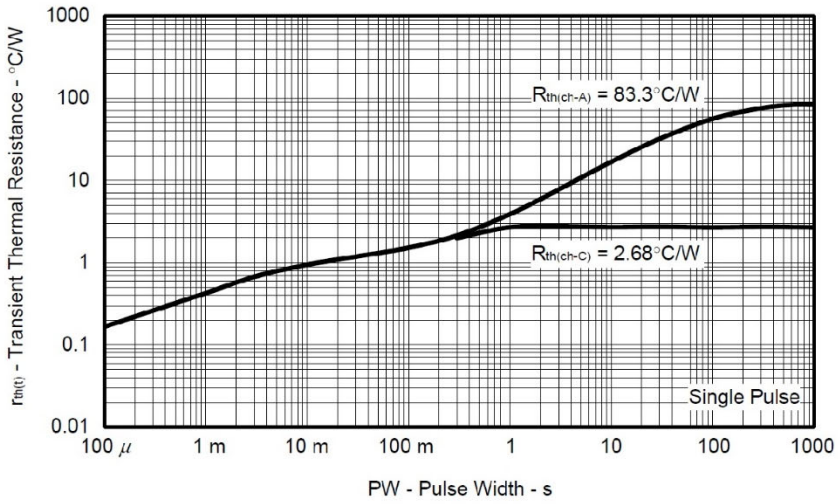

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



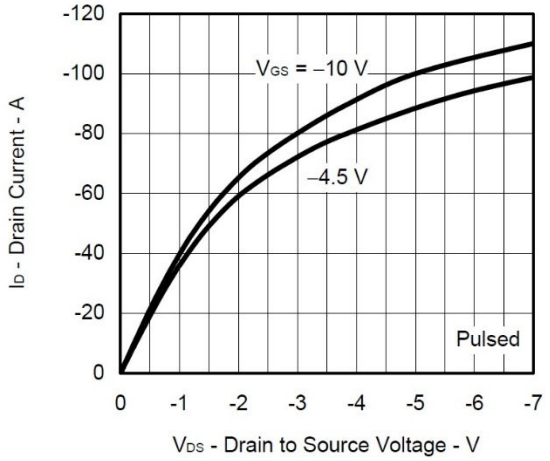

FORWARD BIAS SAFE OPERATING AREA



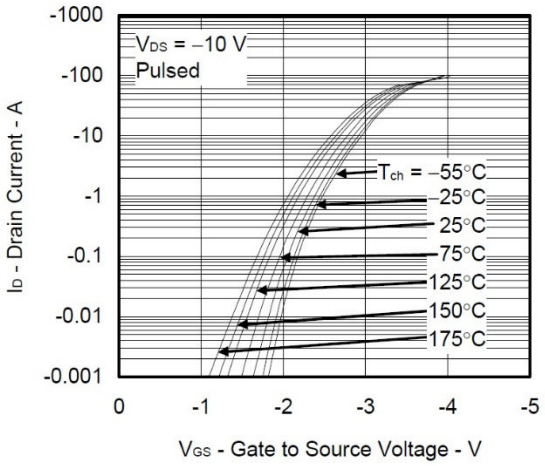

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



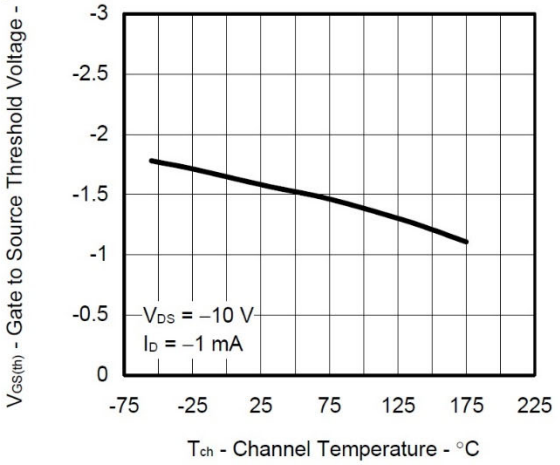
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



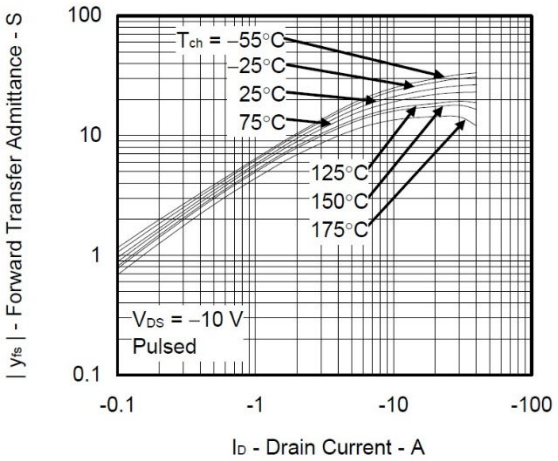

FORWARD TRANSFER CHARACTERISTICS



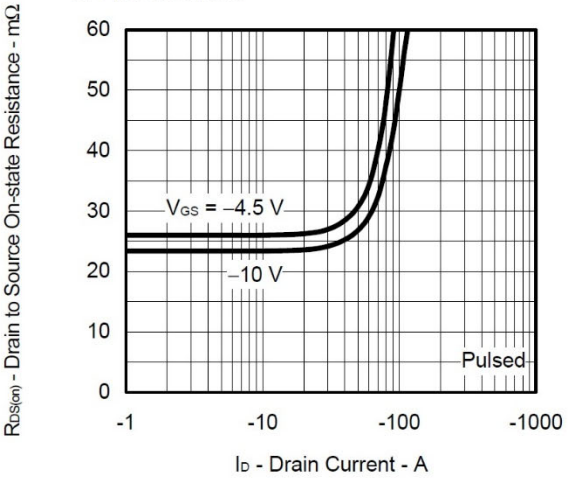

GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



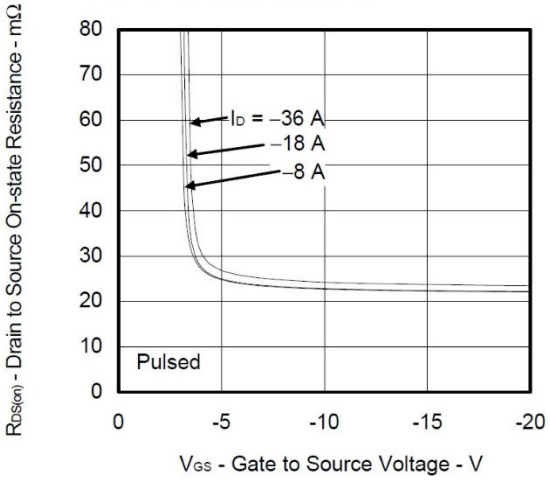

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



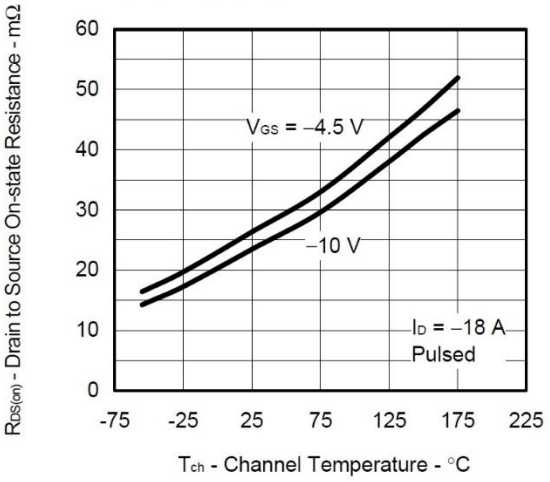

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



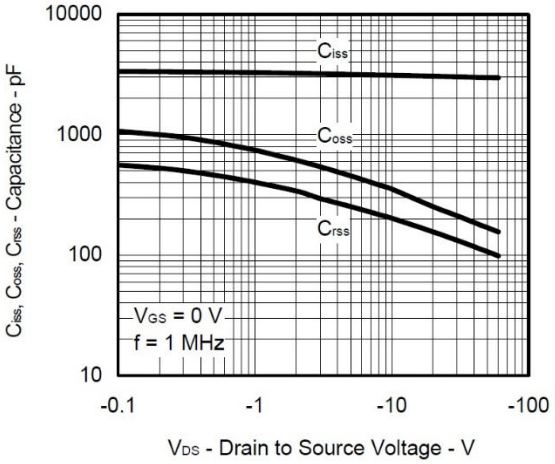

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



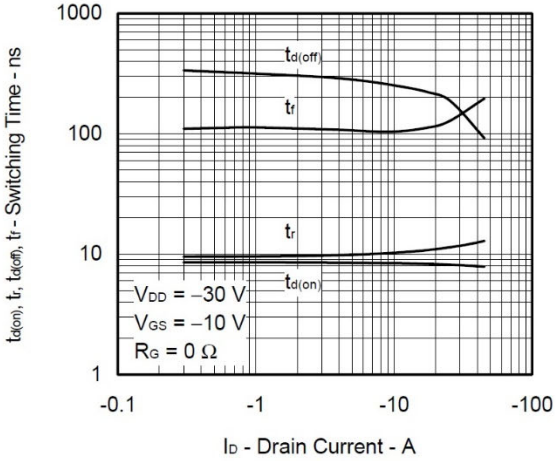
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



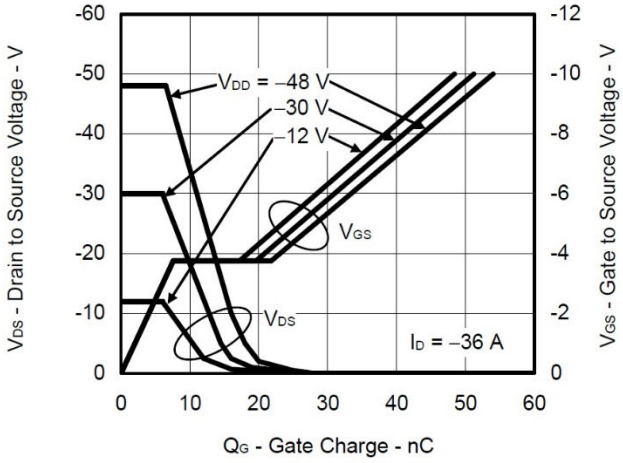

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



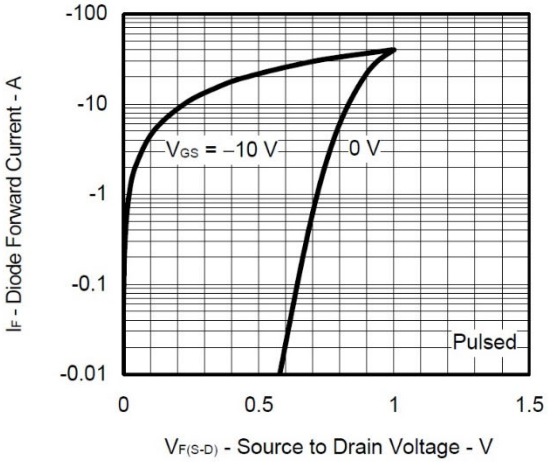

SWITCHING CHARACTERISTICS



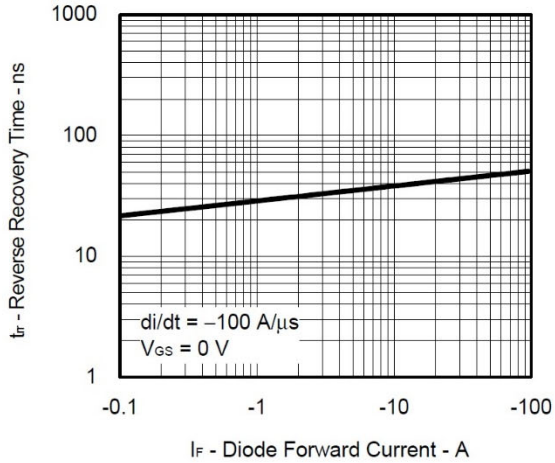

DYNAMIC INPUT/OUTPUT CHARACTERISTICS




SOURCE TO DRAIN DIODE FORWARD VOLTAGE



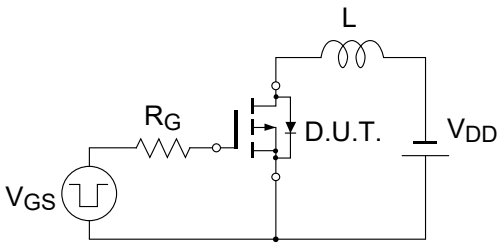

REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



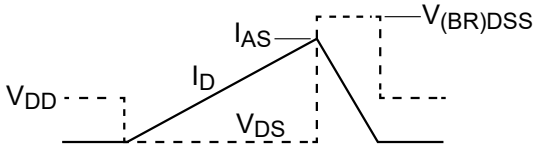
## Test Circuit

Avalanche

Test Circuit



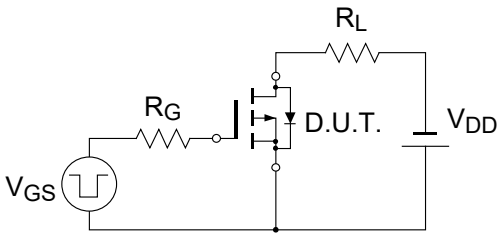

Waveform



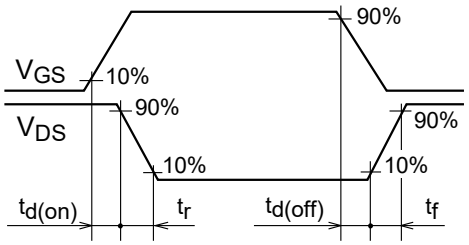

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

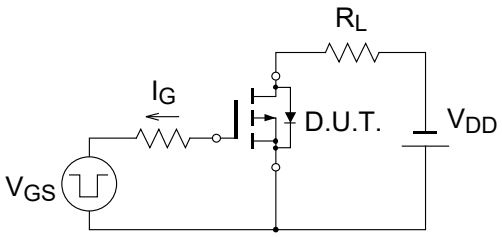



Waveform

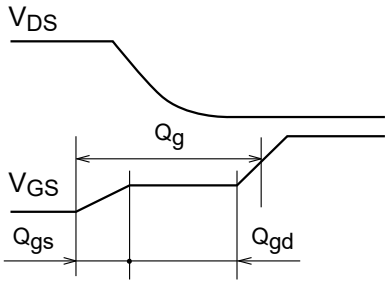



Gate Charge

Test Circuit

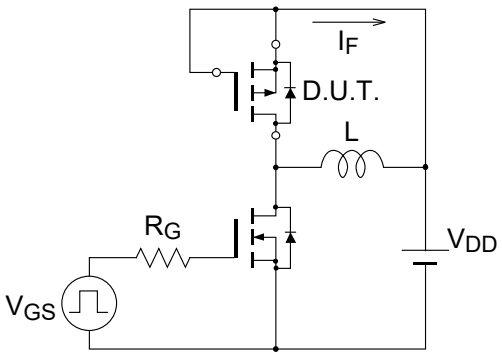



Waveform

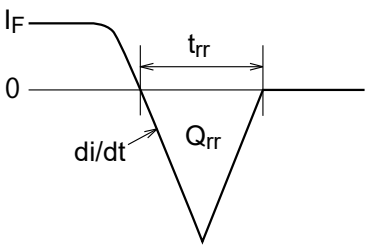



Reverse Recovery

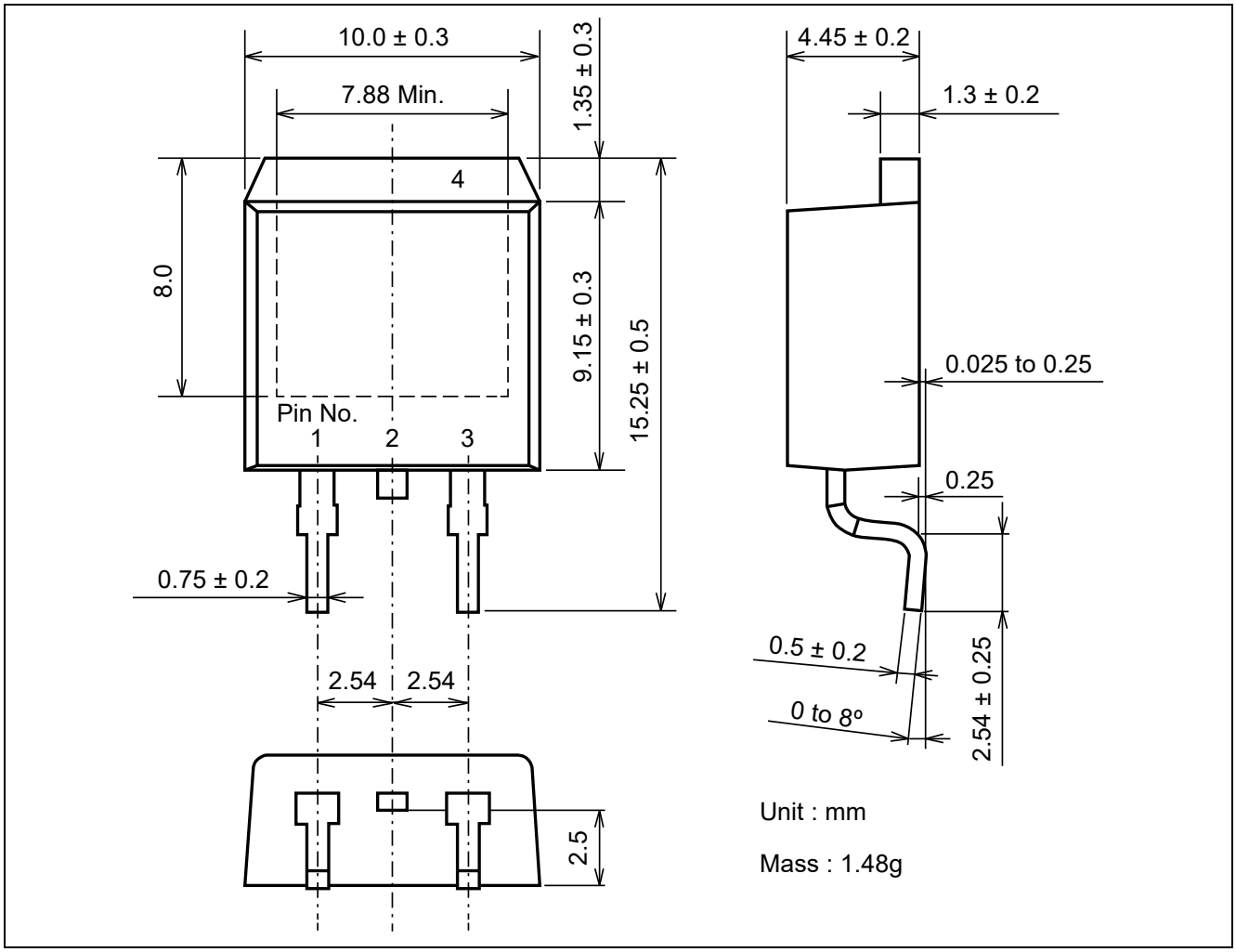
Test Circuit




Waveform



## Package Dimensions




## Ordering Information

| Part No. | Quantity | Shipping container |
|---|---|---|
| NP36P06KDG-E1-AY | 800pcs/reel | Taping |

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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