DATASHEET

# 3.3 V 1:14 LVCMOS PLL Clock Generator

The MPC9774 is a 3.3 V compatible, 1:14 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 125 MHz and output skews less than 175 ps the device meets the needs of the most demanding clock applications.

**Features**

- 1:14 PLL Based Low-Voltage Clock Generator
- 3.3 V Power Supply
- Internal Power-On Reset
- Generates Clock Signals Up to 125 MHz
- Maximum Output Skew of 175 ps
- Two LVCMOS PLL Reference Clock Inputs
- External PLL Feedback Supports Zero-Delay Capability
- Various Feedback and Output Dividers (See Applications Information)
- Supports Up to Three Individual Generated Output Clock Frequencies
- Drives Up to 28 Clock Lines
- Ambient Temperature Range 0°C to +70°C
- Pin and Function Compatible to the MPC974
- 52-Lead LQFP Package, Pb-free
- For drop in replacement use 87974

**MPC9774**

**3.3 V 1:14 LVCMOS PLL CLOCK GENERATOR**



**AE SUFFIX**
**52-LEAD LQFP PACKAGE**
**Pb-FREE PACKAGE**
**CASE 848D-03**
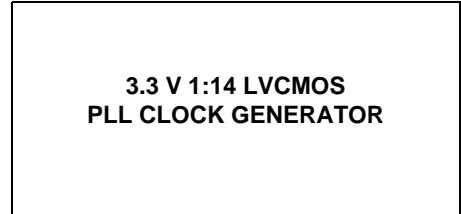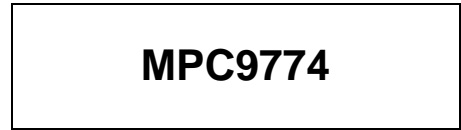
The MPC9774 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9774 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range.

The MPC9774 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 1:1, 2:1, 3:1, 3:2 and 3:2:1 can be realized. Additionally, the device supports a separate configurable feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_SEL pin provides an extended PLL input reference frequency range.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9774 has an internal power-on reset.

The MPC9774 is fully 3.3 V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9774 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is pin and function compatible to the MPC974 and is packaged in a 52-lead LQFP package.
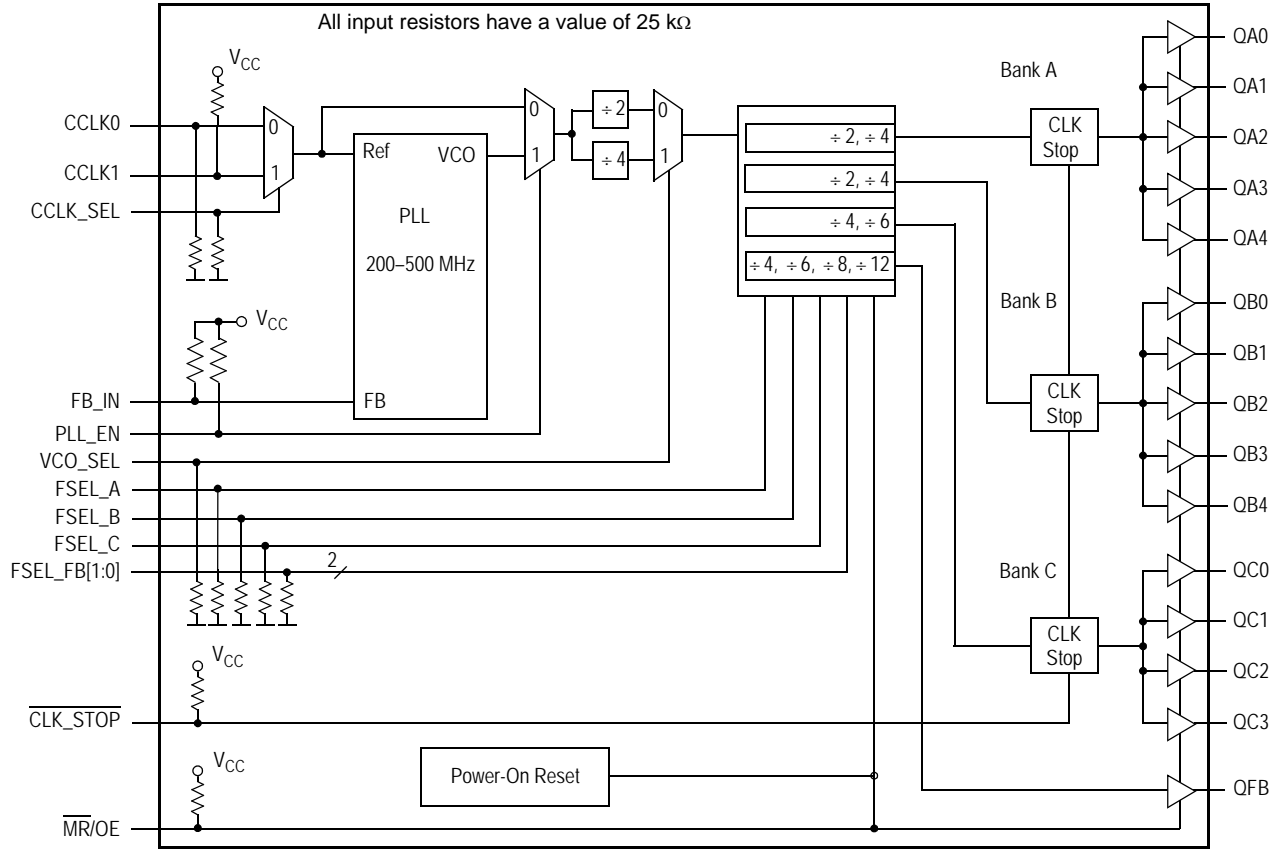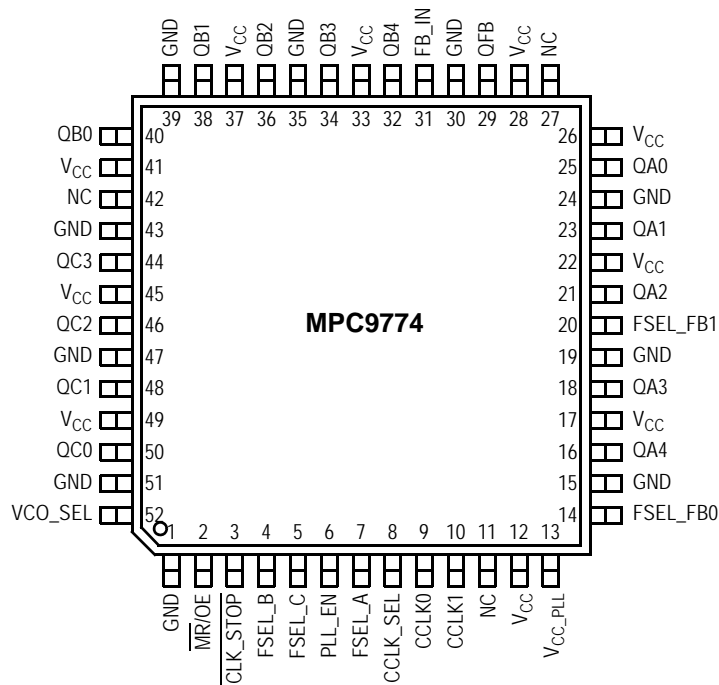
**Figure 1. MPC9774 Logic Diagram**



**Figure 2. MPC9774 52-Lead Package Pinout** (Top View)

**Table 1. Pin Configuration**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK0 | Input | LVCMOS | PLL reference clock |
| CCLK1 | Input | LVCMOS | Alternative PLL reference clock |
| FB_IN | Input | LVCMOS | PLL feedback signal input, connect to QFB |
| CCLK_SEL | Input | LVCMOS | LVCMOS clock reference select |
| VCO_SEL | Input | LVCMOS | VCO operating frequency select |
| PLL_EN | Input | LVCMOS | PLL enable/PLL bypass mode select |
| $\overline{MR}$/OE | Input | LVCMOS | Output enable/disable (high-impedance tristate) and device reset |
| $\overline{CLK\_STOP}$ | Input | LVCMOS | Output enable/clock stop (logic low state) |
| FSEL_A | Input | LVCMOS | Frequency divider select for bank A outputs |
| FSEL_B | Input | LVCMOS | Frequency divider select for bank B outputs |
| FSEL_C | Input | LVCMOS | Frequency divider select for bank C outputs |
| FSEL_FB[1:0] | Input | LVCMOS | Frequency divider select for the QFB output |
| QA[4:0] | Output | LVCMOS | Clock outputs (Bank A) |
| QB[4:0] | Output | LVCMOS | Clock outputs (Bank B) |
| QC[3:0] | Output | LVCMOS | Clock outputs (Bank C) |
| QFB | Output | LVCMOS | PLL feedback output. Connect to FB_IN. |
| GND | Supply | Ground | Negative power supply |
| $V_{CC\_PLL}$ | Supply | $V_{CC}$ | PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL}$. Please see applications section for details. |
| $V_{CC}$ | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |

**Table 2. Function Table (Configuration Controls)**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CCLK_SEL | 0 | Selects CCLK0 as PLL references signal input | Selects CCKL1 as PLL reference signal input |
| VCO_SEL | 0 | Selects VCO ÷ 2. The VCO frequency is scaled by a factor of 2 (high input frequency range) | Selects VCO ÷ 4. The VCO frequency is scaled by a factor of 4 (low input frequency range). |
| PLL_EN | 1 | Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9774 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. | Normal operation mode with PLL enabled. |
| $\overline{CLK\_STOP}$ | 1 | QA, QB an QC outputs disabled in logic low state. QFB is not affected by $\overline{CLK\_STOP}$. $\overline{CLK\_STOP}$ deassertion may cause the initial output clock pulse to be distorted. | Outputs enabled (active) |
| $\overline{MR}$/OE | 1 | Outputs disabled (high-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9774 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up. | Outputs enabled (active) |

### Table 2. Function Table (Configuration Controls)

| Control | Default | 0 | 1 |
|---|---|---|---|

VCO_SEL, FSEL_A, FSEL_B, FSEL_C and FSEL_FB[1:0] control the operating PLL frequency range and input/output frequency ratios. See Table 3 and Table 4 for the device frequency configuration.

### Table 3. Function Table (Output Dividers Bank A, B, and C)

| VCO_SEL | FSEL_A | QA[4:0] | VCO_SEL | FSEL_B | QB[4:0] | VCO_SEL | FSEL_C | QC[3:0] |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | VCO ÷ 4 | 0 | 0 | VCO ÷ 4 | 0 | 0 | VCO ÷ 8 |
| 0 | 1 | VCO ÷ 8 | 0 | 1 | VCO ÷ 8 | 0 | 1 | VCO ÷ 12 |
| 1 | 0 | VCO ÷ 8 | 1 | 0 | VCO ÷ 8 | 1 | 0 | VCO ÷ 16 |
| 1 | 1 | VCO ÷ 16 | 1 | 1 | VCO ÷ 16 | 1 | 1 | VCO ÷ 24 |

### Table 4. Function Table (QFB)

| VCO_SEL | FSEL_B1 | FSEL_B0 | QFB |
|---|---|---|---|
| 0 | 0 | 0 | VCO ÷ 8 |
| 0 | 0 | 1 | VCO ÷ 16 |
| 0 | 1 | 0 | VCO ÷ 12 |
| 0 | 1 | 1 | VCO ÷ 24 |
| 1 | 0 | 0 | VCO ÷ 16 |
| 1 | 0 | 1 | VCO ÷ 32 |
| 1 | 1 | 0 | VCO ÷ 24 |
| 1 | 1 | 1 | VCO ÷ 48 |

### Table 5. General Specifications

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD protection (Machine Model) | 200 | | | V | |
| HBM | ESD protection (Human Body Model) | 2000 | | | V | |
| LU | Latch-Up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 12 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

### Table 6. Absolute Maximum Ratings[1]

| Symbol | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.3 | 3.9 | V |
| $V_{IN}$ | DC Input Voltage | −0.3 | $V_{CC} + 0.3$ | V |
| $V_{OUT}$ | DC Output Voltage | −0.3 | $V_{CC} + 0.3$ | V |
| $I_{IN}$ | DC Input Current | | ±20 | mA |
| $I_{OUT}$ | DC Output Current | | ±50 | mA |
| $T_S$ | Storage Temperature | −65 | 125 | °C |

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 7. DC Characteristics** ($V_{CC}$ = 3.3 V ± 5%, $T_A$ = 0°C to +70°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC\_PLL}$ | PLL Supply Voltage | 3.02 | | $V_{CC}$ | V | LVCMOS |
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = −24 mA[1] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$ = 24 mA<br>$I_{OL}$ = 12 mA |
| $Z_{OUT}$ | Output Impedance | | 14 – 17 | | W | |
| $I_{IN}$ | Input Current[2] | | | ±200 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CC\_PLL}$ | Maximum PLL Supply Current | | 5.0 | 7.5 | mA | $V_{CC\_PLL}$ Pin |
| $I_{CCQ}$ | Maximum Quiescent Supply Current | | | 8.0 | mA | All $V_{CC}$ Pins |

1. The MPC9774 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-down or pull-up resistors affecting the input current.

**Table 8. AC Characteristics** ($V_{CC}$ = 3.3 V ± 5%, $T_A$ = 0°C to +70°C)[1]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $f_{REF}$ | Input Reference Frequency | ÷ 8 feedback | 25.0 | | 62.5 | MHz | PLL locked |
| | | ÷ 12 feedback | 16.6 | | 41.6 | MHz | |
| | | ÷ 16 feedback | 12.5 | | 31.25 | MHz | |
| | | ÷ 24 feedback | 8.33 | | 20.83 | MHz | |
| | | ÷ 32 feedback | 6.25 | | 15.625 | MHz | PLL bypass |
| | | ÷ 48 feedback | 4.16 | | 10.41 | MHz | |
| | Input Reference Frequency in PLL Bypass Mode[2] | | | | 250 | MHz | |
| $f_{VCO}$ | VCO Frequency Range[3] | | 200 | | 500 | MHz | |
| $f_{MAX}$ | Output Frequency | ÷ 4 output | 50.0 | | 125.0 | MHz | PLL locked |
| | | ÷ 8 output | 25.0 | | 62.5 | MHz | |
| | | ÷ 12 output | 16.6 | | 41.6 | MHz | |
| | | ÷ 16 output | 12.5 | | 31.25 | MHz | |
| | | ÷ 24 output | 8.33 | | 20.83 | MHz | |
| $t_{PW,MIN}$ | Input Reference Pulse Width[4] | | 2.0 | | | ns | |
| $t_R$, $t_F$ | CCLKx Input Rise/Fall Time | | | | 1.0 | ns | 0.8 to 2.0 V |
| $t_{(∅)}$ | Propagation Delay (static phase offset)[5]<br>CCLKx to FB_IN (FB = ÷ 8 and $f_{REF}$ = 50 MHz) | | −250 | | +100 | ps | PLL locked |
| $t_{SK(O)}$ | Output-to-Output Skew[6] | within QA bank | | | 100 | ps | |
| | | within QB bank | | | 125 | ps | |
| | | within QC bank | | | 100 | ps | |
| | | any output | | | 175 | ps | |
| DC | Output Duty Cycle | | 47 | 50 | 53 | % | |
| $t_R$, $t_F$ | Output Rise/Fall Time | | 0.1 | | 1.0 | ns | 0.55 to 2.4 V |
| $t_{PLZ, HZ}$ | Output Disable Time | | | | 10 | ns | |
| $t_{PZL}$ | Output Enable Time | | | | 10 | ns | |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter[7] | | | | 90 | ps | |
| $t_{JIT(PER)}$ | Period Jitter[6] | | | | 90 | ps | |

**Table 8. AC Characteristics** ($V_{CC}$ = 3.3 V ± 5%, $T_A$ = 0°C to +70°C)[1] (Continued)

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $t_{JIT(\varnothing)}$ | I/O Phase Jitter RMS (1 σ)[8] | FB = ÷ 8 | | | 15 | ps | |
| | | FB = ÷ 12 | | | 49 | ps | |
| | | FB = ÷ 16 | | | 18 | ps | |
| | | FB = ÷ 24 | | | 22 | ps | |
| | | FB = ÷ 32 | | | 26 | ps | |
| | | FB = ÷ 48 | | | 34 | ps | |
| BW | PLL Closed Loop Bandwidth[9] | FB = ÷ 8 | | 0.50 – 1.80 | | MHz | |
| | | FB = ÷ 12 | | 0.30 – 1.00 | | MHz | |
| | | FB = ÷ 16 | | 0.25 – 0.70 | | MHZ | |
| | | FB = ÷ 24 | | 0.17 – 0.40 | | MHz | |
| | | FB = ÷ 32 | | 0.12 – 0.30 | | MHz | |
| | | FB = ÷ 48 | | 0.07 – 0.20 | | MHz | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | | 10 | ms | |

1. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT}$.
2. In bypass mode, the MPC9774 divides the input reference clock.
3. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio (FB): $f_{REF} = f_{VCO} \div (M \cdot VCO\_SEL)$.
4. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$. E.g. at $f_{REF}$ = 62.5 MHz the input duty cycle range is 12.5% < DC < 87.5%.
5. Static phase offset depends on the reference frequency: $t_{(\varnothing)} = +50$ ps ± $(1 \div (120 \cdot f_{REF}))$ for any reference frequency.
6. Refer to Application section for part-to-part skew calculation.
7. Valid for all outputs at the same frequency.
8. I/O jitter for $f_{VCO}$ = 400 MHz. Refer to Applications Information for I/O jitter at other frequencies and for a jitter calculation for confidence factors other than 1 σ.
9. –3 dB point of PLL transfer characteristics.

# APPLICATIONS INFORMATION

### MPC9774 Configurations

Configuring the MPC9774 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$
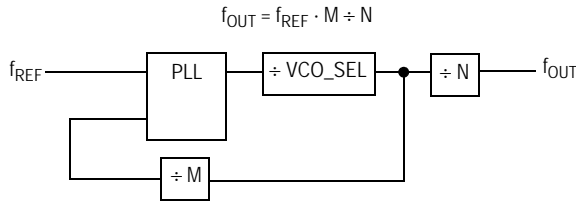


where $f_{REF}$ is the reference frequency of the selected input clock source (CCLK0 or CCLK1), M is the PLL feedback divider and N is a output divider. M is configured by the FSEL_FB[0:1] and N is individually configured for each output bank by the FSEL_A, FSEL_B and FSEL_C inputs.

The reference frequency $f_{REF}$ and the selection of the feedback-divider M is limited by the specified VCO frequency range. $f_{REF}$ and M must be configured to match the VCO frequency range of 200 to 500 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \le (f_{REF} \cdot VCO\_SEL \cdot M) \le f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-two or a divide-by-four and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio. The output frequency for each bank can be derived from the VCO frequency and output divider:

$$f_{QA[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[3:0]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

### Table 9. MPC9774 Divider

| Divider | Function | VCO_SEL | Values |
|---------|----------|---------|--------|
| M | PLL Feedback FSEL_FB[0:1] | $\div 2$ | 8, 12, 16, 24 |
| | | $\div 4$ | 16, 24, 32, 48 |
| $N_A$ | Bank A Output Divider FSEL_A | $\div 2$ | 4, 8 |
| | | $\div 4$ | 8, 16 |
| $N_B$ | Bank B Output Divider FSEL_B | $\div 2$ | 4, 8 |
| | | $\div 4$ | 8, 16 |
| $N_C$ | Bank C Output Divider FSEL_C | $\div 2$ | 8, 12 |
| | | $\div 4$ | 16, 24 |

Table 9 shows the various PLL feedback and output dividers. The output dividers for the three output banks allow the user to configure the outputs into 1:1, 2:1, 3:2, and 3:2:1 frequency ratios. Figure 3 and Figure 4 display example configurations for the MPC9774.
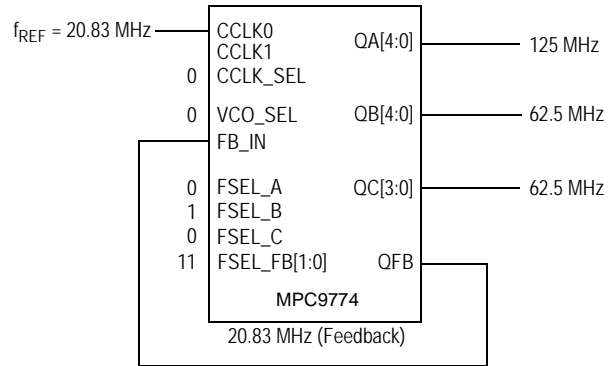


MPC9774 example configuration (feedback of QFB = 20.83 MHz, VCO_SEL = $\div$ 2, M = 12, $N_A$ = 2, $N_B$ = 4, $N_C$ = 4, $f_{VCO}$ = 500 MHz).

| Frequency Range | Min | Max |
|-----------------|-----|-----|
| Input | 8.33 MHz | 20.83 MHz |
| QA outputs | 50 MHz | 125 MHz |
| QB outputs | 25 MHz | 62.5 MHz |
| QC outputs | 25 MHz | 62.5 MHz |

**Figure 3. Example Configuration**
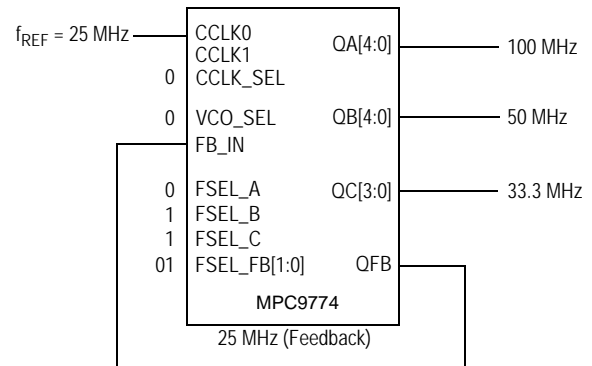


MPC9774 example configuration (feedback of QFB = 25 MHz, VCO_SEL = $\div$ 2, M = 8, $N_A$ = 2, $N_B$ = 4, $N_C$ = 6, $f_{VCO}$ = 400 MHz).

| Frequency Range | Min | Max |
|-----------------|-----|-----|
| Input | 20 MHz | 48 MHz |
| QA outputs | 50 MHz | 120 MHz |
| QB outputs | 50 MHz | 120 MHz |
| QC outputs | 100 MHz | 200 MHz |

**Figure 4. Example Configuration**

### Using the MPC9774 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9774. Designs using the MPC9774 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback of the MPC9774 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

### Calculation of Part-to-Part Skew

The MPC9774 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9774 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:
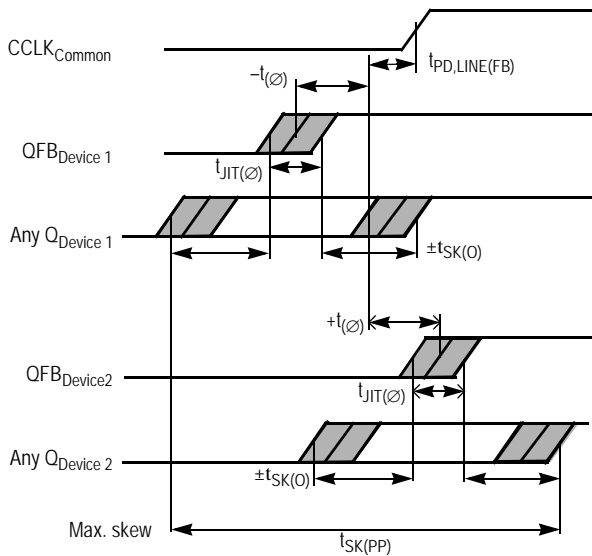
**Figure 5. MPC9774 Maximum Device-to-Device Skew**

Due to the statistical nature of I/O jitter a RMS value (1 $\sigma$) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.
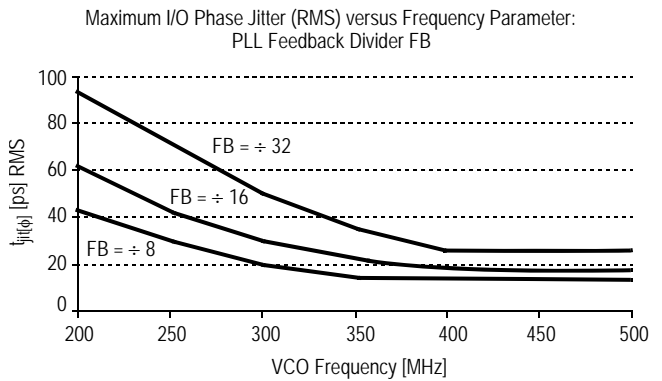
**Table 10. Confidence Factor CF**

| CF | Probability of Clock Edge within the Distribution |
|---|---|
| $\pm 1\sigma$ | 0.68268948 |
| $\pm 2\sigma$ | 0.95449988 |
| $\pm 3\sigma$ | 0.99730007 |
| $\pm 4\sigma$ | 0.99993663 |
| $\pm 5\sigma$ | 0.99999943 |
| $\pm 6\sigma$ | 0.99999999 |

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 6 and Figure 7 to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.
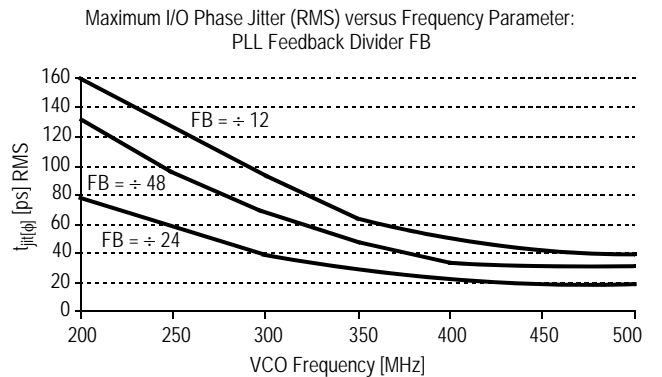
In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of −470 ps to +320 ps relative to CCLK (PLL feedback = ÷ 8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 15 ps RMS max., static phase offset $t_{(\varnothing)}$ = −250 ps to +100 ps):

$$t_{SK(PP)} = [-250 \text{ ps...}+100 \text{ ps}] + [-175 \text{ ps...}175 \text{ ps}] +$$
$$[(15 \text{ ps} \bullet -3)...(15 \text{ ps} \bullet 3)] + t_{PD, LINE(FB)}$$
$$t_{SK(PP)} = [-470 \text{ ps...}+320 \text{ ps}] + t_{PD, LINE(FB)}$$

Maximum I/O Phase Jitter (RMS) versus Frequency Parameter: PLL Feedback Divider FB

**Figure 6. MPC9774 I/O Jitter**

Maximum I/O Phase Jitter (RMS) versus Frequency Parameter: PLL Feedback Divider FB

**Figure 7. MPC9774 I/O Jitter**

**Driving Transmission Lines**

The MPC9774 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale Semiconductor application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9774 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9774 clock driver is effectively doubled due to its capability to drive multiple lines.
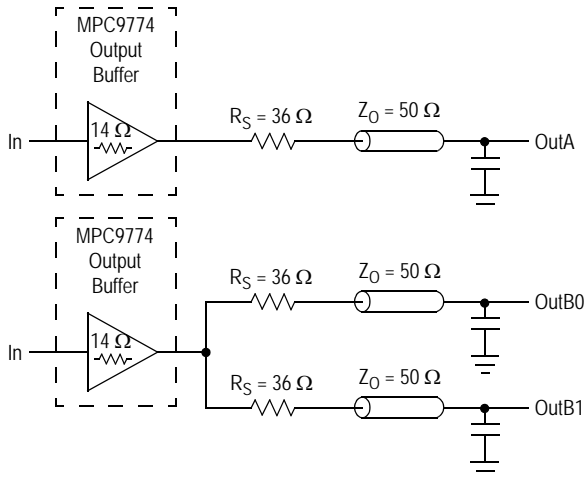


**Figure 8. Single versus Dual Transmission Lines**

The waveform plots in Figure 9 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9774 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9774. The output waveform in Figure 9 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
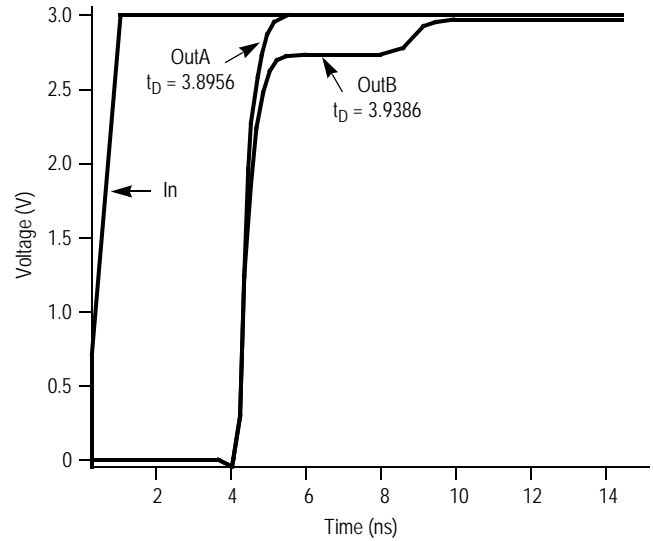$$Z_0 = 50 \ \Omega \ || \ 50 \ \Omega$$
$$R_S = 36 \ \Omega \ || \ 36 \ \Omega$$
$$R_0 = 14 \ \Omega$$
$$V_L = 3.0 (25 \div (18 + 17 + 25)$$
$$= 1.31 \ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).



**Figure 9. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$14 \ \Omega + 22 \ \Omega \ || \ 22 \ \Omega = 50 \ \Omega \ || \ 50 \ \Omega$$
$$25 \ \Omega = 25 \ \Omega$$
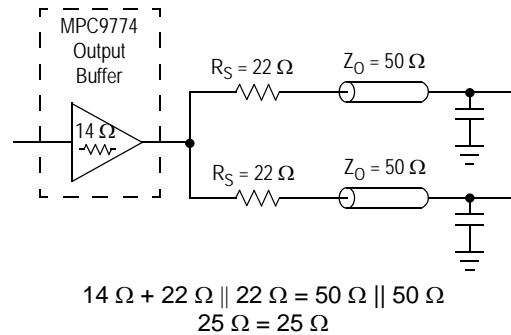
**Figure 10. Optimized Dual Line Termination**

## Power Supply Filtering

The MPC9774 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CC\_PLL}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9774 provides separate power supplies for the output buffers ($V_{CC}$) and the phase-locked loop ($V_{CC\_PLL}$) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the $V_{CC\_PLL}$ pin for the MPC9774. Figure 11 illustrates a typical power supply filter scheme. The MPC9774 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor $R_F$. From the data sheet the $I_{CC\_PLL}$ current (the current sourced through the $V_{CC\_PLL}$ pin) is typically 5 mA (7.5 mA maximum), assuming that a minimum of 3.02 V ($V_{CC\_PLL}$, min) must be maintained on the $V_{CC\_PLL}$ pin. The resistor $R_F$ shown in Figure 11 must have a resistance of 5–15 $\Omega$ to meet the voltage drop criteria.

The minimum values for RF and the filter capacitor $C_F$ are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example, RC

filter shown in Figure 11, the filter cut-off frequency is around 3–5 kHz and the noise attenuation at 100 kHz is better than 42 dB.
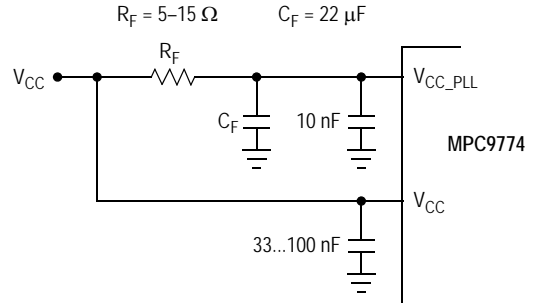


**Figure 11. $V_{CC\_PLL}$ Power Supply Filter**

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9774 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.
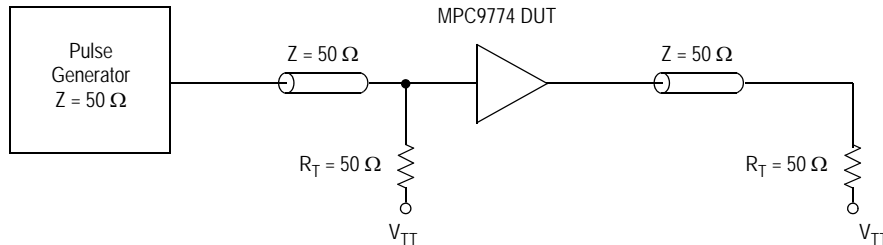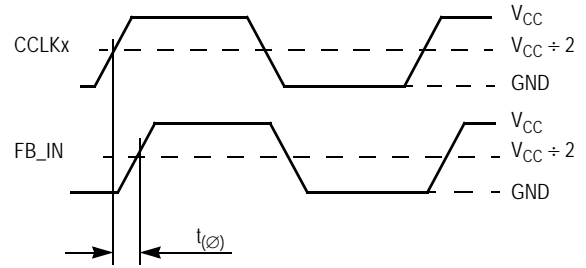


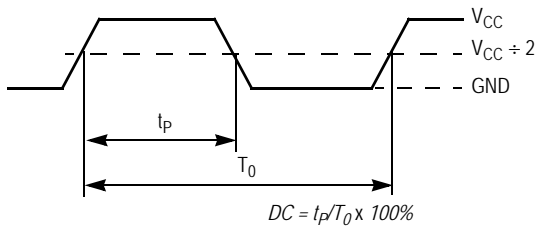**Figure 12. CCLK MPC9774 AC Test Reference**
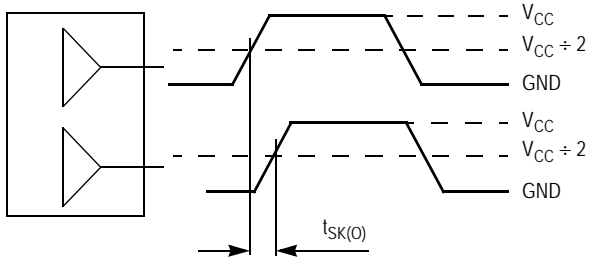
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

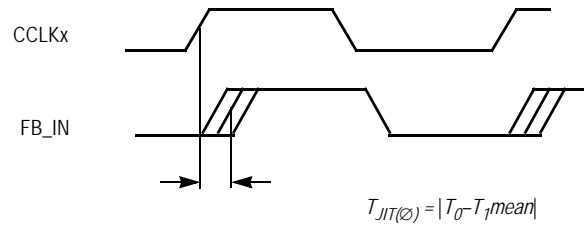**Figure 13. Output-to-Output Skew t$_{SK(O)}$**



**Figure 14. Propagation Delay (t$_{(\varnothing)}$, Static Phase Offset) Test Reference**
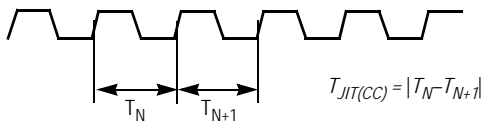


$$DC = t_P/T_0 \times 100\%$$

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage
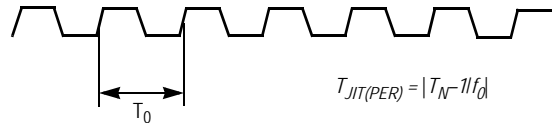
**Figure 15. Output Duty Cycle (DC)**



$$T_{JIT(\varnothing)} = |T_0 - T_1 mean|$$

The deviation in t$_0$ for a controlled edge with respect to a t$_0$ mean in a random sample of cycles

**Figure 16. I/O Jitter**



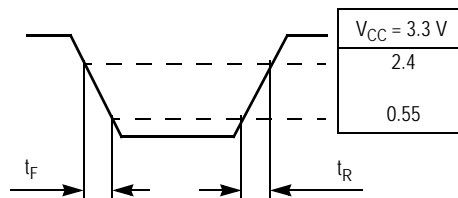$$T_{JIT(CC)} = |T_N - T_{N+1}|$$

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs
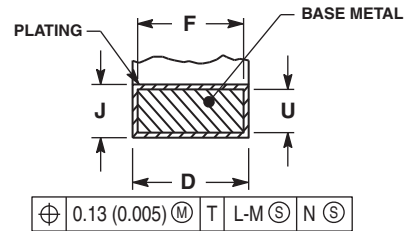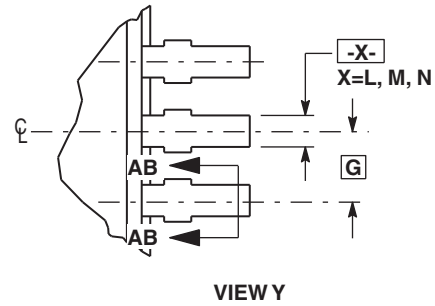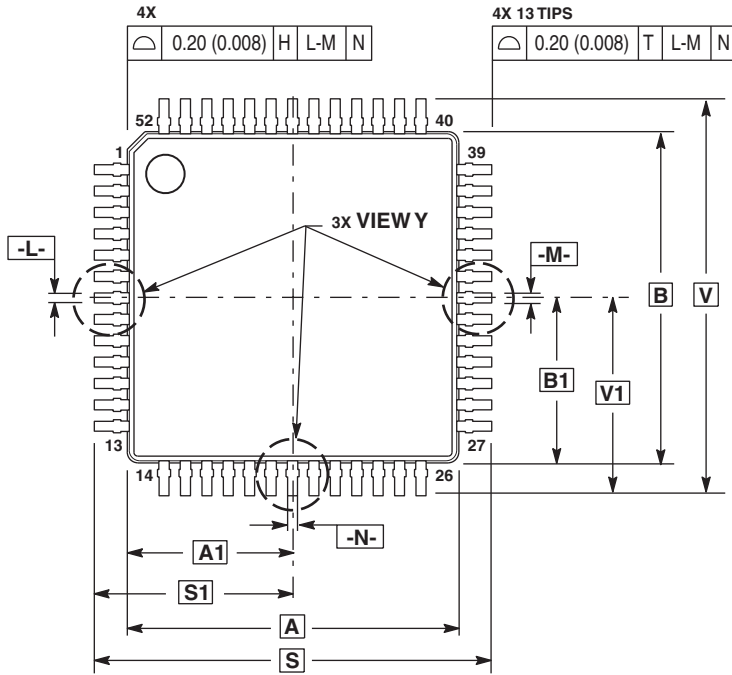
**Figure 17. Cycle-to-Cycle Jitter**



$$T_{JIT(PER)} = |T_N - 1/f_0|$$

The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

**Figure 18. Period Jitter**



| V$_{CC}$ = 3.3 V |
| --- |
| 2.4 |
| 0.55 |

**Figure 19. Output Transition Time Test Reference**

## PACKAGE DIMENSIONS



4X
☐ 0.20 (0.008) H L-M N

4X 13 TIPS
☐ 0.20 (0.008) T L-M N

3X **VIEW Y**

-L-   -M-   -N-

B   V   B1   V1

52   40   39   1   13   27   14   26

A1   S1   A   S

**VIEW AA**

4X θ2
4X θ3
☐ 0.10 (0.004) T

-C-   -H-   -T-   SEATING PLANE

— 0.05 (0.002) ⑤

W   2X R R1   θ1   θ
0.25 (0.010)   GAGE PLANE
C2   C1   K   E   Z

**VIEW AA**

-X-
X=L, M, N

C̵   AB   AB   G

**VIEW Y**

PLATING   F   BASE METAL
J   U   D

⊕ 0.13 (0.005) Ⓜ T L-M Ⓢ N Ⓢ

**SECTION AB-AB**
ROTATED 90˚ CLOCKWISE

NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSTION 0.07 (0.003).
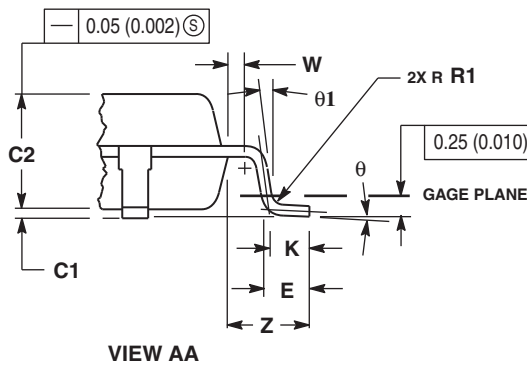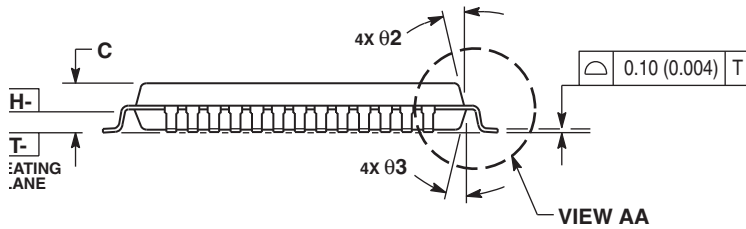
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 10.00 BSC | | 0.394 BSC | |
| A1 | 5.00 BSC | | 0.197 BSC | |
| B | 10.00 BSC | | 0.394 BSC | |
| B1 | 5.00 BSC | | 0.197 BSC | |
| C | --- | 1.70 | --- | 0.067 |
| C1 | 0.05 | 0.20 | 0.002 | 0.008 |
| C2 | 1.30 | 1.50 | 0.051 | 0.059 |
| D | 0.20 | 0.40 | 0.008 | 0.016 |
| E | 0.45 | 0.75 | 0.018 | 0.030 |
| F | 0.22 | 0.35 | 0.009 | 0.014 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.07 | 0.20 | 0.003 | 0.008 |
| K | 0.50 REF | | 0.020 REF | |
| R1 | 0.08 | 0.20 | 0.003 | 0.008 |
| S | 12.00 BSC | | 0.472 BSC | |
| S1 | 6.00 BSC | | 0.236 BSC | |
| U | 0.09 | 0.16 | 0.004 | 0.006 |
| V | 12.00 BSC | | 0.472 BSC | |
| V1 | 6.00 BSC | | 0.236 BSC | |
| W | 0.20 REF | | 0.008 REF | |
| Z | 1.00 REF | | 0.039 REF | |
| θ | 0˚ | 7˚ | 0˚ | 7˚ |
| θ1 | 0˚ | --- | 0˚ | --- |
| θ2 | 12˚ REF | | 12˚ REF | |
| θ3 | 12˚ REF | | 12˚ REF | |

**CASE 848D-03**
**ISSUE D**
**52-LEAD LQFP PACKAGE**

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| 5 | | 1 | NRND – Not Recommend for New Designs | 1/8/13 |
| 5 | | 1 | Removed NRND and removed bullet referencing the replacement part. | 5/5/15 |
| 5 | | 1 | Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02 | 3/16/16 |

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