The MPC9653A is a 3.3 V compatible, 1:8 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 125 MHz and output skews less than 150 ps the device meets the needs of the most demanding clock applications.

MPC9653A

LOW VOLTAGE
3.3 V LVCMOS 1:8
PLL CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

Features

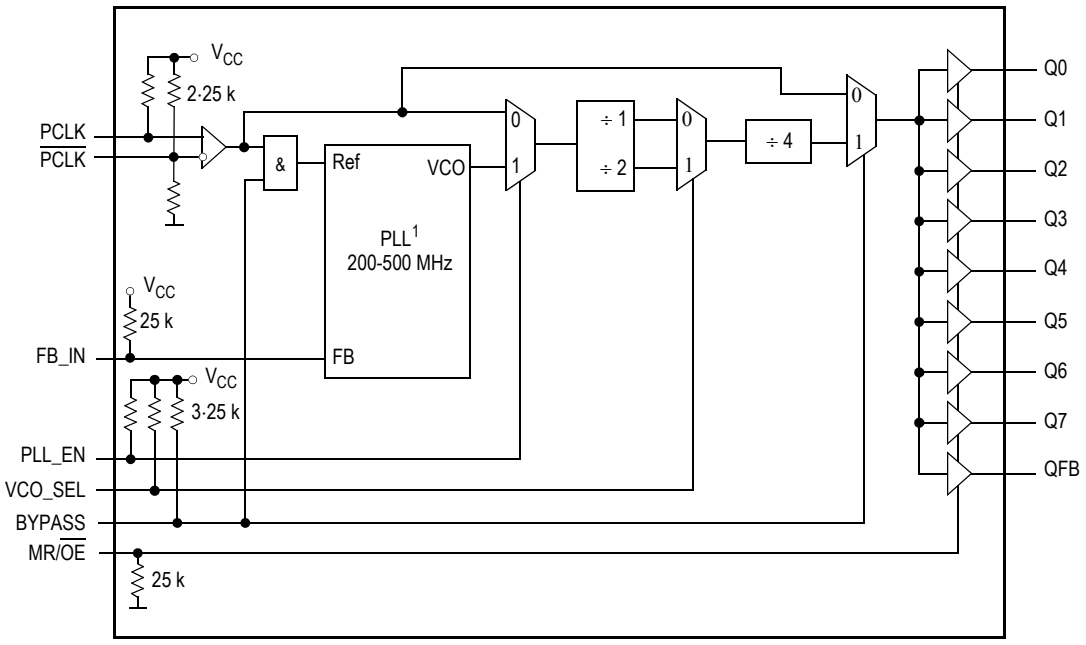
- 1:8 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3 V power supply
- Generates clock signals up to 125 MHz
- PLL guaranteed to lock down to 145 MHz, output frequency = 36.25 MHz
- Maximum output skew of 150 ps
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 16 clock lines
- 32-lead LQFP packaging
- 32-lead Pb-free Package Available
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC953 and MPC9653
- **NRND – Not Recommend for New Designs**

The MPC9653A utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9653A requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 25 to 62.5 MHz or 50 to 125 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-4 or divide-by-8) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9653A is running at either 4x or 8x of the reference clock frequency. The MPC9653A is guaranteed to lock in a low power PLL mode in the high frequency range (VCO_SEL = 0) down to PLL = 145 MHz or F_{ref} = 36.25 MHz.

The MPC9653A has a differential LVPECL reference input along with an external feedback input. The device is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and $\overline{\text{BYPASS}}$ controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/OE pin. Asserting MR/OE also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/OE will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9653A is fully 3.3 V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9653A outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm^2 32-lead LQFP package.



Note 1. PLL will lock @ 145 MHz

Figure 1. MPC9653A Logic Diagram

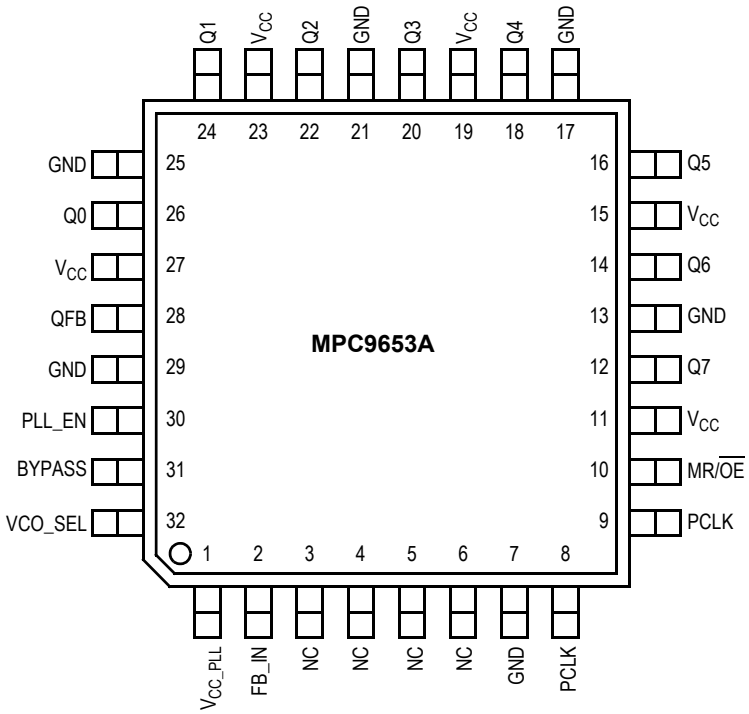


Figure 2. MPC9653A 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	PECL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
VCO_SEL	Input	LVCMOS	Operating frequency range select
$\overline{\text{BYPASS}}$	Input	LVCMOS	PLL and output divider bypass select
PLL_EN	Input	LVCMOS	PLL enable/disable
MR/$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
Q0–7	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	Clock output for PLL feedback, connect to FB_IN
GND	Supply	Ground	Negative power supply (GND)
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Refer to APPLICATIONS INFORMATION for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9653A is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output[1]
$\overline{\text{BYPASS}}$	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9653A is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0–7} = 4 \cdot f_{VCO}$	VCO ÷ 2 (Low output range). $f_{REF} = f_{Q0–7} = 8 \cdot f_{VCO}$
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

1. PLL operation requires $\overline{\text{BYPASS}}$ = 1 and PLL_EN = 1.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	(PCLK)	300			mV	LVPECL
V_{CMR}(1)	Common Mode Range	(PCLK)	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA(2)
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output impedance			14 – 17		Ω	
I_{IN}	Input Current(3)				±200	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current			5.0	10	mA	V_{CC_PLL} Pin
I_{CCQ}(4)	Maximum Quiescent Supply Current				10	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9653A is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines. The MPC9653A meets the V_{OH} and V_{OL} specification of the MPC953 (V_{OH} > V_{CC} -0.6 V at I_{OH} = -20 mA and V_{OL} > 0.6 V at I_{OL} = 20 mA).
3. Inputs have pull-down or pull-up resistors affecting the input current.
4. OE/$\overline{MR}$ = 1 (outputs in high-impedance state).

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency PLL Mode, External Feedback Input reference frequency in PLL bypass mode[4]	÷ 4 feedback[2] ÷ 8 feedback[3]	50 25 0		125 62.5 200	MHz MHz MHz	PLL locked PLL locked
f_{VCO}	VCO Operating Frequency Range[5], [6]		200		500	MHz	
$f_{VCOlock}$	VCO Lock Frequency Range[7]		145		500	MHz	
f_{MAX}	Output Frequency	÷ 4 feedback[2] ÷ 8 feedback[3]	50 25		125 62.5	MHz MHz	PLL locked PLL locked
V_{PP}	Peak-to-Peak Input Voltage	PCLK	450		1000	mV	LVPECL
V_{CMR}[8]	Common Mode Range	PCLK	1.2		V_{CC} – 0.75	V	LVPECL
$t_{PW, MIN}$	Input Reference Pulse Width[9]		2			ns	
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[10]	PCLK to FB_IN	–75		125	ps	PLL locked
t_{PD}	Propagation Delay PLL and divider bypass ($\overline{BYPASS}$ = 0), PCLK to Q0–7 PLL disable ($\overline{BYPASS}$ = 1 and PLL_EN = 0), PCLK to Q0–7		 1.2 3.0		 3.3 7.0	 ns ns	
$t_{sk(O)}$	Output-to-Output Skew[11]				150	ps	
$t_{sk(PP)}$	Device-to-Device Skew in PLL and Divider Bypass[12]				1.5	ns	$\overline{BYPASS}$ = 0
DC	Output Duty Cycle		45	50	55	%	PLL locked
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				7.0	ns	
$t_{PZL, LZ}$	Output Enable Time				6.0	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle jitter				100	ps	
$t_{JIT(PER)}$	Period Jitter				100	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[13]	RMS (1σ)			25	ps	
BW	PLL closed loop bandwidth[14] PLL mode, external feedback	÷ 4 feedback[2] ÷ 8 feedback[3]			0.8 – 4 0.5 – 1.3	MHz MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. ÷ 4 PLL feedback (high frequency range) requires VCO_SEL = 0, PLL_EN = 1, $\overline{BYPASS}$ = 1 and MR/$\overline{OE}$ = 0.
3. ÷ 8 PLL feedback (low frequency range) requires VCO_SEL = 1, PLL_EN = 1, $\overline{BYPASS}$ = 1 and MR/$\overline{OE}$ = 0.
4. In bypass mode, the MPC9653A divides the input reference clock.
5. The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.
6. f_{VCO} is frequency range where AC parameters are guaranteed.
7. $f_{VCOlock}$ is frequency range that the PLL guaranteed to lock, AC parameters only guaranteed over f_{VCO}.
8. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
9. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$. For example, at f_{REF} = 100 MHz the input duty cycle range is 20% < DC < 80%.
10. Valid for f_{REF} = 50 MHz and FB = ÷ 8 (VCO_SEL = 1). For other reference frequencies: $t_{(\varnothing)}$ [ps] = 50 ps ± (1 ÷ (120 · f_{REF})).
11. Refer to the Application Information section for part-to-part skew calculation in PLL zero-delay mode.
12. For a specified temperature and voltage, includes output skew.
13. I/O phase jitter is reference frequency dependent. Refer to APPLICATIONS INFORMATION section for details.
14. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9653A

The MPC9653A supports output clock frequencies from 25 to 125 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 500 MHz for stable and optimal operation. Two operating frequency ranges are supported: 25 to 62.5 MHz and 50 to 125 MHz. Table 7 illustrates the configurations supported by the MPC9653A. PLL zero-delay is supported if $\overline{\text{BYPASS}}$ = 1, PLL_EN = 1 and the input frequency is within the specified PLL reference frequency range.

Table 7. MPC9653A Configurations (QFB connected to FB_IN)

$\overline{\text{BYPASS}}$	PLL_EN	VCO_SEL	Operation	Frequency		
				Ratio	Output Range (f_{Q0-7})	VCO
0	X	X	Test mode: PLL and divider bypass	$f_{Q0-7} = f_{REF}$	0 – 200 MHz	n/a
1	0	0	Test mode: PLL bypass	$f_{Q0-7} = f_{REF} \div 4$	0 – 50 MHz	n/a
1	0	1	Test mode: PLL bypass	$f_{Q0-7} = f_{REF} \div 8$	0 – 25 MHz	n/a
1	1	0	PLL mode (high frequency range)	$f_{Q0-7} = f_{REF}$	50 to 125 MHz	$f_{VCO} = f_{REF} \cdot 4$
1	1	1	PLL mode (low frequency range)	$f_{Q0-7} = f_{REF}$	25 to 62.5 MHz	$f_{VCO} = f_{REF} \cdot 8$

Power Supply Filtering

The MPC9653A is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9653A provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9653A. Figure 3 illustrates a typical power supply filter scheme. The MPC9653A frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (10 mA maximum), assuming that a minimum of 2.985 V must be maintained on the V_{CC_PLL} pin.

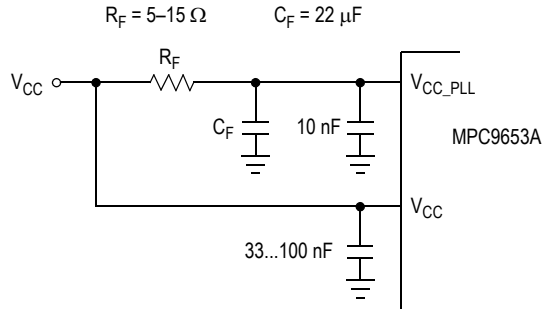


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 4 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9653A has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9653A in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9653A. Designs using the MPC9653A as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9653A clock driver allows for its use as a zero-delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9653A zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9653As are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\,LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

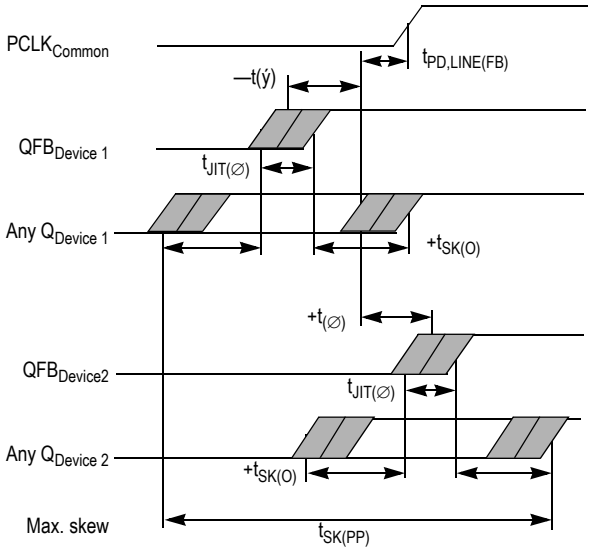


Figure 4. MPC9653A Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –197 ps to 297 ps (at 125 MHz reference frequency) relative to PCLK:

$$t_{SK(PP)} = [-17ps...117ps] + [-150ps...150ps] + [(10ps\ @\ -3)...(10ps\ @\ 3)] + t_{PD,\,LINE(FB)}$$

$$t_{SK(PP)} = [-197ps...297ps] + t_{PD,\,LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5, can be used for a more precise timing performance analysis.

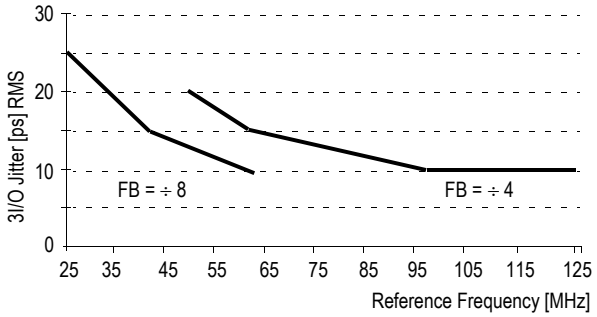


Figure 5. Maximum I/O Jitter versus Frequency

Driving Transmission Lines

The MPC9653A clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale Semiconductor application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9653A clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 5, illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9653A clock driver is effectively doubled due to its capability to drive multiple lines.

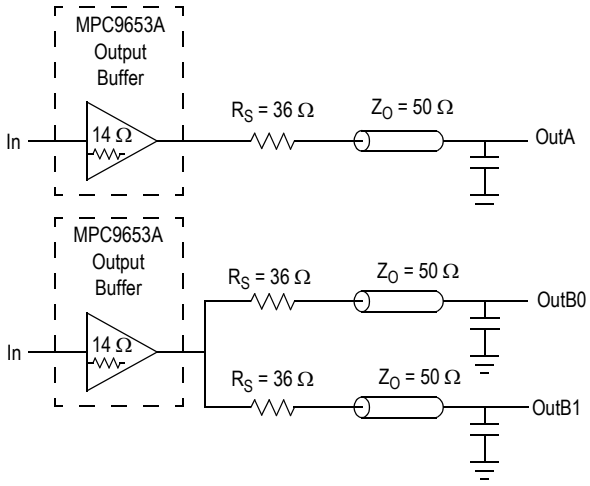


Figure 6. Single versus Dual Transmission Lines

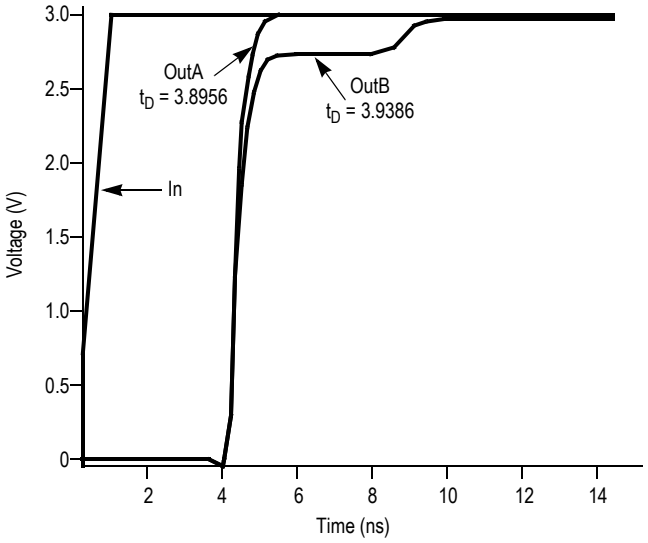


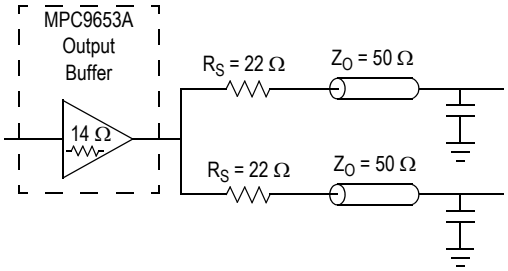
Figure 7. Single versus Dual Waveforms

The waveform plots in Figure 7 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9653A output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9653A. The output waveform in Figure 7 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 14 + 25)$$
$$= 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8, should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$$
$$25\ \Omega = 25\ \Omega$$

Figure 8. Optimized Dual Line Termination

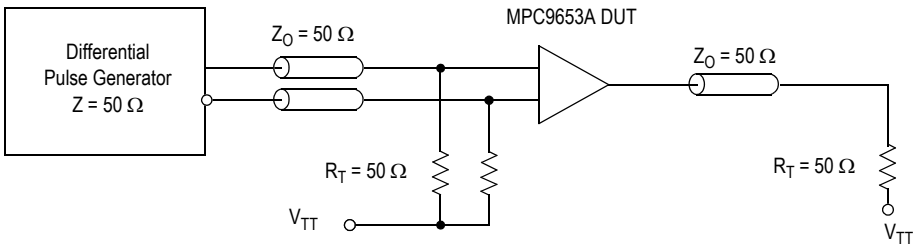
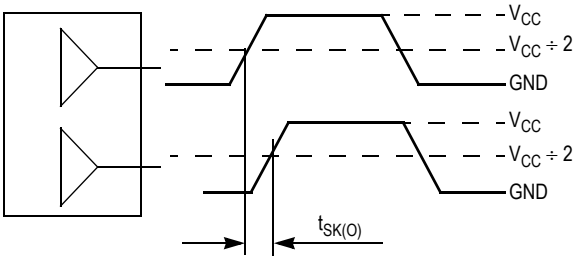


Figure 9. MPC9653A AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-Output Skew $t_{SK(O)}$

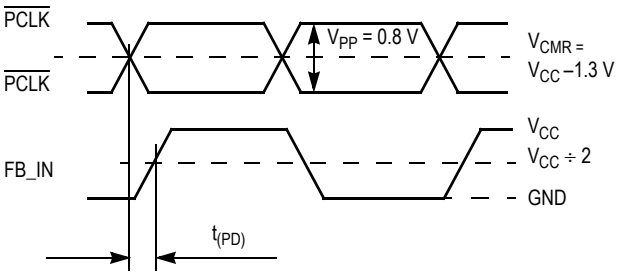
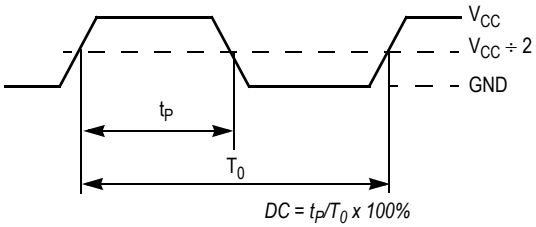
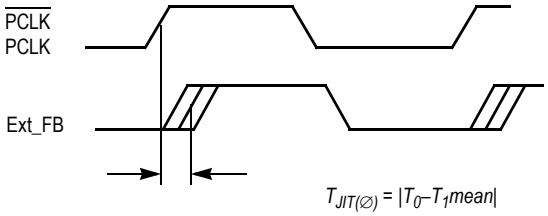


Figure 11. Propagation delay ($t_{(PD)}$, static phase offset) Test Reference



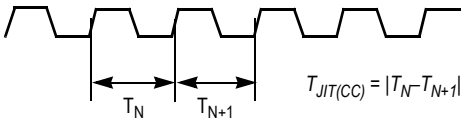
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



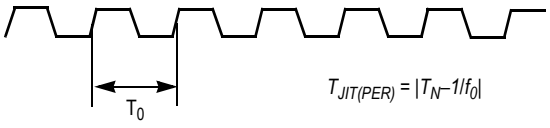
The deviation in t_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

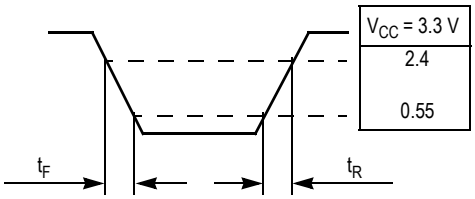
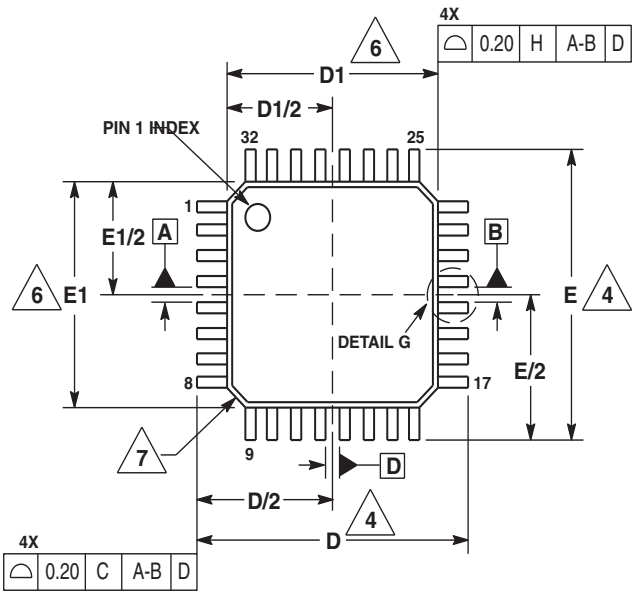
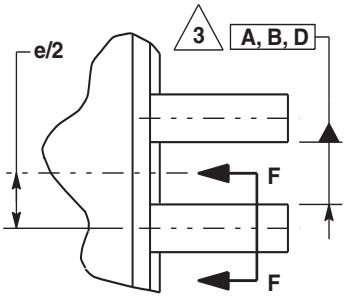


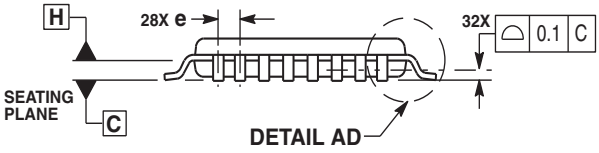
Figure 16. Output Transition Time Test Reference

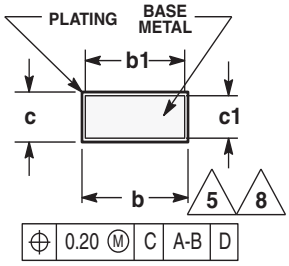
PACKAGE DIMENSIONS



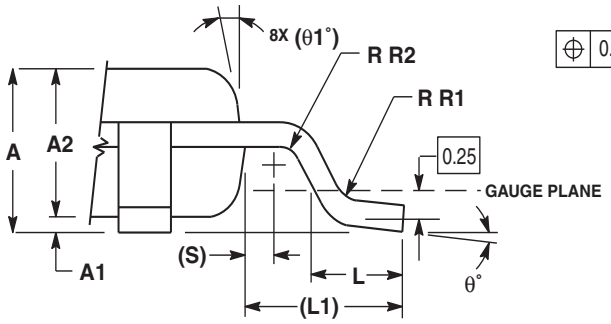


DETAIL G





SECTION F-F



DETAIL AD

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
4		1	NRND – Not Recommend for New Designs	1/8/13

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