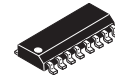


The MPC962308 is a 3.3 V Zero Delay Buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. The MPC962308 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. The input-to-output skew is guaranteed to be less than 250 ps and output-to-output skew is guaranteed to be less than 200 ps.

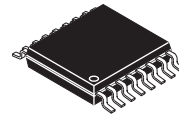
**Features**

- 1:8 outputs LVCMOS zero-delay buffer
- Zero input-output propagation delay, adjustable by the capacitive load on FBK input
- Multiple Configurations, see [Table 2](#)
- Multiple low-skew outputs
- 200 ps max output-output skew
- 700 ps max device-device skew
- Two banks of four outputs, output tristate control by two select inputs
- Supports a clock I/O frequency range of 10 MHz to 133 MHz
- Low jitter, 200 ps max cycle-cycle (-1, -1H, -4, -5H)
- ±250 ps static phase offset (SPO)
- 16-pin SOIC package or 16-pin TSSOP package
- Single 3.3 V supply
- Ambient temperature range: -40°C to +85°C
- Compatible with the CY2308 and CY23S08
- Spread spectrum compatible
- **Not Recommend for New Designs**  
**Use replacement part IDT2308**

**MPC962308**



**D SUFFIX**  
16-LEAD SOIC PACKAGE  
CASE 751B-05



**DT SUFFIX**  
16-LEAD TSSOP PACKAGE  
CASE 948F-01

The MPC962308 has two banks of four outputs each which can be controlled by the select inputs as shown in [Table 1](#). Bank B can be tristated if all of the outputs are not required. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes. The MPC962308 PLL enters a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate and there is less than 50 μA of current draw. The PLL shuts down in two additional cases explained in [Table 1](#).

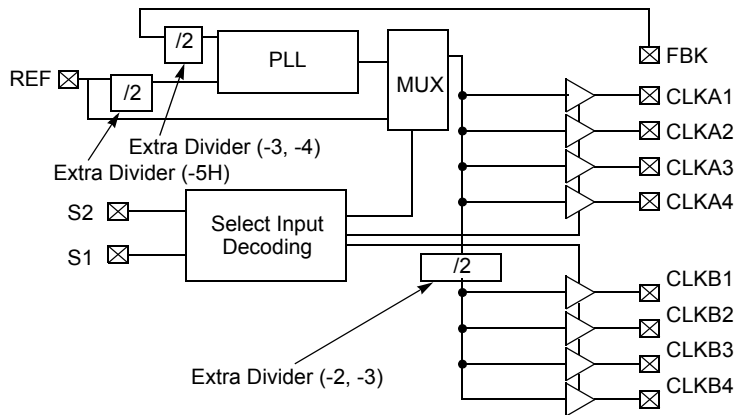
Multiple MPC962308 devices can accept and distribute the same input clock throughout the system. In this situation, the difference between the output skews of two devices will be less than 700 ps.

The MPC962308 is available in five different configurations as shown in [Table 2](#). In the MPC962308-1, the reference frequency is reproduced by the PLL and provided at the outputs. A high drive version of this configuration, the MPC962308-1H, is available to provide faster rise and fall times of the device.

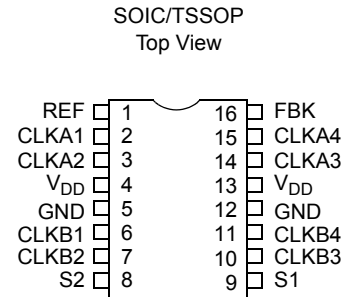
The MPC962308-2 provides 2X and 1X the reference frequency at the output banks. In addition, the MPC962308-3 provides 4X and 2X the reference frequency at the output banks. The output banks driving the feedback will determine the different configurations of the above devices. The MPC962308-4 provides outputs 2X the reference frequency. The MPC962308-5H is a high drive version with outputs of REF/2.

The MPC962308 is fully 3.3 V compatible and requires no external components for the internal PLL. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines on the incident edge. Depending on the configuration, the device is offered in a 16-lead SOIC or 16-lead TSSOP package.

**Block Diagram**



**Pin Configuration**



**Table 1. Select Input Decoding**

| S2 | S1 | CLOCK A1—A4           | CLOCK B1—B4         | Output Source | PLL Shutdown |
|----|----|-----------------------|---------------------|---------------|--------------|
| 0  | 0  | Three-State           | Three-State         | PLL           | Y            |
| 0  | 1  | Driven                | Three-State         | PLL           | N            |
| 1  | 0  | Driven <sup>(1)</sup> | Driven <sup>1</sup> | Reference     | Y            |
| 1  | 1  | Driven                | Driven              | PLL           | N            |

1. Outputs inverted on MPC962308-2 in bypass mode, S2=1 and S1=0.

**Table 2. Available MPC962308 Configurations**

| Device       | Feedback From    | Bank A Frequency | Bank B Frequency                        |
|--------------|------------------|------------------|---|
| MPC962308-1  | Bank A or Bank B | Reference        | Reference                               |
| MPC962308-1H | Bank A or Bank B | Reference        | Reference                               |
| MPC962308-2  | Bank A           | Reference        | Reference/2                             |
| MPC962308-2  | Bank B           | 2 X Reference    | Reference                               |
| MPC962308-3  | Bank A           | 2 X Reference    | Reference or Reference <sup>[(1)]</sup> |
| MPC962308-3  | Bank B           | 4 X Reference    | 2 X Reference                           |
| MPC962308-4  | Bank A or Bank B | 2 X Reference    | 2 X Reference                           |
| MPC962308-5H | Bank A or Bank B | Reference /2     | Reference /2                            |

1. Output phase is indeterminate (0° or 180° from input clock). If phase integrity is required, use the MPC962308-2.

**Table 3. Pin Description**

| Pin | Signal               | Description                                   |
|-----|----------------------|---|
| 1   | REF <sup>(1)</sup>   | Input reference frequency, 5 V tolerant input |
| 2   | CLKA1 <sup>(2)</sup> | Clock output, Bank A                          |
| 3   | CLKA2 <sup>(2)</sup> | Clock output, Bank A                          |
| 4   | V <sub>DD</sub>      | 3.3 V supply                                  |
| 5   | GND                  | Ground  |
| 6   | CLKB1 <sup>(2)</sup> | Clock output, Bank B                          |
| 7   | CLKB2 <sup>(2)</sup> | Clock output, Bank B                          |
| 8   | S2 <sup>(3)</sup>    | Select input, bit 2                           |
| 9   | S1 <sup>(3)</sup>    | Select input, bit 1                           |
| 10  | CLKB3 <sup>(2)</sup> | Clock output, Bank B                          |
| 11  | CLKB4 <sup>(2)</sup> | Clock output, Bank B                          |
| 12  | GND                  | Ground  |
| 13  | V <sub>DD</sub>      | 3.3 V supply                                  |
| 14  | CLKA3 <sup>(2)</sup> | Clock output, Bank A                          |
| 15  | CLKA4 <sup>(2)</sup> | Clock output, Bank A                          |
| 16  | FBK                  | PLL feedback input                            |

1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.

**Table 4. Maximum Ratings**

| Characteristics   | Value                        | Unit |
|---|------------------------------|------|
| Supply Voltage to Ground Potential                      | -0.5 to +3.9                 | V    |
| DC Input Voltage (Except REF)                           | -0.5 to V <sub>DD</sub> +0.5 | V    |
| DC Input Voltage REF                                    | -0.5 to 5.5                  | V    |
| Storage Temperature                                     | -65 to +150                  | °C   |
| Junction  | 150                          | °C   |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | >2000                        | V    |

**Table 5. Operating Conditions for MPC962308-X Industrial Temperature Devices**

| Parameter       | Description                                 | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| V <sub>DD</sub> | Supply Voltage                              | 3.0 | 3.6 | V    |
| T <sub>A</sub>  | Operating Temperature (Ambient Temperature) | -40 | 85  | °C   |
| C <sub>L</sub>  | Load Capacitance, below 100 MHz             |     | 30  | pF   |
|                 | Load Capacitance, from 100 MHz to 133 MHz   |     | 15  | pF   |
| C <sub>IN</sub> | Input Capacitance <sup>(1)</sup>            |     | 7   | pF   |

1. Applies to both REF clock and FBK.

**Table 6. Electrical Characteristics for MPC962308-X Industrial Temperature Devices<sup>(1)</sup>**

| Parameter          | Description                        | Test Conditions   | Min | Max          | Unit    |
|--------------------|------------------------------------|---|-----|--------------|---------|
| $V_{IL}$           | Input LOW Voltage                  |   |     | 0.8          | V       |
| $V_{IH}$           | Input HIGH Voltage                 |   | 2.0 |              | V       |
| $I_{IL}$           | Input LOW Current                  | $V_{IN} = 0V$   |     | 50.0         | $\mu A$ |
| $I_{IH}$           | Input HIGH Current                 | $V_{IN} = V_{DD}$   |     | 100.0        | $\mu A$ |
| $V_{OL}$           | Output LOW Voltage <sup>(2)</sup>  | $I_{OL} = 8\text{ mA} (-1, -2, -3, -4)$<br>$I_{OL} = 12\text{ mA} (-1H, -5H)$   |     | 0.4          | V       |
| $V_{OH}$           | Output HIGH Voltage <sup>(2)</sup> | $I_{OH} = -8\text{ mA} (-1, -2, -3, -4)$<br>$I_{OH} = -12\text{ mA} (-1H, -5H)$ | 2.4 |              | V       |
| $I_{DD}$ (PD mode) | Power Down Supply Current          | REF = 0 MHz   |     | 25.0         | $\mu A$ |
| $I_{DD}$           | Supply Current                     | Unloaded outputs, 100 MHz,<br>Select inputs at $V_{DD}$ or GND                  |     | 45.0         | mA      |
|                    |                                    |   |     | 70(-1H, -5H) | mA      |
|                    |                                    | Unloaded outputs, 66-MHz REF<br>(-1, -2, -3, -4)                                |     | 35.0         | mA      |
|                    |                                    | Unloaded outputs, 35-MHz REF<br>(-1, -2, -3, -4)                                |     | 20.0         | mA      |

1. All parameters are specified with loaded outputs.

2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

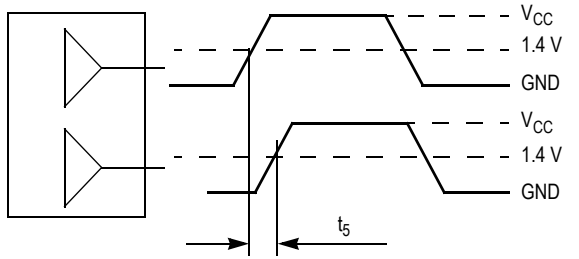
**Table 7. Switching Characteristics for MPC962308-X Industrial Temperature Devices<sup>(1)</sup>**

| Parameter         | Name  | Test Conditions   | Min  | Typ | Max   | Unit |
|-------------------|---|---|------|-----|-------|------|
| t <sub>1</sub>    | Output Frequency  | 30-pF load, All devices   | 10   |     | 100   | MHz  |
| t <sub>1</sub>    | Output Frequency <sup>(2)</sup>   | 20-pF load, -1H, -5H devices  | 10   |     | 133.3 | MHz  |
| t <sub>1</sub>    | Output Frequency <sup>(2)</sup>   | 15-pF load, -1, -2, -3, -4 devices  | 10   |     | 133.3 | MHz  |
|                   | Duty Cycle <sup>(2)</sup> = t <sub>2</sub> ÷ t <sub>1</sub><br>(-1, -2, -3, -4, -1H, -5H) | Measured at 1.4 V, FOUT =66.66 MHz<br>30-pF load                              | 40.0 |     | 60.0  | %    |
|                   | Duty Cycle <sup>(2)</sup> = t <sub>2</sub> ÷ t <sub>1</sub><br>(-1, -2, -3, -4, -1H, -5H) | Measured at 1.4 V, FOUT <50.0 MHz<br>15-pF load                               | 45.0 |     | 55.0  | %    |
| t <sub>3</sub>    | Rise Time <sup>(2)</sup><br>(-1, -2, -3, -4)  | Measured between 0.8 V and 2.0 V,<br>30-pF load                               |      |     | 2.50  | ns   |
|                   | Rise Time <sup>(2)</sup><br>(-1, -2, -3, -4)  | Measured between 0.8 V and 2.0 V,<br>15-pF load                               |      |     | 1.50  | ns   |
|                   | Rise Time <sup>(2)</sup><br>(-1H, -5H)  | Measured between 0.8 V and 2.0 V,<br>30-pF load                               |      |     | 1.50  | ns   |
| t <sub>4</sub>    | Fall Time <sup>(2)</sup><br>(-1, -2, -3, -4)  | Measured between 0.8 V and 2.0 V,<br>30-pF load                               |      |     | 2.50  | ns   |
|                   | Fall Time <sup>(2)</sup><br>(-1, -2, -3, -4)  | Measured between 0.8 V and 2.0 V,<br>15-pF load                               |      |     | 1.50  | ns   |
|                   | Fall Time <sup>(2)</sup><br>(-1H, -5H)  | Measured between 0.8 V and 2.0 V,<br>30-pF load                               |      |     | 1.25  | ns   |
|                   | Output-to-Output Skew on<br>same Bank (-1, -2, -3, -4) <sup>(2)</sup>                     | All outputs equally loaded  |      |     | 200   | ps   |
| t <sub>5</sub>    | Output-to-Output Skew<br>(-1H, -5H)   | All outputs equally loaded  |      |     | 200   | ps   |
|                   | Output Bank A to Output<br>Bank B Skew (-1, -4, -5H)                                      | All outputs equally loaded  |      |     | 200   | ps   |
|                   | Output Bank A to Output<br>Bank B Skew (-2, -3)   | All outputs equally loaded  |      |     | 400   | ps   |
| t <sub>6</sub>    | Delay, REF Rising Edge to<br>FBK Rising Edge <sup>(2)</sup>                               | Measured at V <sub>DD</sub> /2  |      | 0   | ±250  | ps   |
| t <sub>7</sub>    | Device-to-Device Skew <sup>(2)</sup>  | Measured at V <sub>DD</sub> /2 on the FBK pins of<br>devices                  |      | 0   | 700   | ps   |
| t <sub>8</sub>    | Output Slew Rate <sup>(2)</sup>   | Measured between 0.8 V and 2.0 V on -1H,<br>-5H device using Test Circuit # 2 | 1    |     |       | V/ns |
| t <sub>J</sub>    | Cycle-to-Cycle Jitter<br>(-1, -1H, -4, -5H) <sup>(2)</sup>                                | Measured at 66.67 MHz, loaded outputs,<br>15-pF load                          |      |     | 200   | ps   |
|                   |   | Measured at 66.67 MHz, loaded outputs,<br>30-pF load                          |      |     | 200   | ps   |
|                   |   | Measured at 133.3 MHz, loaded outputs,<br>15 pF load                          |      |     | 100   | ps   |
| t <sub>J</sub>    | Cycle-to-Cycle Jitter<br>(-2, -3) <sup>(2)</sup>  | Measured at 66.67 MHz, loaded outputs<br>30-pF load                           |      |     | 400   | ps   |
|                   |   | Measured at 66.67 MHz, loaded outputs<br>15-pF load                           |      |     | 400   | ps   |
| t <sub>LOCK</sub> | PLL Lock Time <sup>(2)</sup>  | Stable power supply, valid clocks presented<br>on REF and FBK pins            |      |     | 1.0   | ms   |

1. All parameters are specified with loaded outputs.

2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

APPLICATIONS INFORMATION



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-Output Skew  $t_{SK(O)}$

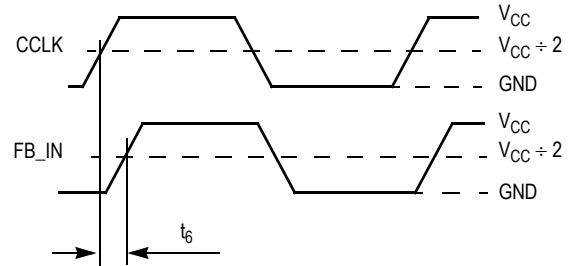
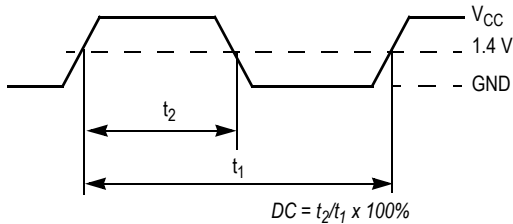


Figure 2. Static Phase Offset Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)

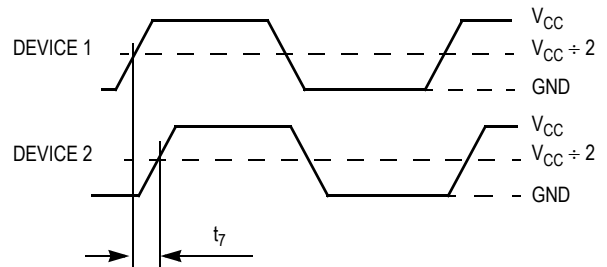
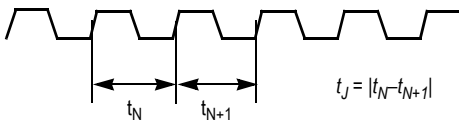


Figure 4. Device-to-Device Skew



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-Cycle Jitter

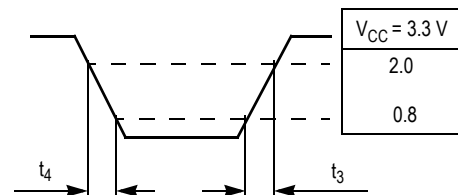
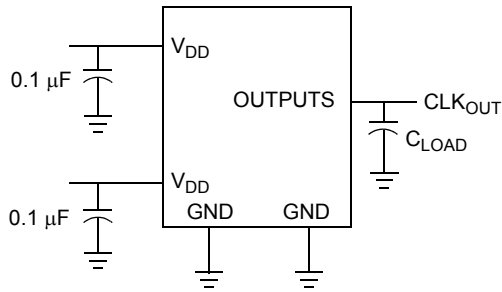


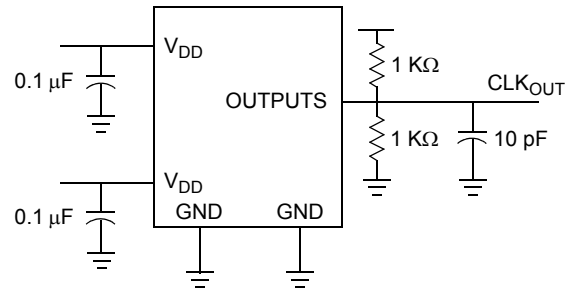
Figure 6. Output Transition Time Test Reference

**Test Circuit #1**



Test Circuit for all parameters except  $t_b$

**Test Circuit #2**

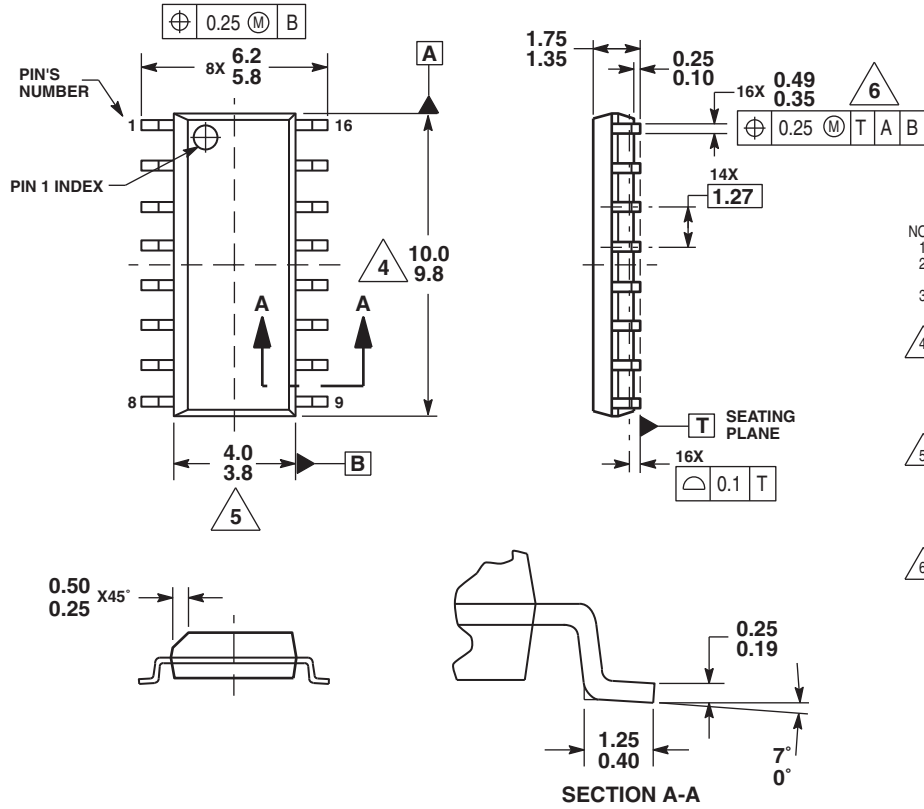


Test Circuit for  $t_b$ , Output slew rate on -1H, -5 device

**Ordering Information (Available)**

| Ordering Code    | Package Name | Package Type                         |
|------------------|--------------|--------------------------------------|
| MPC962308D-1     | D16          | 16-pin 150-mil SOIC                  |
| MPC962308D-1R2   | D16          | 16-pin 150-mil SOIC — Tape and Reel  |
| MPC962308D-1H    | D16          | 16-pin 150-mil SOIC                  |
| MPC962308D-1HR2  | D16          | 16-pin 150-mil SOIC — Tape and Reel  |
| MPC962308DT-1H   | DT16         | 16-pin 150-mil TSSOP                 |
| MPC962308DT-1HR2 | DT16         | 16-pin 150-mil TSSOP — Tape and Reel |
| MPC962308D-2     | D16          | 16-pin 150-mil SOIC                  |
| MPC962308D-2R2   | D16          | 16-pin 150-mil SOIC — Tape and Reel  |

PACKAGE DIMENSIONS

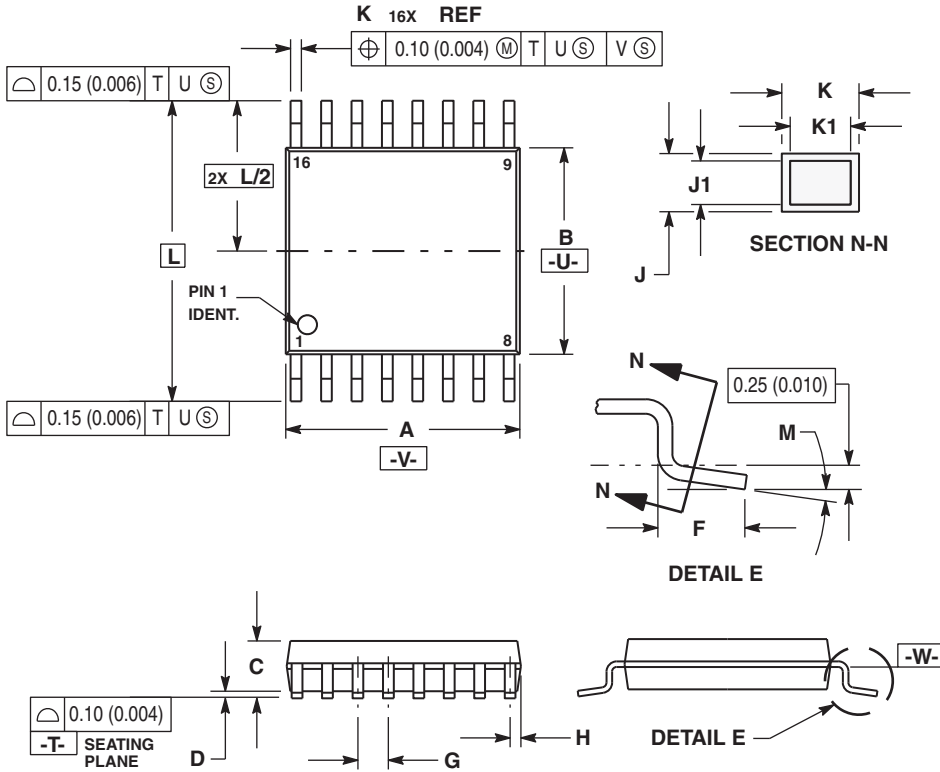


- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62MM.

CASE 751B-05  
 ISSUE K  
 16-LEAD SOIC PLASTIC PACKAGE



PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0'          | 8'   | 0'        | 8'    |

CASE 948F-01  
ISSUE O  
16-LEAD TSSOP PLASTIC PACKAGE

## Revision History Sheet

| Rev | Table | Page | Description of Change                | Date   |
|-----|-------|------|--------------------------------------|--------|
| 4   |       | 1    | NRND – Not Recommend for New Designs | 1/8/13 |
|     |       |      |                                      |        |

NOTES



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(Disclaimer Rev.1.0 Mar 2020)

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