

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVC MOS output capabilities. The device is offered in two versions; the MPC942C has an LVC MOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVC MOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

- LVC MOS/LVTTL Clock Input
- 2.5V LVC MOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Targeted Output-to-Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 V_{CC}
- 32-Lead TQFP Packaging
- Single 3.3V or 2.5V Supply
- **For Functional replacement use 83940DYL**

With a low output impedance ($\approx 12\Omega$), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

The LVC MOS/LVTTL input of the MPC942C provides a more standard LVC MOS interface. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

The MPC942 is a single supply device. The V_{CC} power pins require either 2.5V or 3.3V. The 32-lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

MPC942C

LOW VOLTAGE
1:18 CLOCK
DISTRIBUTION CHIP

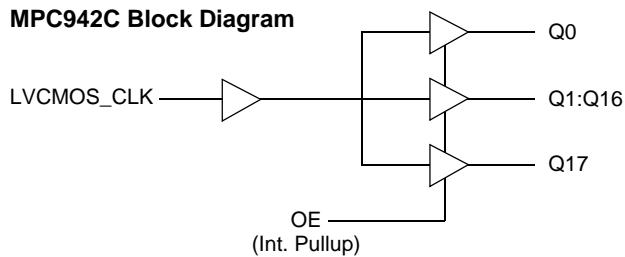


AC SUFFIX
32-LEAD TQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

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LOGIC DIAGRAM

MPC942C Block Diagram



FUNCTION TABLE

OE	Output
0	HIGH IMPEDANCE
1	OUTPUTS ENABLED

Pinout: 32-Lead (Top View)

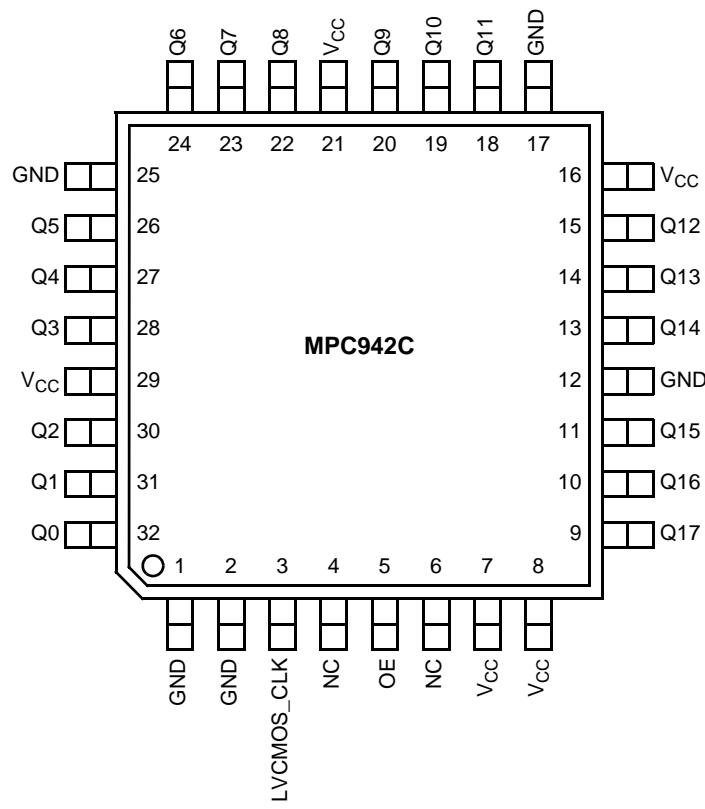


Table 1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.3	3.6	V
V _I	Input Voltage	-0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	-40	125	°C

Table 2. DC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{V} \pm 5\%$, $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CCI}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.0			V	$I_{OH} = -16\text{ mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 16\text{ mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5		mA	

Table 3. AC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{V} \pm 5\%$, $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			200	MHz	
t_{PLH}	Propagation Delay	1.5		2.8	ns	
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.3	ns	Notes 1, 2
$t_{sk(pr)}$	Part-to-Part Skew			600	ps	Notes 1, 3
d_t	Duty Cycle	45		55	%	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	

Table 4. DC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$, $V_{CCO} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{ mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{ mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5		mA	

Table 5. AC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$, $V_{CCO} = 3.3\text{V} \pm 5\%$)

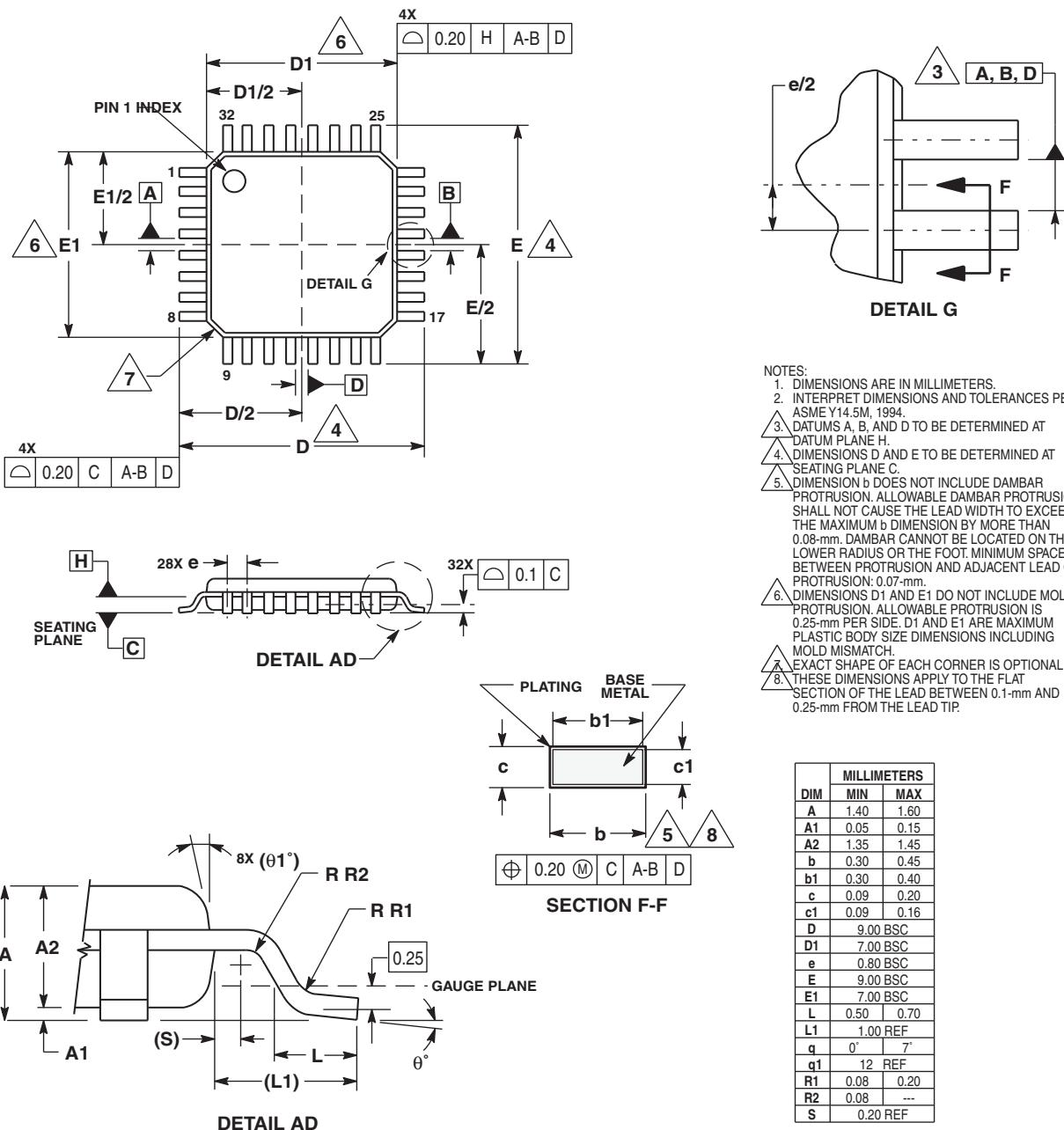
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			250	MHz	
t_{PLH}	Propagation Delay	1.3		2.3	ns	Note 1
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.0	ns	Notes 1, 2
$t_{sk(pr)}$	Part-to-Part Skew			500	ps	Notes 1, 3
d_t	Duty Cycle	45		55	%	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	

1. Tested using standard input levels, production tested @ 133 MHz.

2. Across temperature and voltage ranges, includes output skew.

3. For a specific temperature and voltage, includes output skew.

PACKAGE DIMENSIONS



CASE 873A-03
ISSUE B
LQFP PLASTIC PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
2		1	NRND – Not Recommend for New Designs	1/8/13
2		1	Product Discontinuation Notice - PDN CQ-15-02	5/6/15
3		1	Obsolete per Product Discontinuation Notice - PDN CQ-15-02.	10/4/16

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