

The MPC940L is a 1:18 low voltage clock distribution chip with 2.5 V or 3.3 V LVC MOS output capabilities. The device features the capability to select either a differential LVPECL or an LVC MOS compatible input. The 18 outputs are 2.5 V or 3.3 V LVC MOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 150 ps, the MPC940L is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5 V outputs also make the device ideal for supplying clocks for a high performance microprocessor based design. For a similar device at a lower price/performance point, the reader is referred to the MPC9109.

- LVPECL or LVC MOS Clock Input
- 2.5 V LVC MOS Outputs for Pentium II Microprocessor Support
- 150 ps Maximum Output-to-Output Skew
- Maximum Output Frequency of 250 MHz
- 32-Lead LQFP Packaging, Pb-Free
- Dual or Single Supply Device:
 - Dual V_{CC} Supply Voltage, 3.3 V Core and 2.5 V Output
 - Single 3.3 V V_{CC} Supply Voltage for 3.3 V Outputs
 - Single 2.5 V V_{CC} Supply Voltage for 2.5 V I/O
- For drop in replacement use 83940DYL

With a low output impedance ($\approx 20 \Omega$), in both the HIGH and LOW logic states, the output buffers of the MPC940L are ideal for driving series terminated transmission lines. With a 20Ω output impedance the 940L has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36. If a lower output impedance is desired please see the MPC942 data sheet.

The differential LVPECL inputs of the MPC940L allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVC MOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVC MOS_CLK_SEL pin will select the LVC MOS level clock input. All inputs of the MPC940L have internal pullup/pulldown resistors so they can be left open if unused.

The MPC940L is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3 V core and 3.3 V output, a 3.3 V core and 2.5 V outputs as well as a 2.5 V core and 2.5 V outputs. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7 mm body size with a conservative 0.8 mm pin spacing.

MPC940L

LOW VOLTAGE
1:18 CLOCK
DISTRIBUTION CHIP



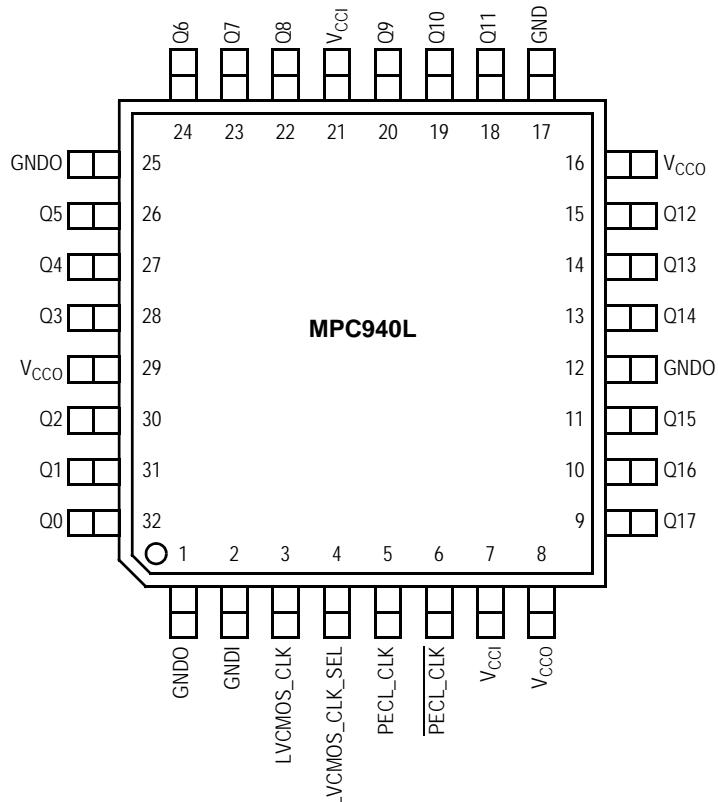
AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04

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LOGIC DIAGRAM



Pinout: 32-Lead LQFP (Top View)



FUNCTION TABLE

| LVCMS_CLK_SEL | Input |
|---------------|-----------|
| 0 | PECL_CLK |
| 1 | LVCMS_CLK |

POWER SUPPLY VOLTAGES

| Supply Pin | Voltage Level |
|------------------|-------------------------|
| V _{CCO} | 2.5 V or 3.3 V \pm 5% |
| V _{COO} | 2.5 V or 3.3 V \pm 5% |

Table 1. Pin Configurations

| Pin | I/O | Type | Function |
|------------------|--------|--------|-----------------------------------|
| PECL_CLK | Input | LVPECL | Reference Clock Input |
| <u>PECL_CLK</u> | | | |
| LVCMS_CLK | Input | LVCMS | Alternative Reference Clock Input |
| LVCMS_CLK_SEL | Input | LVCMS | Selects Clock Source |
| Q0-Q17 | Output | LVCMS | Clock Outputs |
| V _{CCO} | | Supply | Output Positive Power Supply |
| V _{COO} | | Supply | Core Positive Power Supply |
| GND | | Supply | Output Negative Power Supply |
| GNDI | | Supply | Core Negative Power Supply |

Table 2. Absolute Maximum Ratings⁽¹⁾

| Symbol | Parameter | Min | Max | Unit |
|------------|---------------------------|------|----------------|------|
| V_{CC} | Supply Voltage | -0.3 | 3.6 | V |
| V_I | Input Voltage | -0.3 | $V_{DD} + 0.3$ | V |
| I_{IN} | Input Current | | ± 20 | mA |
| T_{Stor} | Storage Temperature Range | -40 | 125 | °C |

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{ V} \pm 5\%$; $V_{CCO} = 3.3\text{ V} \pm 5\%$)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|-----------|-------------------------------------|-----------------|-----|-----------------|---------------|--------------------------|
| V_{IH} | Input HIGH Voltage CMOS_CLK | 2.4 | | V_{CCI} | V | |
| V_{IL} | Input LOW Voltage CMOS_CLK | | | 0.8 | V | |
| V_{PP} | Peak-to-Peak Input Voltage PECL_CLK | 500 | | 1000 | mV | |
| V_{CMR} | Common Mode Range PECL_CLK | $V_{CCI} - 1.4$ | | $V_{CCI} - 0.6$ | V | |
| V_{OH} | Output HIGH Voltage | 2.4 | | | V | $I_{OH} = -20\text{ mA}$ |
| V_{OL} | Output LOW Voltage | | | 0.5 | V | $I_{OL} = 20\text{ mA}$ |
| I_{IN} | Input Current | | | ± 200 | μA | |
| C_{IN} | Input Capacitance | | 4.0 | | pF | |
| C_{pd} | Power Dissipation Capacitance | | 10 | | pF | per output |
| Z_{OUT} | Output Impedance | 18 | 23 | 28 | Ω | |
| I_{CC} | Maximum Quiescent Supply Current | | 0.5 | 1.0 | mA | |

Table 4. AC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{ V} \pm 5\%$; $V_{CCO} = 3.3\text{ V} \pm 5\%$)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|--------------|--|------------|------------|------------|--------|----------------------------------|
| F_{max} | Maximum Input Frequency | | | 250 | MHz | |
| t_{PLH} | Propagation Delay PECL_CLK $\leq 150\text{ MHz}$ CMOS_CLK $\leq 150\text{ MHz}$ | 2.0 1.8 | 2.7 2.5 | 3.4 3.0 | ns | |
| t_{PLH} | Propagation Delay PECL_CLK $> 150\text{ MHz}$ CMOS_CLK $> 150\text{ MHz}$ | 2.0 1.8 | 2.9 2.4 | 3.7 3.2 | ns | |
| $t_{sk(0)}$ | Output-to-Output Skew PECL_CLK CMOS_CLK | | | 150 150 | ps | |
| $t_{sk(pp)}$ | Part-to-Part Skew PECL_CLK $\leq 150\text{ MHz}$ CMOS_CLK $\leq 150\text{ MHz}$ | | | 1.4 1.2 | ns | Note ⁽¹⁾ |
| $t_{sk(pp)}$ | Part-to-Part Skew PECL_CLK $> 150\text{ MHz}$ CMOS_CLK $> 150\text{ MHz}$ | | | 1.7 1.4 | ns | Note ⁽¹⁾ |
| $t_{sk(pp)}$ | Part-to-Part Skew PECL_CLK CMOS_CLK | | | 850 750 | ps | Note ⁽²⁾ |
| DC | Output Duty Cycle $f_{CLK} < 134\text{ MHz}$ $f_{CLK} \leq 250\text{ MHz}$ | 45 40 | 50 50 | 55 60 | % % | Input DC = 50% Input DC = 50% |
| t_r, t_f | Output Rise/Fall Time | 0.3 | | 1.1 | ns | 0.5 – 2.4 V |

1. Across temperature and voltage ranges. Includes output skew.

2. For specific temperature and voltage. Includes output skew.

Table 5. DC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{ V} \pm 5\%$; $V_{CCO} = 2.5\text{ V} \pm 5\%$)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|-----------|----------------------------------|----------|-----------------|-----|-----------------|---------------|--------------------------|
| V_{IH} | Input HIGH Voltage | CMOS_CLK | 2.4 | | V_{CCI} | V | |
| V_{IL} | Input LOW Voltage | CMOS_CLK | | | 0.8 | V | |
| V_{PP} | Peak-to-Peak Input Voltage | PECL_CLK | 500 | | 1000 | mV | |
| V_{CMR} | Common Mode Range | PECL_CLK | $V_{CCI} - 1.4$ | | $V_{CCI} - 0.6$ | V | |
| V_{OH} | Output HIGH Voltage | | 1.8 | | | V | $I_{OH} = -12\text{ mA}$ |
| V_{OL} | Output LOW Voltage | | | | 0.5 | V | $I_{OL} = 12\text{ mA}$ |
| I_{IN} | Input Current | | | | ± 200 | μA | |
| C_{IN} | Input Capacitance | | | 4.0 | | pF | |
| C_{pd} | Power Dissipation Capacitance | | | 10 | | pF | per output |
| Z_{OUT} | Output Impedance | | | 23 | | Ω | |
| I_{CC} | Maximum Quiescent Supply Current | | | 0.5 | 1.0 | mA | |

Table 6. AC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{ V} \pm 5\%$; $V_{CCO} = 2.5\text{ V} \pm 5\%$)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|--------------|-------------------------|--|------------|------------|------------|--------|----------------------------------|
| f_{max} | Maximum Input Frequency | | | | 250 | MHz | |
| t_{PLH} | Propagation Delay | PECL_CLK $\leq 150\text{ MHz}$ CMOS_CLK $\leq 150\text{ MHz}$ | 2.0 1.7 | 2.8 2.5 | 3.5 3.0 | ns | |
| t_{PLH} | Propagation Delay | PECL_CLK $> 150\text{ MHz}$ CMOS_CLK $> 150\text{ MHz}$ | 2.0 1.8 | 2.9 2.5 | 3.8 3.3 | ns | |
| $t_{sk(o)}$ | Output-to-Output Skew | PECL_CLK CMOS_CLK | | | 150 150 | ps | |
| $t_{sk(pp)}$ | Part-to-Part Skew | PECL_CLK $\leq 150\text{ MHz}$ CMOS_CLK $\leq 150\text{ MHz}$ | | | 1.5 1.3 | ns | Note ⁽¹⁾ |
| $t_{sk(pp)}$ | Part-to-Part Skew | PECL_CLK $> 150\text{ MHz}$ CMOS_CLK $> 150\text{ MHz}$ | | | 1.8 1.5 | ns | Note ⁽¹⁾ |
| $t_{sk(pp)}$ | Part-to-Part Skew | PECL_CLK CMOS_CLK | | | 850 750 | ps | Note ⁽²⁾ |
| DC | Output Duty Cycle | $f_{CLK} < 134\text{ MHz}$ $f_{CLK} \leq 250\text{ MHz}$ | 45 40 | 50 50 | 55 60 | % % | Input DC = 50% Input DC = 50% |
| t_r, t_f | Output Rise/Fall Time | | 0.3 | | 1.2 | ns | 0.5 – 1.8 V |

1. Across temperature and voltage ranges. Includes output skew.

2. For specific temperature and voltage. Includes output skew.

Table 7. DC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{ V} \pm 5\%$; $V_{CCO} = 2.5\text{ V} \pm 5\%$)

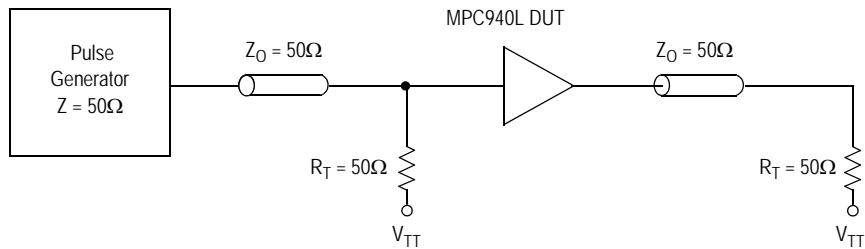
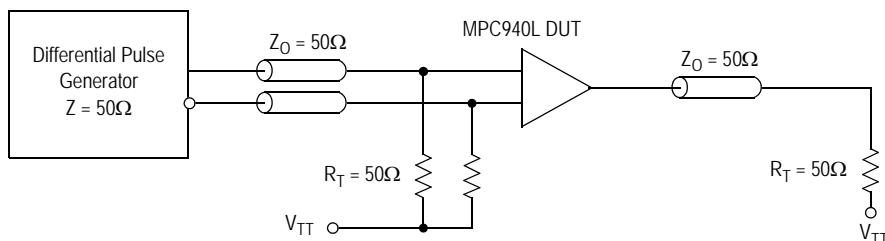
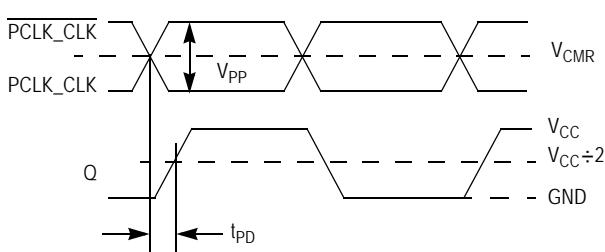
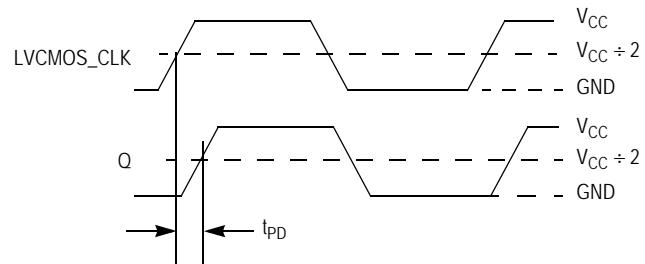
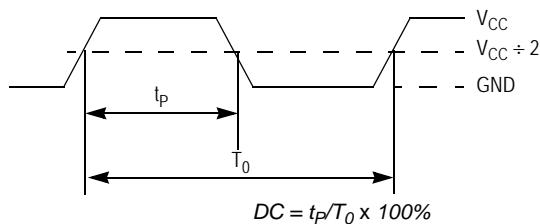
| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|-----------|----------------------------------|----------|-----------------|-----|-----------------|---------------|--------------------------|
| V_{IH} | Input HIGH Voltage | CMOS_CLK | 2.0 | | V_{CCI} | V | |
| V_{IL} | Input LOW Voltage | CMOS_CLK | | | 0.8 | V | |
| V_{PP} | Peak-to-Peak Input Voltage | PECL_CLK | 500 | | 1000 | mV | |
| V_{CMR} | Common Mode Range | PECL_CLK | $V_{CCI} - 1.0$ | | $V_{CCI} - 0.6$ | V | |
| V_{OH} | Output HIGH Voltage | | 1.8 | | | V | $I_{OH} = -12\text{ mA}$ |
| V_{OL} | Output LOW Voltage | | | | 0.5 | V | $I_{OL} = 12\text{ mA}$ |
| I_{IN} | Input Current | | | | ± 200 | μA | |
| C_{IN} | Input Capacitance | | | 4.0 | | pF | |
| C_{pd} | Power Dissipation Capacitance | | | 10 | | pF | per output |
| Z_{OUT} | Output Impedance | | 18 | 23 | 28 | Ω | |
| I_{CC} | Maximum Quiescent Supply Current | | | 0.5 | 1.0 | mA | |

Table 8. AC Characteristics ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{ V} \pm 5\%$; $V_{CCO} = 2.5\text{ V} \pm 5\%$)

| Symbol | Characteristic | | Min | Typ | Max | Unit | Condition |
|--------------|-------------------------|--|------------|------------|------------|--------|----------------------------------|
| f_{max} | Maximum Input Frequency | | | | 200 | MHz | |
| t_{PLH} | Propagation Delay | PECL_CLK $\leq 150\text{ MHz}$ CMOS_CLK $\leq 150\text{ MHz}$ | 2.6 2.3 | 4.0 3.1 | 5.2 4.0 | ns | |
| t_{PLH} | Propagation Delay | PECL_CLK $> 150\text{ MHz}$ CMOS_CLK $> 150\text{ MHz}$ | 2.8 2.3 | 3.8 3.1 | 5.0 4.0 | ns | |
| $t_{sk(o)}$ | Output-to-Output Skew | PECL_CLK CMOS_CLK | | | 200 200 | ps | |
| $t_{sk(pp)}$ | Part-to-Part Skew | PECL_CLK $\leq 150\text{ MHz}$ CMOS_CLK $\leq 150\text{ MHz}$ | | | 2.6 1.7 | ns | Note ⁽¹⁾ |
| $t_{sk(pp)}$ | Part-to-Part Skew | PECL_CLK $> 150\text{ MHz}$ CMOS_CLK $> 150\text{ MHz}$ | | | 2.2 1.7 | ns | Note ⁽¹⁾ |
| $t_{sk(pp)}$ | Part-to-Part Skew | PECL_CLK CMOS_CLK | | | 1.2 1.0 | ns | Note ⁽²⁾ |
| DC | Output Duty Cycle | $f_{CLK} < 134\text{ MHz}$ $f_{CLK} \leq 200\text{ MHz}$ | 45 40 | 50 50 | 55 60 | % % | Input DC = 50% Input DC = 50% |
| t_r, t_f | Output Rise/Fall Time | | 0.3 | | 1.2 | ns | 0.5 - 1.8 V |

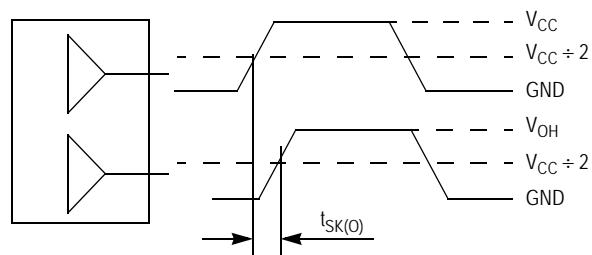
1. Across temperature and voltage ranges. Includes output skew.

2. For specific temperature and voltage. Includes output skew.

Figure 1. LVCMOS_CLK MPC940L AC Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$ Figure 2. PECL_CLK MPC940L AC Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$ Figure 3. Propagation Delay (t_{PD}) Test ReferenceFigure 4. LVCMOS Propagation Delay (t_{PD}) Test Reference

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 5. Output Duty Cycle (DC)



The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device.

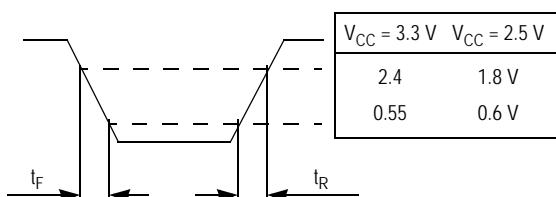
Figure 6. Output-to-Output Skew $T_{SK(O)}$ 

Figure 7. Output Transition Time Test Reference

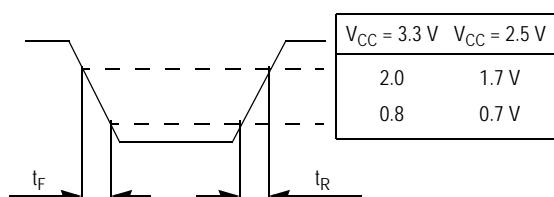
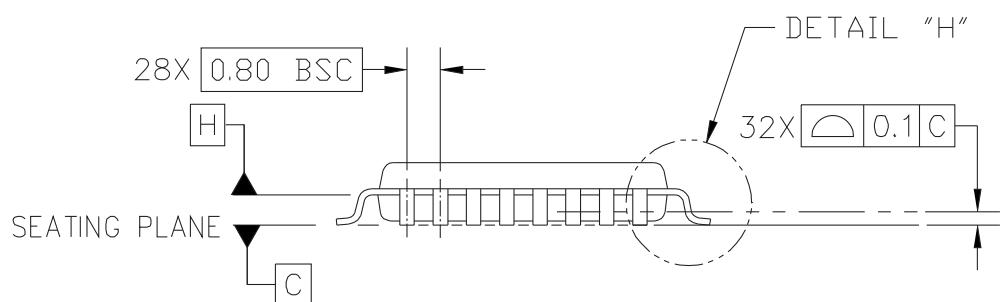
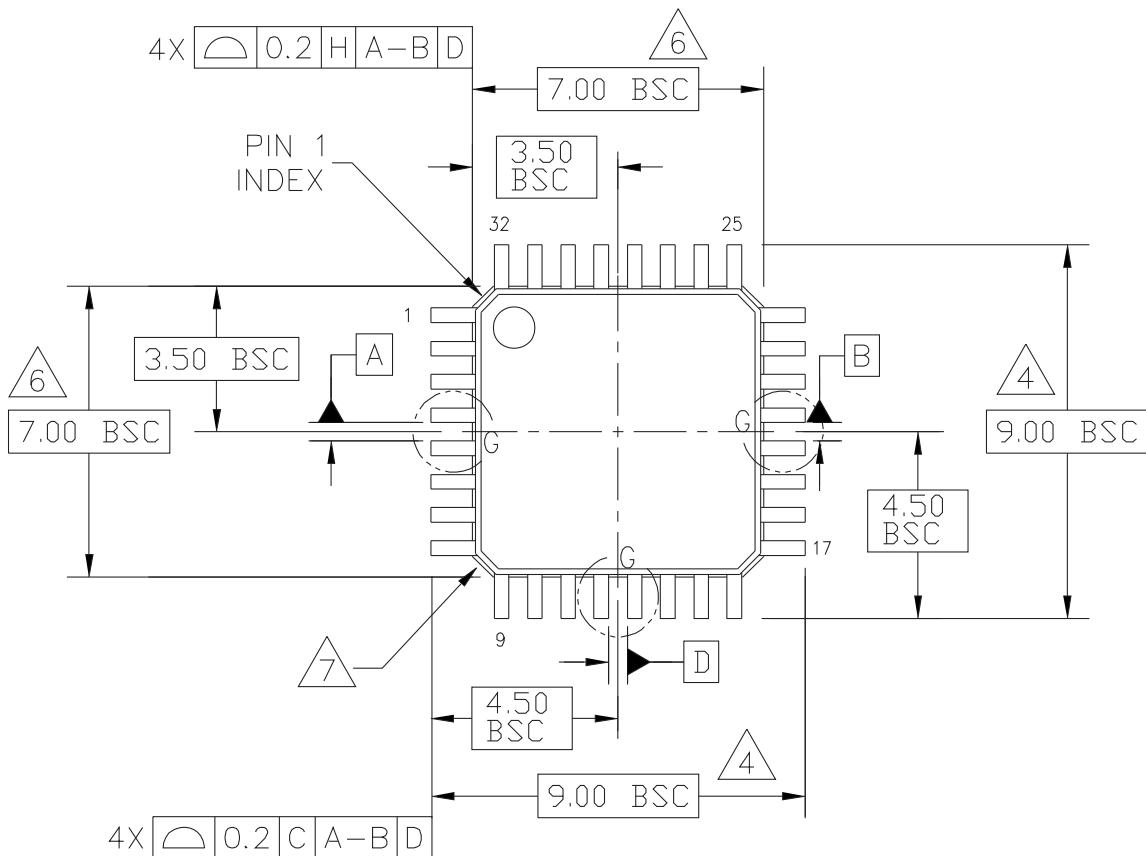


Figure 8. Input Transition Time Test Reference

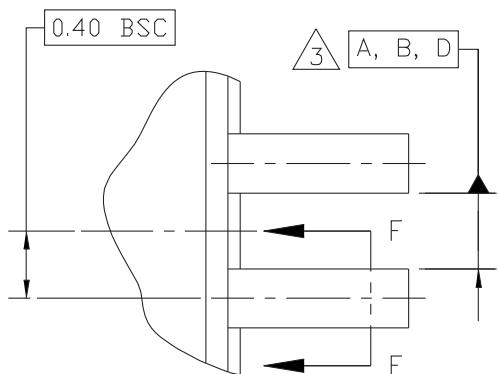
PACKAGE DIMENSIONS



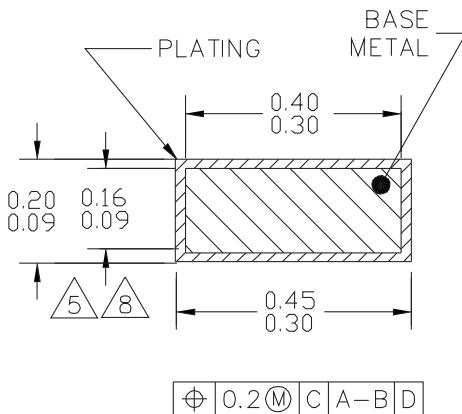
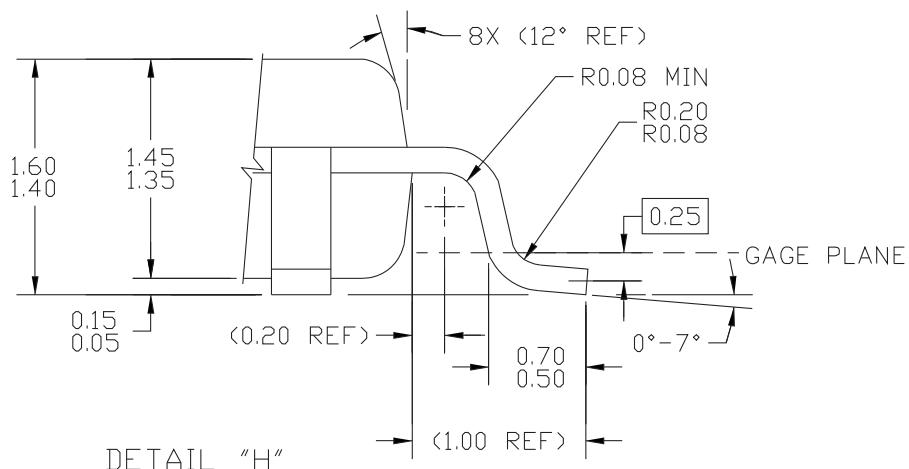
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| TITLE: | DOCUMENT NO: 98ASH70029A | REV: C |
| LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | CASE NUMBER: 873A-04 | 01 APR 2005 |
| | STANDARD: JEDEC MS-026 BBA | |

**CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE**

PACKAGE DIMENSIONS



DETAIL G

SECTION F-F
ROTATED 90°CW
32 PLACES

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**CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

| | | |
|---|--|----------------------------|
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| TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | DOCUMENT NO: 98ASH70029A CASE NUMBER: 873A-04 STANDARD: JEDEC MS-026 BBA | REV: C 01 APR 2005 |
| | | |

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**CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE**

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Termperture |
|-------------------|-----------|-------------------------|--------------------|-------------|
| MPC940LAC | MPC940LAC | Lead-Free, 32 Lead LQFP | Tray | 0°C to 70°C |
| MPC940LACR2 | MPC940LAC | Lead-Free, 32 Lead LQFP | 2500 Tape & Reel | 0°C to 70°C |

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|---|----------|
| 8 | | 1 | NRND – Not Recommend for New Designs. | 12/20/12 |
| 8 | | 1 | Product Discontinuation Notice - PDN CQ-15-02. | 5/6/15 |
| 9 | | 1 | Obsolete per Product Discontinuation Notice - PDN CQ-15-02. | 10/4/16 |

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