BUFFER/CLOCK DRIVER

MK3805

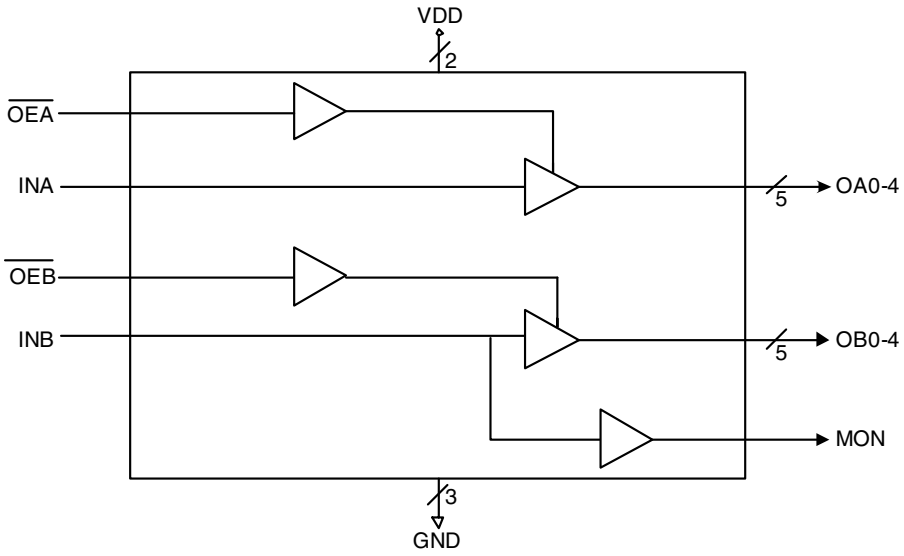
Description

The MK3805 is a non-inverting clock driver/buffer providing two independent banks of four outputs each. These buffers have a tri-state output enable input (active low) with 1-input, 5-output configuration per group. The skew between the outputs of the same package is 0.5 ns and the skew between the outputs of different packages is 0.8 ns. The maximum input to output delay is 4.5 ns.

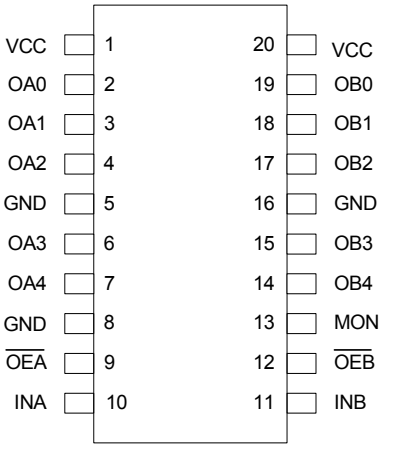
Features

- Packaged in 20-pin SSOP
- Pb (lead) free package
- Five outputs for each bank with one clock input
- Two separate banks of five outputs each
- Advanced, low-power, CMOS process
- Ten output clocks
- Two separate inputs
- Industrial temperature range -40° C to +85° C
- Hysteresis on all inputs

Block Diagram



Pin Assignment



20 pin (150 mil) SSOP/20 pin (300mil) SOIC

Truth Table

Inputs		Outputs	
$\overline{OEA}$, $\overline{OEB}$	INA, INB	OAN, OBN	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VCC	Power	Connect to +3.3 V.
2	OA0	Output	Clock output.
3	OA1	Output	Clock output.
4	OA2	Output	Clock output.
5	GND	Power	Connect to ground.
6	OA3	Output	Clock output.
7	OA4	Output	Clock output.
8	GND	Power	Connect to ground.
9	$\overline{OEA}$	Input	Tri state output enable input (active low).
10	INA	Input	Clock input.
11	INB	Input	Clock input.
12	$\overline{OEB}$	Input	Tri state output enable input (active low).
13	MON	Output	Monitor output.
14	OB4	Output	Clock output.
15	OB3	Output	Clock output.
16	GND	Power	Connect to ground.
17	OB2	Output	Clock output.
18	OB1	Output	Clock output.
19	OB0	Output	Clock output.
20	VCC	Power	Connect to +3.3 V.

External Components

The MK3805 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01µF must be connected between VDD and GND, as close to these pins as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through the signal layers. Other signal traces should be routed away from the MK3805. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3805. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.13	+3.3	+3.46	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40° C to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13	3.3	3.46	V
Supply Current	IDD	No load, $\overline{OEA}$,$\overline{OEB}$ GND, fo=10MHz, 50% duty cycle		3.3		mA
	IDD	No load, $\overline{OEA}$,$\overline{OEB}$ GND, fo=2.5MHz, 50% duty cycle		1.8		mA
Quiescent Current	ICC			3	30	µA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}	CLK output		±50		mA
Input Capacitance				5		pF
Nominal Output Impedance	Z_O			20		Ω
Input Hysteresis	V_H			150		mV

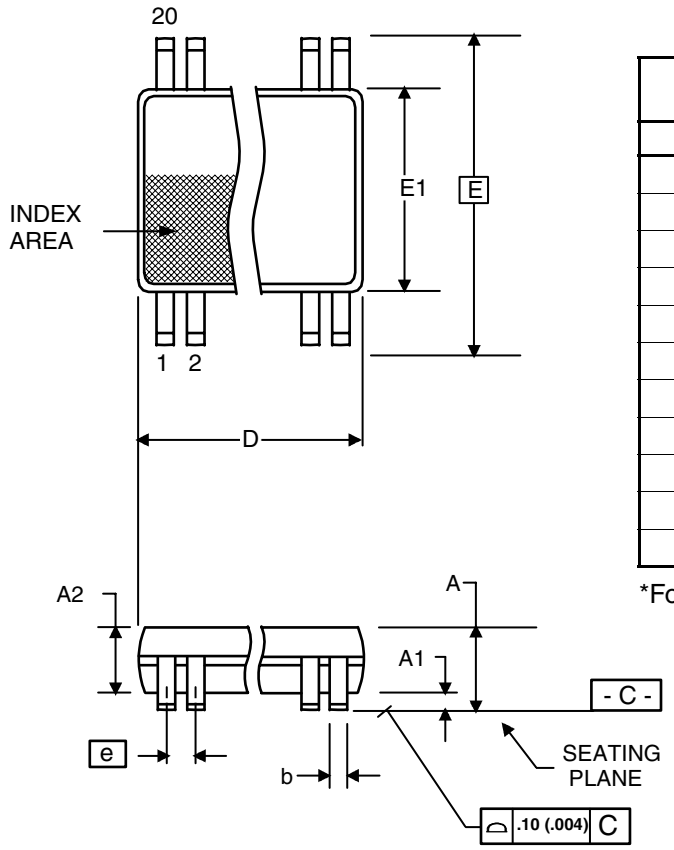
AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40° C to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Skew between outputs of same package)	$tsk_{(o)}$	CL=50 pF, RL=500Ω			0.5	ns
Skew between outputs of different packages at same temp (same transition)	$tsk_{(t)}$	CL=50 pF, RL=500Ω			0.8	ns
Propagation Delay INA to OAN INB to OBN	t_{PLH}, t_{PHL}	CL=50 pF, RL=500Ω	1.5		4.5	ns
Output Rise Time 0.8 V to 2.0 V	t_R	CL=50 pF, RL=500Ω			2	ns
Output Fall Time 2.0 V to 0.8 V	t_F	CL=50 pF, RL=500Ω			2	ns
Output Enable Time	$\overline{OEA}$ to OAN, $\overline{OEB}$ to OBN	CL=50 pF, RL=500Ω	1.5		6.2	ns
Output Disable Time	$\overline{OEA}$ to OAN, $\overline{OEB}$ to OBN	CL=50 pF, RL=500Ω	1.5		5.0	ns
Duty Cycle Measured at VDD/2		CL=50 pF, RL=500Ω	45		55	%
Operating Frequency		CL=50 pF, RL=500Ω	1		100	MHz

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	0.008	0.012
C	0.18	0.25	.007	.010
D	8.55	8.75	.337	.344
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK3805RILF	MK3805RILF	Tubes	20-pin SSOP	-40 to +85° C
MK3805RILFTR	MK3805RILF	Tape and Reel	20-pin SSOP	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.