VCXO AND MULTIPLIER

MK3732-10

Description

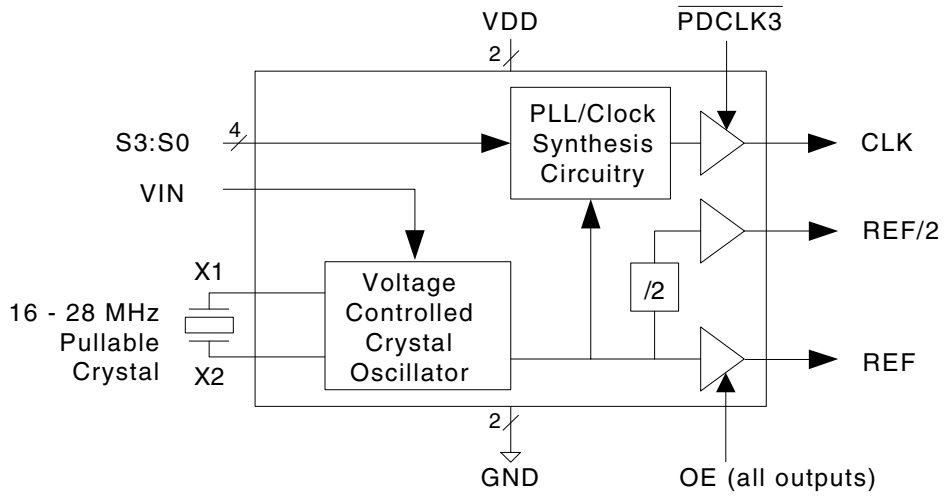
The MK3732-10 is a low cost, low jitter, high performance VCXO and PLL clock synthesizer designed to replace expensive discrete VCXOs and multipliers. The patented on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ±115 ppm. Using IDT' analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 27 MHz pullable crystal input to produce three output clocks.

IDT manufactures the largest variety of MPEG clock synthesizers for all applications. Consult IDT to eliminate VCXOs, crystals, and oscillators from your board.

Features

- Packaged in 16 pin SOIC
- Replaces a VCXO and oscillator
- Contains popular multiplier values
- Uses an inexpensive 27 MHz pullable crystal
- Includes popular audio frequencies from 27 MHz
- On-chip patented VCXO with pull range of 230 ppm (±115 ppm) minimum
- VCXO tuning voltage of 0 to 3.3 V
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V

Block Diagram



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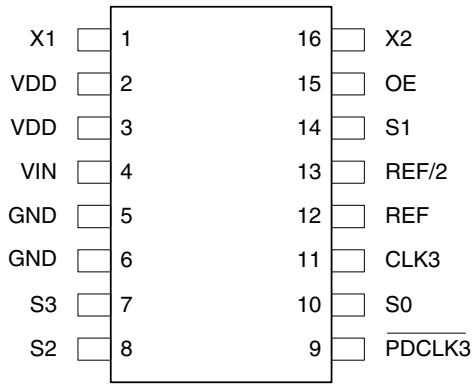
Pin Assignment



16 Pin (150 mil) SOIC

Clock Select Table

S3	S2	S1	S0	Input	CLK1	CLK2	CLK3	Multiplier
0	0	0	0	16 - 28	REF/2	REF	20 - 35	x1.25
0	0	0	1	16 - 28	REF/2	REF	21 - 37.5	x1.333
0	0	1	0	16 - 28	REF/2	REF	24 - 42	x1.5
0	0	1	1	16 - 28	REF/2	REF	32 - 56	x2
0	1	0	0	16 - 28	REF/2	REF	40 - 70	x2.5
0	1	0	1	16 - 28	REF/2	REF	42 - 75	x2.667
0	1	1	0	16 - 28	REF/2	REF	48 - 84	x3
0	1	1	1	TEST				
1	0	0	0	16 - 28	REF/2	REF	64 - 112	x4
1	0	0	1	16 - 28	REF/2	REF	80 - 140	x5
1	0	1	0	16 - 28	REF/2	REF	85 - 150	x5.333
1	0	1	1	16 - 27	REF/2	REF	96 - 162	x6
1	1	0	0	27	13.5	27	11.289	N/A
1	1	0	1	27	13.5	27	12.288	N/A
1	1	1	0	27	13.5	27	8.192	N/A
1	1	1	1	27	13.5	27	24.576	N/A

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Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI	XI	Crystal connection. Connect to a pullable of 16 to 28 MHz cyrstal.
2 - 3	VDD	Power	Connect to +3.3 V.
4	VIN	Input	Voltage input to VCXO. Zero to 3.3V signal which controls the VCXO frequency.
5 - 6	GND	Power	Connect to ground.
7	S3	Input	Select input #3. Selects outputs per table above. Internal pull-up resistor.
8	S2	Input	Select input #2. Selects outputs per table above. Internal pull-up resistor.
9	$\overline{\text{PDCLK3}}$	Input	Power down for CLK3.
10	S0	Input	Select input #0. Selects outputs per table above. Internal pull-up resistor.
11	CLK3	Output	PLL output clock that is either a multiple of the input or an audio clock. See table above.
12	REF	Output	Buffered VCXO reference clock output. Matches crystal frequency.
13	REF/2	Output	Reference clock output divided by two.
14	S1	Input	Select input #1. Selects outputs per table above. Internal pull-up resistor.
15	OE	Input	Output enable. Tri-states outputs when low. Internal pull-up resistor.
16	X2	XO	Crystal connection. Connect to a pullable 16 to 28 MHz crystal.

Pin Descriptions

The MK3732-10 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between VDD and GND on pins 2 and 5 and pins 3 and 6, as close to the MK3732-10 as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB traces between the clock outputs (CLK, pin 5) and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Quartz Crystal

The MK3732-10 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The MK3732-10 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the MK3732-10 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14pF.

Recommended Crystal Parameters:

Initial Accuracy at 25° C	±20 ppm
Temperature Stability	±30 ppm

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Aging	±20 ppm
Load Capacitance	14 pf
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	250 Max
Equivalent Series Resistance	35 Ω Max

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3732-10. There should be no via's between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal. **See application note MAN05.**

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

The procedure for determining the value of these capacitors can be found in application note MAN05.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3732-10. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.15	3.3	+3.45	V
Reference crystal parameters	Refer to pages 3 - 4			

DC Electrical Characteristics

VDD=3.3V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Input High Voltage	V_{IH}	X1 pin, clock in Non VCXO mode	(VDD/2)+1			V
Input Low Voltage	V_{IL}	X1 pin, clock in Non VCXO mode			(VDD/2)-1	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	-0.5			V
Operating Supply Current	IDD	No Load		19		mA
Short Circuit Current		Each output		±50		mA
Input Capacitance	C_{IN}	S2:S0, OE		5		pF
Frequency Synthesis Error		All clocks			0	ppm
VIN, VCXO Control Voltage	V_{IA}		0		3.3	V

AC Electrical Characteristics

VDD = 3.3V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Crystal Frequency	f_{IN}		16	27	28	MHz
Output Clock Frequency	f_{OUT}		8		162	MHz
Output Clock Rise Time		0.8 to 2.0V		1.5		ns
Output Clock Fall Time		2.0 to 0.8V		1.5		ns
Output Clock Duty Cycle		at VDD/2	40		60	%
Maximum Absolute Jitter				±350		ps
Output pullability		0V < VIN < 3.3V, Note 1	±115			ppm

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on pages 3-4.

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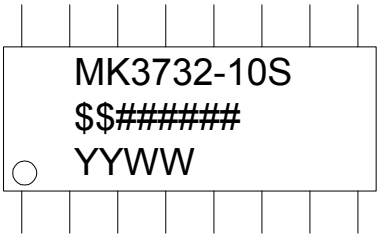
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Marking Diagram



Notes:

1. ###### is the lot number
2. YYWW is the last two digits of the year and the week number that the part was assembled

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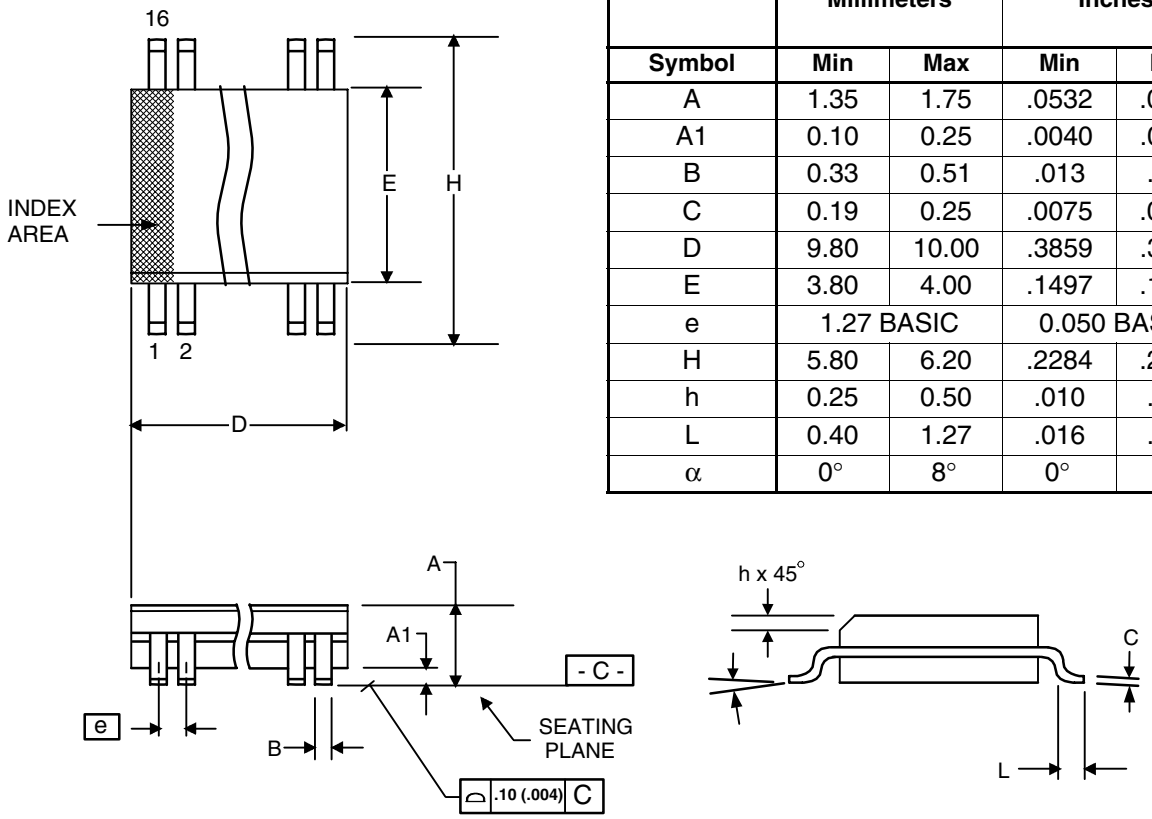
Package Outline and Package Dimensions (16 pin SOIC)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
MK3732-10SLF	MK3732-10LF	Tubes	16 pin SOIC	0 to +70° C
MK3732-10SLFTR	MK3732-10LF	Tape and Reel	16 pin SOIC	0 to +70° C

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