

Description

The MK2304-2 is a low jitter, low skew, high performance Phase Lock Loop (PLL) based zero delay buffer for high speed applications. Based on IDT's proprietary low jitter PLL techniques, the device provides four low skew outputs at speeds up to 133 MHz at 3.3 V. The MK2304-2 includes a bank of two outputs running at 1/2X. In the zero delay mode, the rising edge of the input clock is aligned with the rising edges of all 4 outputs. Compared to competitive CMOS devices, the MK2304-2 has the lowest jitter.

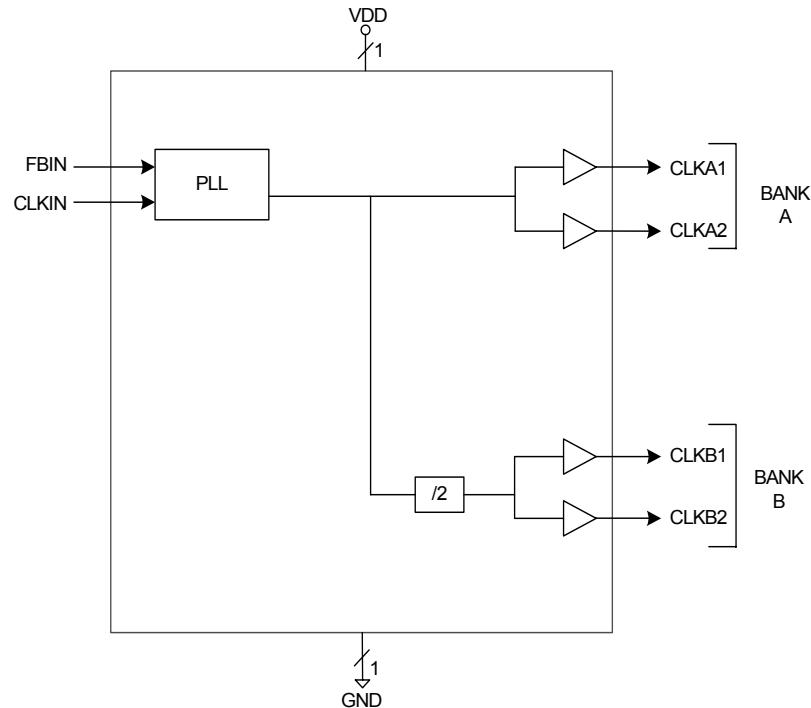
The MK2304-2 PLL enters a power-down state when there are no rising edges on the REF input. In this mode, all outputs are tri-stated and the PLL is turned off, resulting in less than 25 μ A of current draw.

IDT manufactures the largest variety of clock generators and buffers and is the largest clock supplier in the world.

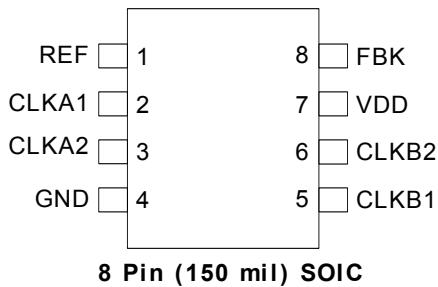
Features

- Packaged in 8 pin SOIC
- Zero input-output delay
- Two 1X outputs plus two 1/2X outputs
- Output to output skew is less than 200 ps
- Output clocks up from 10 MHz to 133 MHz at 3.3 V
- Ability to generate 2X the input
- Full CMOS outputs with 8 mA output drive capability at TTL levels at 3.3 V
- Spread Smart™ technology works with spread spectrum clock generators
- Advanced, low power, sub micron CMOS process
- Operating voltage of 3.3 V
- Available in industrial temperature operation
- Pb (lead) free package
- Low Standby Current

Block Diagram



Pin Assignment



Feedback Configuration Table

Feedback From	CLKA1:A2	CLKB1:B2
Bank A	CLKIN	CLKIN/2
Bank B	2XCLKIN	CLKIN

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	REF	Input	Clock input. Connect to input clock source, 5 V tolerant input.
2	CLKA1	Output	Clock A1 output.
3	CLKA2	Output	Clock A2 output.
4	GND	Power	Connect to ground.
5	CLKB1	Output	Clock B1 output.
6	CLKB1	Output	Clock B2 output.
7	VDD	Power	3.3V Power Supply.
8	FBK	Input	PLL feedback input

External Components

The MK2304-2 requires a minimum number of external components for proper operation. Decoupling capacitors of $0.1\mu\text{F}$ should be connected between VDD and GND, as close to the part as possible. A 33Ω series terminating resistor should be used on each clock output to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2304-2. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs, except CLKIN	-0.5 V to VDD+0.5 V
CLKIN	-0.5 V to +5.5 V
Ambient Operating Temperature (commercial)	0 to +70 °C
Ambient Operating Temperature (industrial)	-40 to +85 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	125 °C
Soldering Temperature	260 °C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	°C
Ambient Operating Temperature (industrial)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

VDD=3.3 V ±10%, Amb temp -40° C to 85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V _{IH}		2			V
Input Low Voltage	V _{IL}				0.8	V
Output High Voltage	V _{OH}	I _{OH} = -8 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 8 mA			0.4	V
Operating Supply Current 100 MHz, CLKIN	IDD	No Load		45		mA
Stand by Supply Current 0 MHz, CLKIN	IDD	No Load		12	25	uA
Short Circuit Current	I _{OS}	Each output		TBD		mA
Input Capacitance	C _{IN}	FBIN		7		pF
Power-up Time					50	ms

AC Electrical Characteristics

VDD = 3.3V $\pm 10\%$, Ambient Temperature -40° C to 85° C

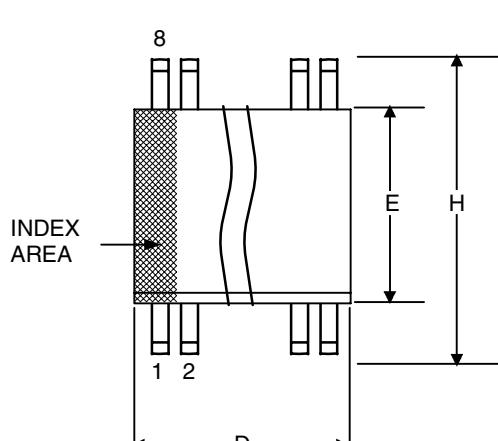
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency		FBIN to CLKA1, 30 pF Load	10		100	MHz
Output Frequency		FBIN to CLKA1, 15 pF Load	10		133	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, $C_L=30$ pF			2.2	ns
Output Rise Time	t_{OR}	0.8 to 2.0 V, $C_L=15$ pF			1.5	ns
Output Fall Time	t_{OF}	0.8 to 2.0 V, $C_L=30$ pF			2.2	ns
Output Fall Time	t_{OF}	0.8 to 2.0 V, $C_L=15$ pF			1.5	ns
Output Clock Duty Cycle		At 1.4 V, $C_L=30$ pF	40	50	60	%
Output Clock Duty Cycle		At 1.4 V, $C_L=15$ pF	45	50	65	%
Device-to-Device skew, equally loaded		Rising edges at VDD/2			500	ps
Output-to-Output skew, equally loaded, On same bank		Rising edges at VDD/2			200	ps
Skew from Output Bank A to Output Bank B		All outputs equally loaded			400	ps
Delay CLKIN Rising Edge to FBIN Rising Edge		Measured at VDD/2			± 250	ps
Cycle-to-Cycle Jitter		30 pF loads 66.67 MHz outputs			400	ps
		15 pF loads 66.67 MHz outputs			375	ps
PLL Lock Time	t_{LOCK}	Stable power supply, valid clocks on CLKIN, FBIN			1	ms

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

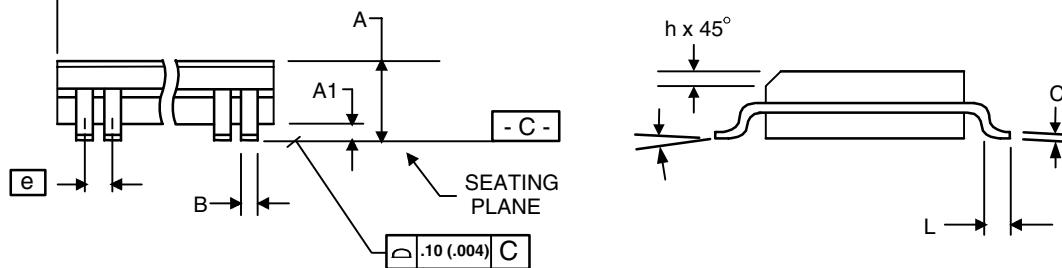
Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions are in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK2304S-2LF	2304S02L	Tubes	8-pin SOIC	0 to 70° C
MK2304S-2LFTR	2304S02L	Tape and Reel	8-pin SOIC	0 to 70° C
MK2304S-2ILF	2304S2IL	Tubes	8-pin SOIC	-40° C to 85° C
MK2304S-2ILFTR	2304S2IL	Tape and Reel	8-pin SOIC	-40° C to 85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

MK2304-2

ZERO DELAY, LOW SKEW BUFFER

ZDB

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.