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April 1st, 2010
Renesas Electronics Corporation

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M61530FP

4ch Electronic Volume with 5.1ch Analog Input

REJ03F0058-0100Z
Rev.1.0
Sep.19.2003

Description

The M61530FP is a four-channel volume IC which is optimal for combination with the M61519FP two-channel electronic volume. A multi-channel system is easily configured with the aid of these two chips.

Features

Function names	Features
Main volume control	0 to –87 dB in 1-dB steps, –∞ Four independently controlled volumes (SL, SR, C, LFE)
Low pass filter (LPF)	On-chip operational amplifiers for configuration of post-filters through the addition of external C and R elements
AGC	AGC circuit is included to prevent clipping <SW ch>
Bass boost	HPF type, with on/off switch <SL/SR ch>
Output gain control	0, +6, +9, or +12 dB (four steps) <SW ch>
Input gain control	0, +5, +10 dB (three steps) <FL/FR ch>
Microcomputer I/F	Two-line serial data control

Application

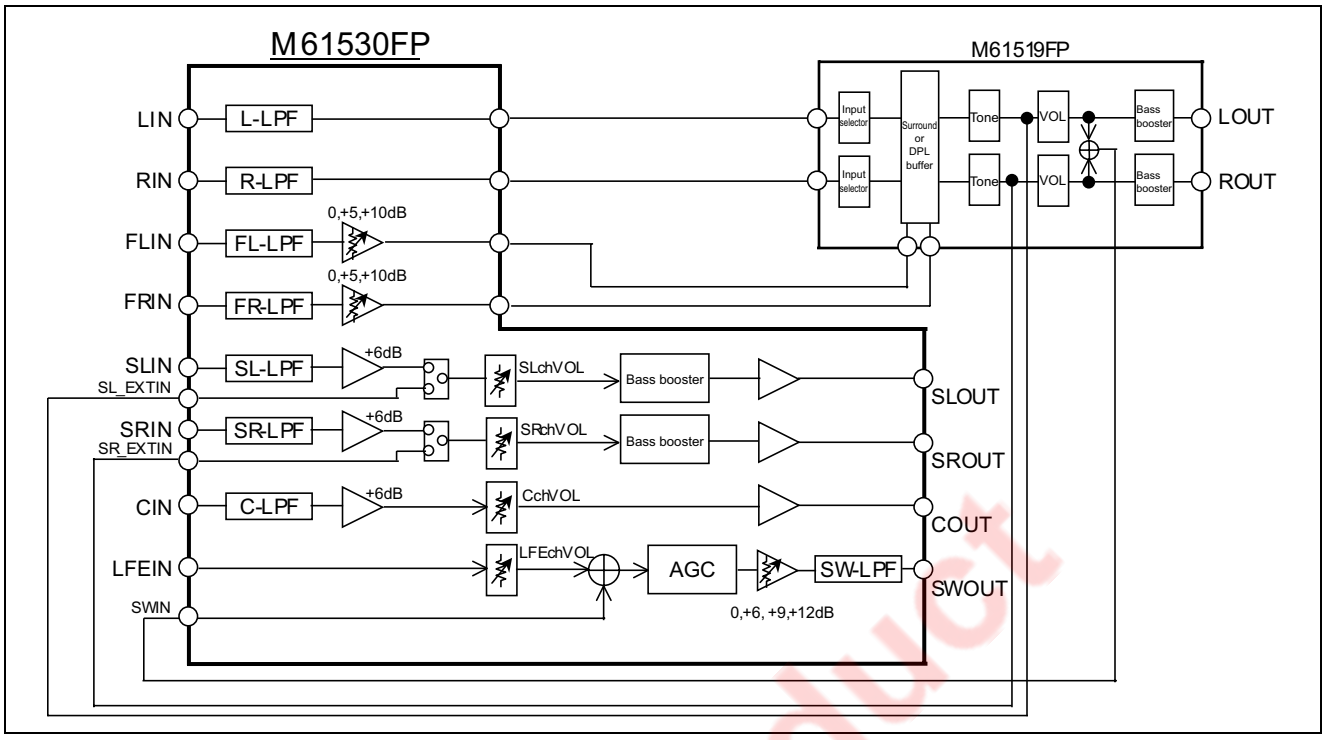
Mini-component systems, micro-component systems, etc.

Recommended Operating Conditions

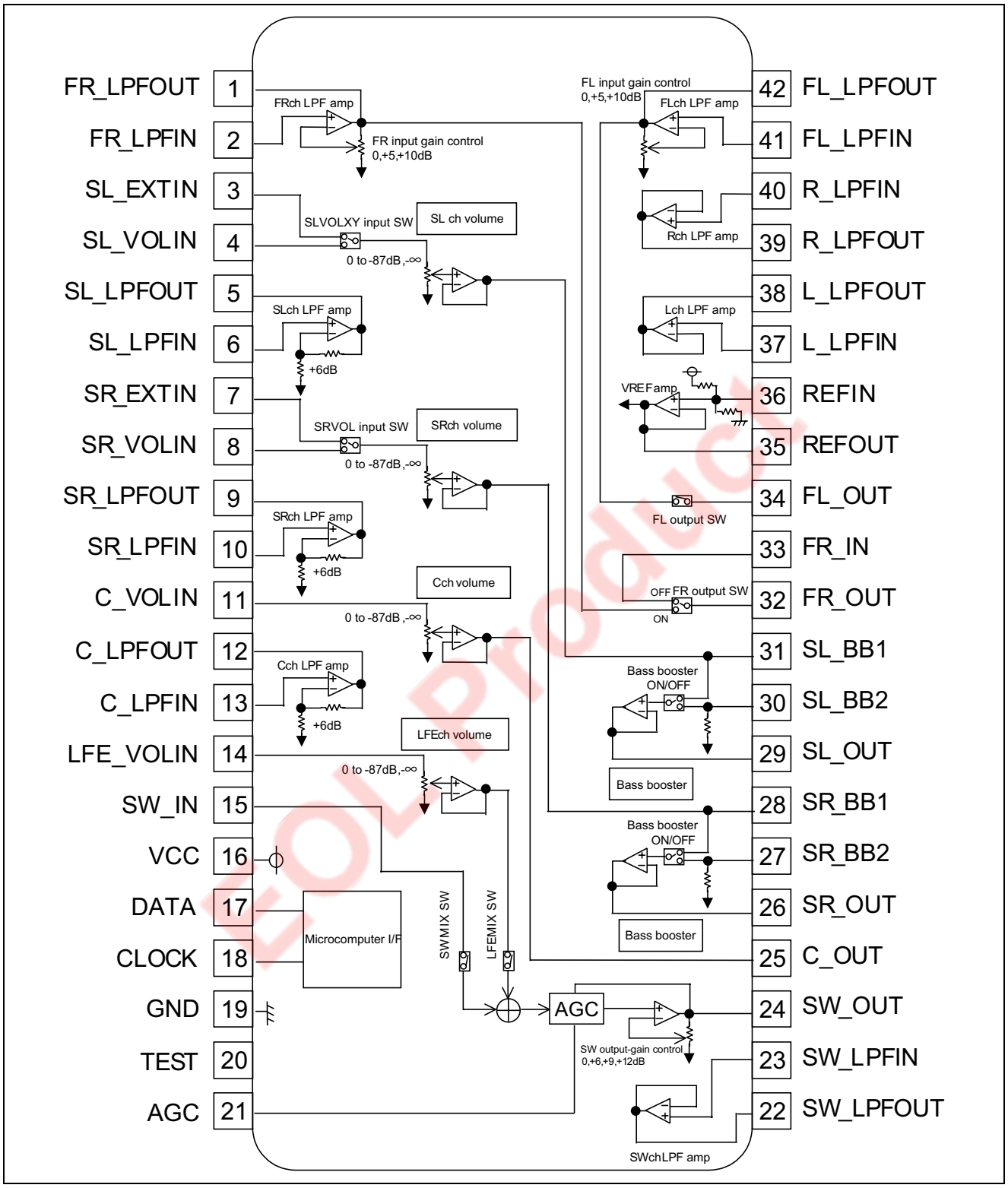
Power-supply voltage range: Vcc = 8 to 10 V

Rated power-supply voltage: Vcc = 9 V

System Block Diagram



Block diagram with pin connections

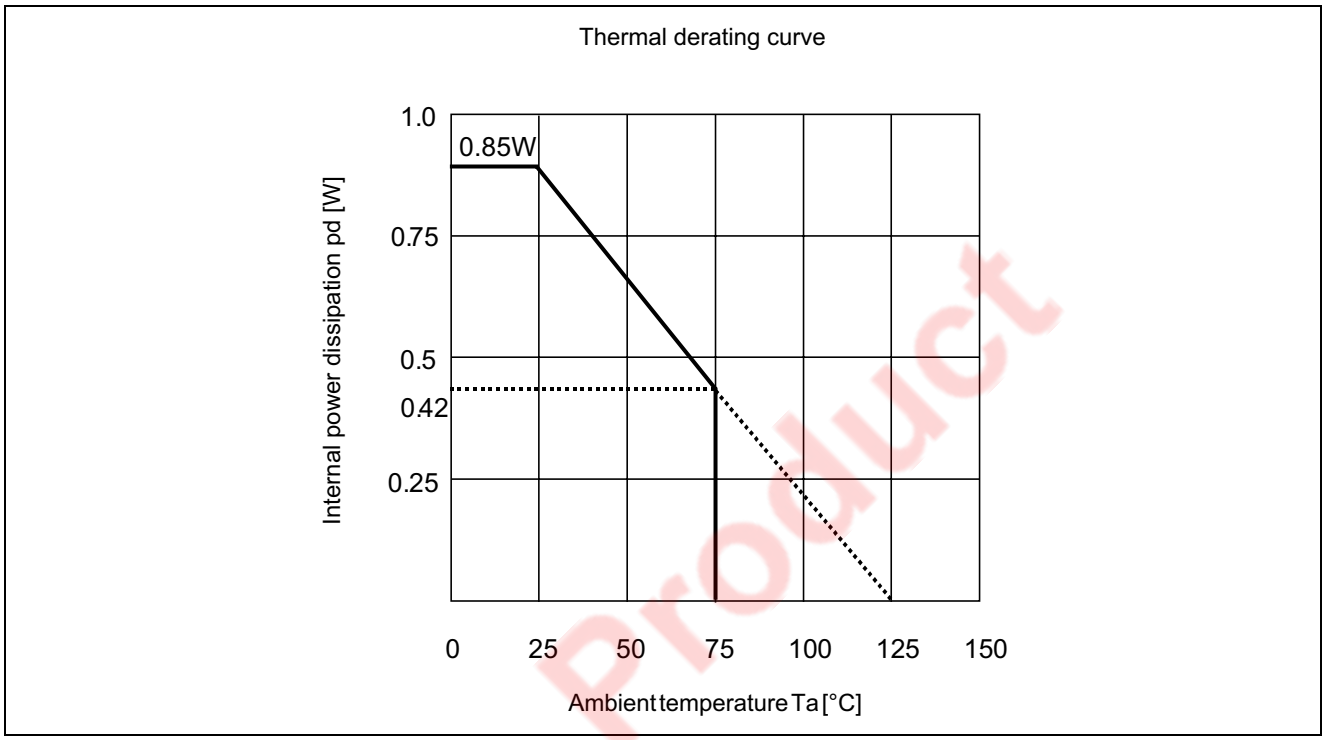


Pin description

Pin No.	Pin Name	Description
1	FR_LPFOUT	Configure a low-pass filter by adding external C and R elements to the input of the FR channel
2	FR_LPFIN	
3	SL_EXTIN	SL channel external input pin
4	SL_VOLIN	SL channel volume input pin
5	SL_LPFOUT	Configure a low-pass filter by adding external C and R elements to the input of the SL channel
6	SL_LPFIN	
7	SR_EXTIN	SR channel external input pin
8	SR_VOLIN	SR channel volume input pin
9	SR_LPFOUT	Configure a low-pass filter by adding external C and R elements to the input of SR channel
10	SR_LPFIN	
11	C_VOLIN	C channel volume input pin
12	C_LPFOUT	Configure a low-pass filter by adding external C and R elements to the input of the C channel
13	C_LPFIN	
14	LFE_VOLIN	LFE channel volume input pin
15	SW_IN	SW channel input pin
16	VCC	Power-supply pin for internal analog and digital circuitry (VCC = 9 V)
17	DATA	DATA input pin for serial data transfer
18	CLOCK	CLOCK input pin for serial data transfer
19	GND	GND pin for internal analog and digital circuitry
20	TEST	Pin for setting the test mode (normally fixed low)
21	AGC	C connection pin for setting attack/recovery time for AGC
22	SW_LPFOUT	Configure a low-pass filter by adding external C and R elements to the input of the SW channel
23	SW_LPFIN	
24	SW_OUT	SW channel output pin
25	C_OUT	C channel output pin
26	SR_OUT	SR channel output pin
27	SR_BB2	Pin for connecting external components that set bass-boost frequency characteristics for the SR channel
28	SR_BB1	
29	SL_OUT	SL channel output pin
30	SL_BB2	Pin for connecting external components that set bass-boost frequency characteristics for the SL channel
31	SL_BB1	
32	FR_OUT	FR channel output pin
33	FR_IN	Pin for interfacing with the M61519FP surround circuit
34	FL_OUT	FL channel output pin
35	REFOUT	Internal reference output pin
36	REFIN	Internal reference input pin
37	L_LPFI N	Configure a low-pass filter by adding external C and R elements to the input of the L channel
38	L_LPFOUT	
39	R_LPFOUT	Configure a low-pass filter by adding external C and R elements to the input of the R channel
40	R_LPFIN	
41	FL_LPFIN	Configure a low-pass filter by adding external C and R elements to the input the of FL channel
42	FL_LPFOUT	

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Conditions
Power-supply voltage	VCC	10.5	V	
Internal power dissipation	Pd	850	mW	Ta≤25°C
Thermal reduction rate	Kθ	8.6	mW/°C	Ta>25°C
Ambient operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

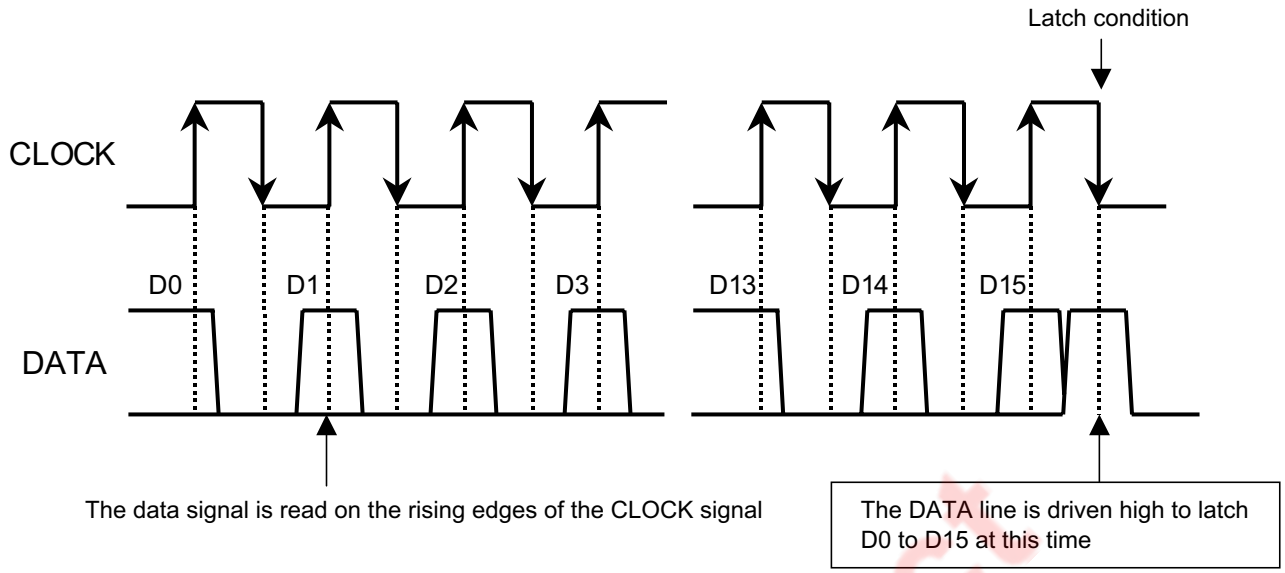


Recommended Operating Condition

(Unless otherwise noted, Ta = 25°C)

Item	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Power-supply voltage	VCC	8	9	10	V	
Logical high level input voltage	VIH	2.2	—	5.5	V	VCC=9V
Logical low level input voltage	VIL	0	—	0.6	V	VCC=9V

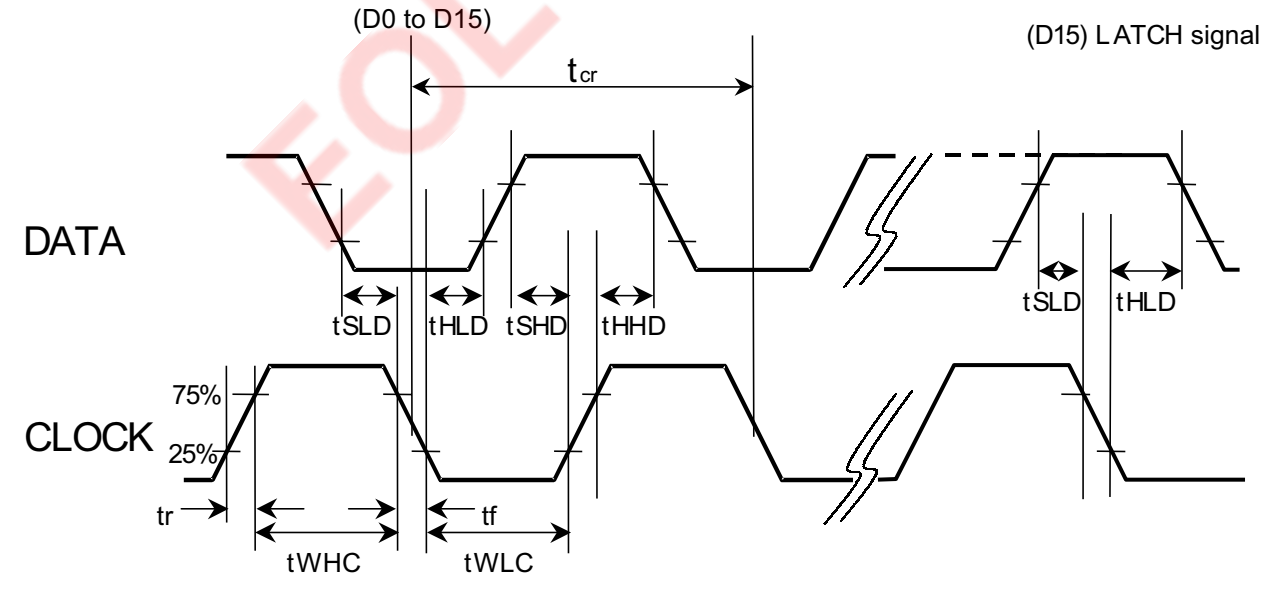
Relation between DATA and CLOCK



1. Data transmission
The DATA signal is read on the rising edges of the CLOCK signal. The DATA line must always be low on the falling edge of the CLOCK signal during transmission of the DATA signal.

2. Data Latch
Data for this IC is in 16-bits (D0 to D15) words. Latch the transmitted data by driving the DATA line high on the falling edge of the CLOCK signal after the transmission of D15.

CLOCK and DATA timing



Digital module timing

Item	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Clock: Cycle time	tcr	4	—	—	µS
Clock: Pulse width (high)	tWHC	1.6	—	—	
Clock: Pulse width (low)	tWLC	1.6	—	—	
Clock: Rising time	tr	—	—	0.4	
Clock: Falling time	tf	—	—	0.4	
Data: Setup time (high), clock rising	tSHD	0.8	—	—	
Data: Setup time (low), clock falling	tSLD	0.8	—	—	
Data: Hold time (high)	tHHD	0.8	—	—	
Data: Hold time (low)	tHLD	0.8	—	—	

Data input format

(Set all data shown below to the initial values every time power is turned on.)

(1)

D0a	D1a	D2a	D3a	D4a	D5a	D6a	D7a	D8a	D9a	D10a	D11a	D12a	D13a	D14	D15
(8) SLch trim potentiometer				(8) SRch trim potentiometer				(1) FL/FR input gain control		(2) FL/FR output SW	(3) Input SW for SL/SR volume	(4) LFEMIX SW	(5) SWMIX SW	0	0

(2)

D0b	D1b	D2b	D3b	D4b	D5b	D6b	D7b	D8b	D9b	D10b	D11b	D12b	D13b	D14	D15
(8) Cch trim potentiometer				(8) LFEch trim volume				(6) Bass boost	(7) SW output gain control		0	0	0	0	1

(3)

D0c	D1c	D2c	D3c	D4c	D5c	D6c	D7c	D8c	D9c	D10c	D11c	D12c	D13c	D14	D15
(9) SLch master volume					(9) SRch master volume					0	0	0	0	1	0

(4)

D0d	D1d	D2d	D3d	D4d	D5d	D6d	D7d	D8d	D9d	D10d	D11d	D12d	D13d	D14	D15
(9) Cch master volume					(9) LFEch master volume					0	0	0	0	1	1

Code settings

: Initial setting

(1) FL/FR input gain control

Setting	D8a	D9a
0dB	0	0
+5dB	0	1
+10dB	1	0

(3) Input switch for SL/SR volume

Setting	D11a
SL/SRch input	0
External input	1

(5) SW MIX SW

Setting	D13a
ON	0
OFF	1

(6) Bass boost

Setting	D8b
OFF	0
ON	1

(2) FL/FR output SW

Setting	D10a
ON	0
OFF	1

(4) LFE MIX SW

Setting	D12a
ON	0
OFF	1

(7) SW output gain control

Setting	D9b	D10b
0dB	0	0
+6dB	0	1
+9dB	1	0
+12dB	1	1

Note: Do not use data codes other than those specified above.

(8) SL/SR/C/LFEch trim volume

Attenuation	SLch	D0a	D1a	D2a	D3a
	SRch	D4a	D5a	D6a	D7a
	Cch	D0b	D1b	D2b	D3b
	LFEch	D4b	D5b	D6b	D7b
0dB		0	0	0	0
-1dB		0	0	0	1
-2dB		0	0	1	0
-3dB		0	0	1	1
-4dB		0	1	0	0
-5dB		0	1	0	1
-6dB		0	1	1	0
-7dB		0	1	1	1
-8dB		1	0	0	0
-9dB		1	0	0	1
-10dB		1	0	1	0
-11dB		1	0	1	1
-12dB		1	1	0	0
-13dB		1	1	0	1
-14dB		1	1	1	0
-15dB		1	1	1	1

(9) SL/SR/C/LFEch master volume

Attenuation	SLch	D0c	D1c	D2c	D3c	D4c
	SRch	D5c	D6c	D7c	D8c	D9c
	Cch	D0d	D1d	D2d	D3d	D4d
	LFEch	D5d	D6d	D7d	D8d	D9d
0dB		0	0	0	0	0
-2dB		0	0	0	0	1
-4dB		0	0	0	1	0
-6dB		0	0	0	1	1
-8dB		0	0	1	0	0
-10dB		0	0	1	0	1
-12dB		0	0	1	1	0
-14dB		0	0	1	1	1
-16dB		0	1	0	0	0
-18dB		0	1	0	0	1
-20dB		0	1	0	1	0
-22dB		0	1	0	1	1
-24dB		0	1	1	0	0
-26dB		0	1	1	0	1
-28dB		0	1	1	1	0
-30dB		0	1	1	1	1
-32dB		1	0	0	0	0
-34dB		1	0	0	0	1
-36dB		1	0	0	1	0
-38dB		1	0	0	1	1
-40dB		1	0	1	0	0
-42dB		1	0	1	0	1
-44dB		1	0	1	1	0
-48dB		1	0	1	1	1
-52dB		1	1	0	0	0
-56dB		1	1	0	0	1
-60dB		1	1	0	1	0
-64dB		1	1	0	1	1
-68dB		1	1	1	0	0
-72dB		1	1	1	0	1
-76dB		1	1	1	1	0
-∞dB		1	1	1	1	1

Note: When the sum of the trim potentiometer and master volume settings is –87 dB or less, the overall level is –87 dB (e.g. when the trim potentiometer is –15 dB and master volume is -76 dB, the total level becomes -87 dB).

Note: Do not use data codes other than those specified above.

Electrical characteristics

Unless otherwise noted, Ta = 25°C, Vcc = 9 V, f = 1 kHz, input gain control = 0 dB, bass boost = off, trim/master volume = 0 dB, FL/FR output SW = on, SL/SR VOL input SW = SL/SR input, LFE MIXS SW = on, SW MIX= off, output gain control = 0 dB

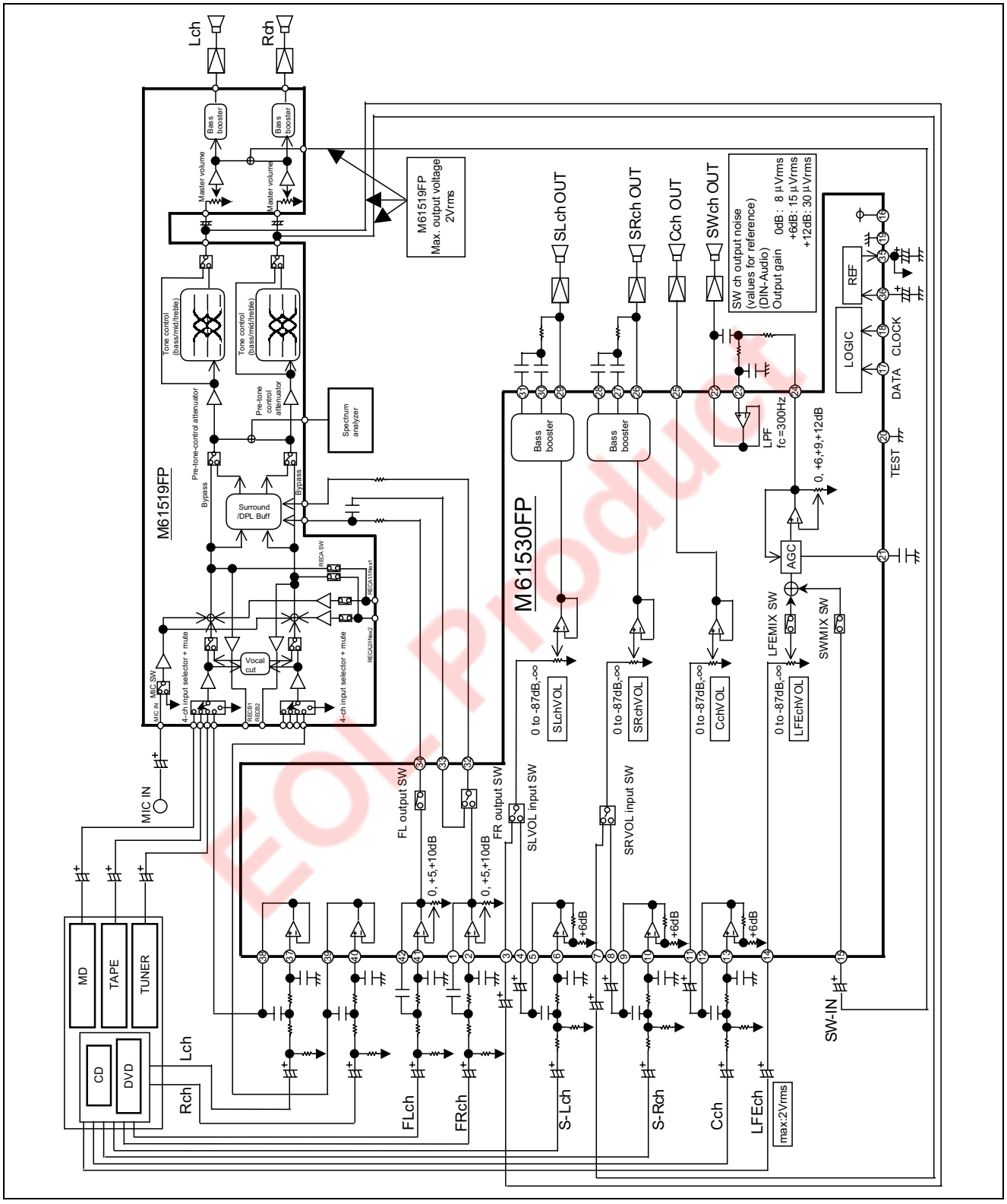
Item		Symbol	Limits Min.	Typ.	Max.	Unit	Condition
Power supply	Circuit current	IACC	—	14	25	mA	When no signal is detected, current flows to pin 16
I/O	Max. input voltage	VIM1	1.6	2.0	—	Vrms	Pins 2, 37, 40, and 41: Input, pins 1, 38, 39, and 42: Output, RL = 10 kΩ, THD = 1%
		VIM2	0.8	1.0	—	Vrms	Pins 6, 10, and 13: Input, pins 5, 9, and 12: Output, RL = 10 kΩ, THD = 1%
		VIM3	1.6	2.0	—	Vrms	Pin 14: Input, pin 22: Output, RL = 10 kΩ, THD = 5%, f = 100 kHz
	Absolute max. input voltage	AVIM	—	—	2.0 Note	Vrms	Pins 3, 7, 14, and 15: Input
	Max. output voltage	VOM1	1.8	2.4	—	Vrms	Pins 6 and 10: Input, pins 29 and 26: Output, RL = 10 kΩ, THD = 5%, bass boost = on, f = 100 Hz
		VOM2	1.6	2.0	—	Vrms	Pin 13: Input, pin 25: Output, RL = 10 kΩ, THD = 5%
		VOM3	1.4	1.8	—	Vrms	Gain between pins 14 and 22, Vi = 0.5 Vrms, FLAT, f = 100 Hz
	Bypass gain	GV1	+2.3	+4.3	+6.3	dB	Gain from pins 6 to 29, pin 10 to 26, and pins 13 to 25, Vi = 0.5 Vrms, FLAT
		GV2	-2	0	+2	dB	Gain from pins 2 to 32 and 41 to 34, Vi = 0.5 Vrms, FLAT
		GV3	-2	0	+2	dB	Gain from pin 14 to 22, Vi = 0.5 Vrms, FLAT, f = 100 Hz
	Output noise voltage	Vno1	—	6.0	12.0	µVrms	DIN-Audio, when no signal is present, Rg = 0 for pins 6 and 10, pins 29 and 26 are outputs —
			—	2.5	8.0	µVrms	SL/SR ch volume = -∞ dB
		Vno2	—	6.0	10.0	µVrms	DIN-Audio, when no signal is present, Rg = 0 for pin 13, pin 25 is an output C ch volume = 0 dB
			—	2.0	4.0	µVrms	C ch volume = -∞ dB
		Vno3	—	6.5	16.0	µVrms	DIN-Audio, when no signal is detected, Rg = 0 for pin 14, pin 22 is an output, SW ch LPF: fc=300 Hz LFE ch volume = 0 dB
			—	6.5	16.0	µVrms	LFE ch volume = -∞ dB
	Total harmonic distortion rate	THD1	—	0.003	0.2	%	Pins 6 and 10: input, pins 29 and 26: output, bandwidth: 400 Hz to 30 kHz, Vo = 0.5 Vrms, RL = 10 kΩ
		THD2	—	0.003	0.1	%	Pin 13: input, pin 25: output, bandwith: 400 Hz to 30 kHz, Vo = 0.5 Vrms, RL = 10 kΩ
		THD3	—	0.008	0.2	%	Pin 14: input, pin 22: output, 30-kHz low-pass filter, Vo = 0.5 Vrms, RL = 10 kΩ, output gain control = 0 dB, when AGC is not operating, f = 100 Hz
		THD4	—	2	—	%	Pin 14: input, pin 22: output, 30-kHz low-pass filter, RL = 10 kΩ, Vi = 700 mVrms, f = 100 Hz, when AGC is operating, output gain control = + 12 dB
	Volume max. attenuation	ATT	—	-100	-87	dB	Vo = 1 Vrms, pins 22, 25, 26, and 29 are outputs, JIS-A, volume = -∞

Item		Symbol	Limits Min.	Typ.	Max.	Unit	Condition
I/O	Max. gain	GVM1	+8	+10	+12	dB	Gain from pin 2 to 32 and 41 to 34, Vi = 0.1 Vrms, FLAT, input gain control = + 10 dB
		GVM2	+10	+12	+14	dB	Gain between pins 14 and 22, f = 100 Hz Vi = 0.1 Vrms, FLAT, output gain control = + 12 dB
	Crosstalk between channels	CT	—	-90	-55	dB	Gain from pins 6 to 29, pins 10 to 26, pins 13 to 25, and pins 14 to 22, Vi = 0.5 Vrms, JIS-A, RL = 47 kΩ, Rg = 0 Ω, input on a channel other than the measurement target
AGC	Attack time	TAGCAT	—	40	—	ms	Pin 14: input, pin 22: output, RL = 10 kΩ, output gain control = +12 dB
	Recovery time	TAGCRE	—	850	—	ms	Pin 14: input, pin 22: output, RL = 10 kΩ, output gain control = +12 dB

Note: The voltage on pins 3, 7, 14, and 15 must not exceed the the absolute maximum input-voltage range (2 Vrms).

System block diagram

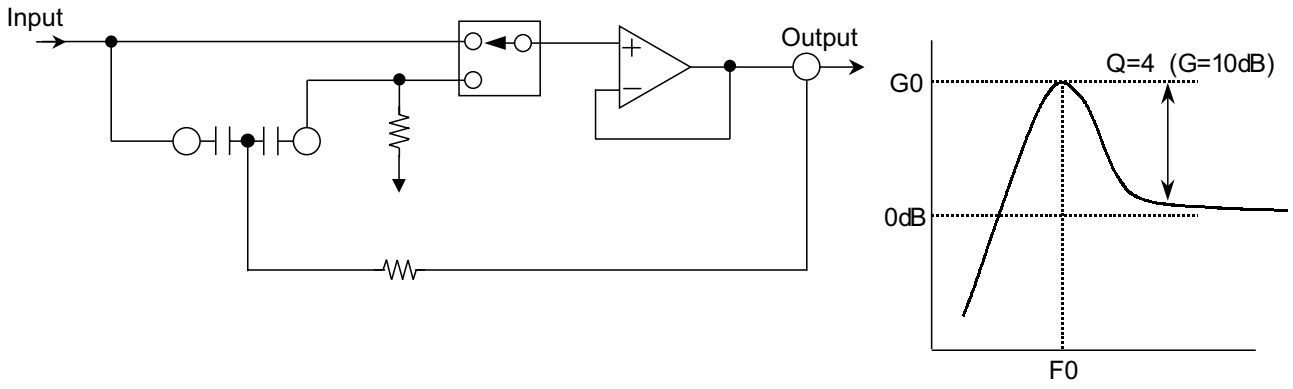
M61530FP + M61519FP application example

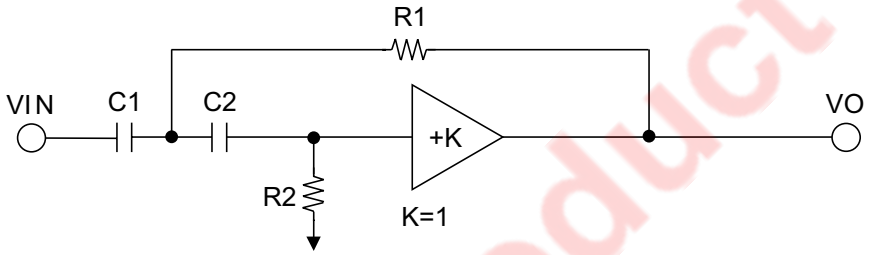


Note: In the above application, the voltage input to pin 14 (LFE ch) must not exceed the absolute maximum input voltage (2 Vrms).

Functional description

(1) Equivalent circuit of the bass-boost circuit





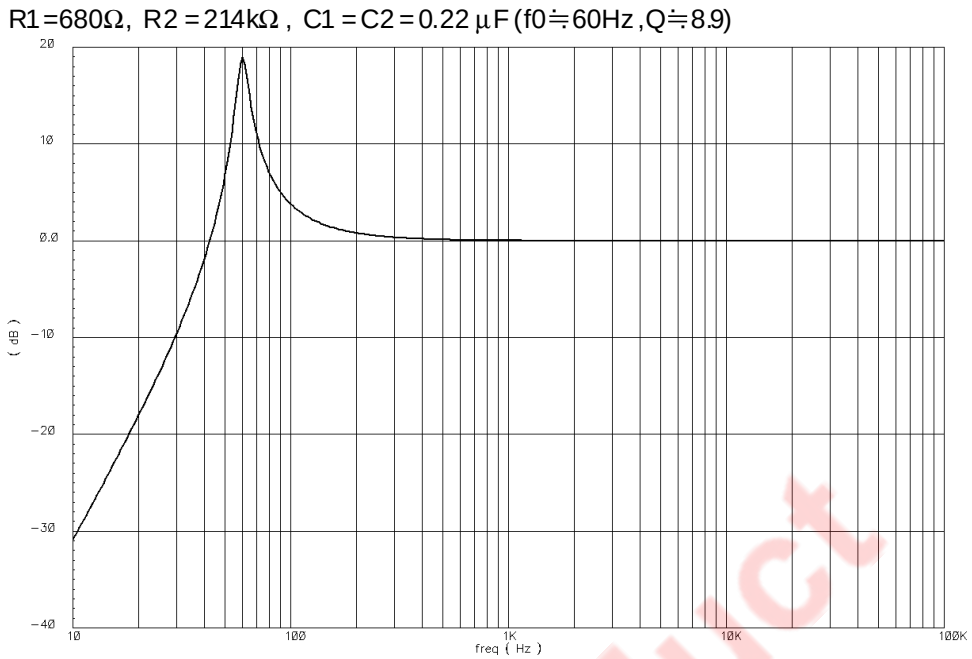
Note: Resistor R2 is within the IC. (R2≒214kΩ ± 30%)

$$fo = \frac{1}{2\pi\sqrt{R1R2C1C2}}\ Hz \qquad Q = \frac{\sqrt{R1R2C1C2}}{R1(C1+C2)+(1-K)R2C2}$$

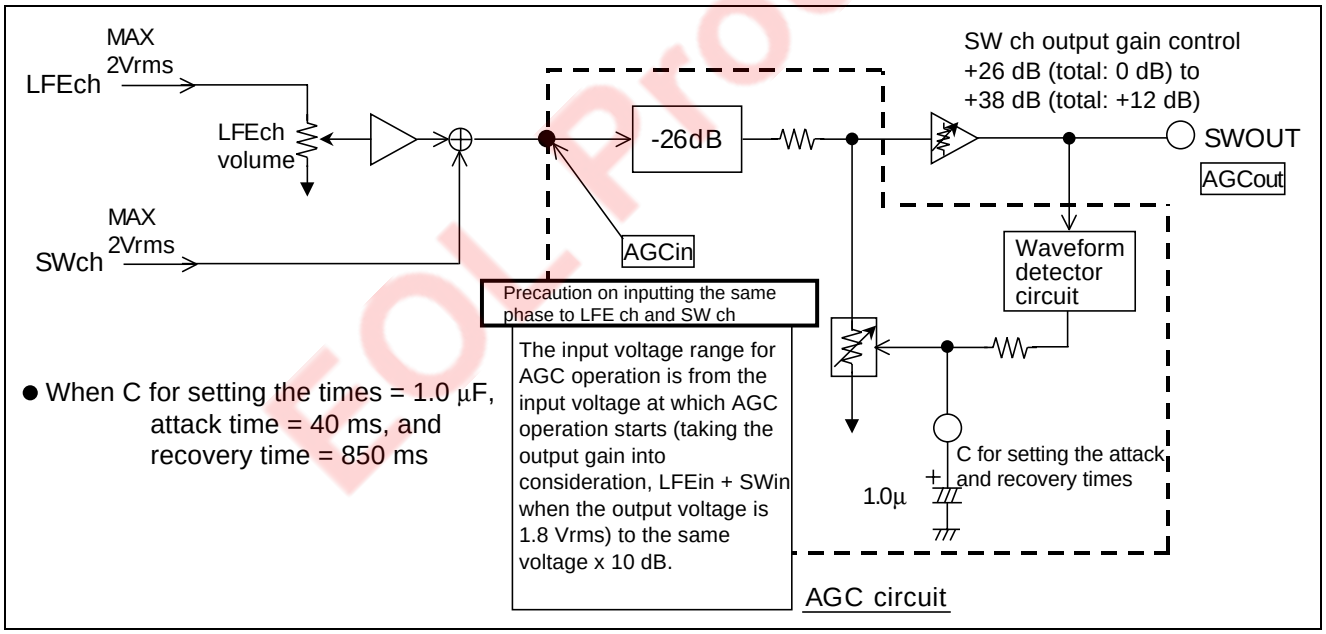
Amplitude characteristics of the second-order high-pass filter (reference)

Q	G0
1	0 to1dB
2	6dB
4	10dB
5	13dB
10	20dB

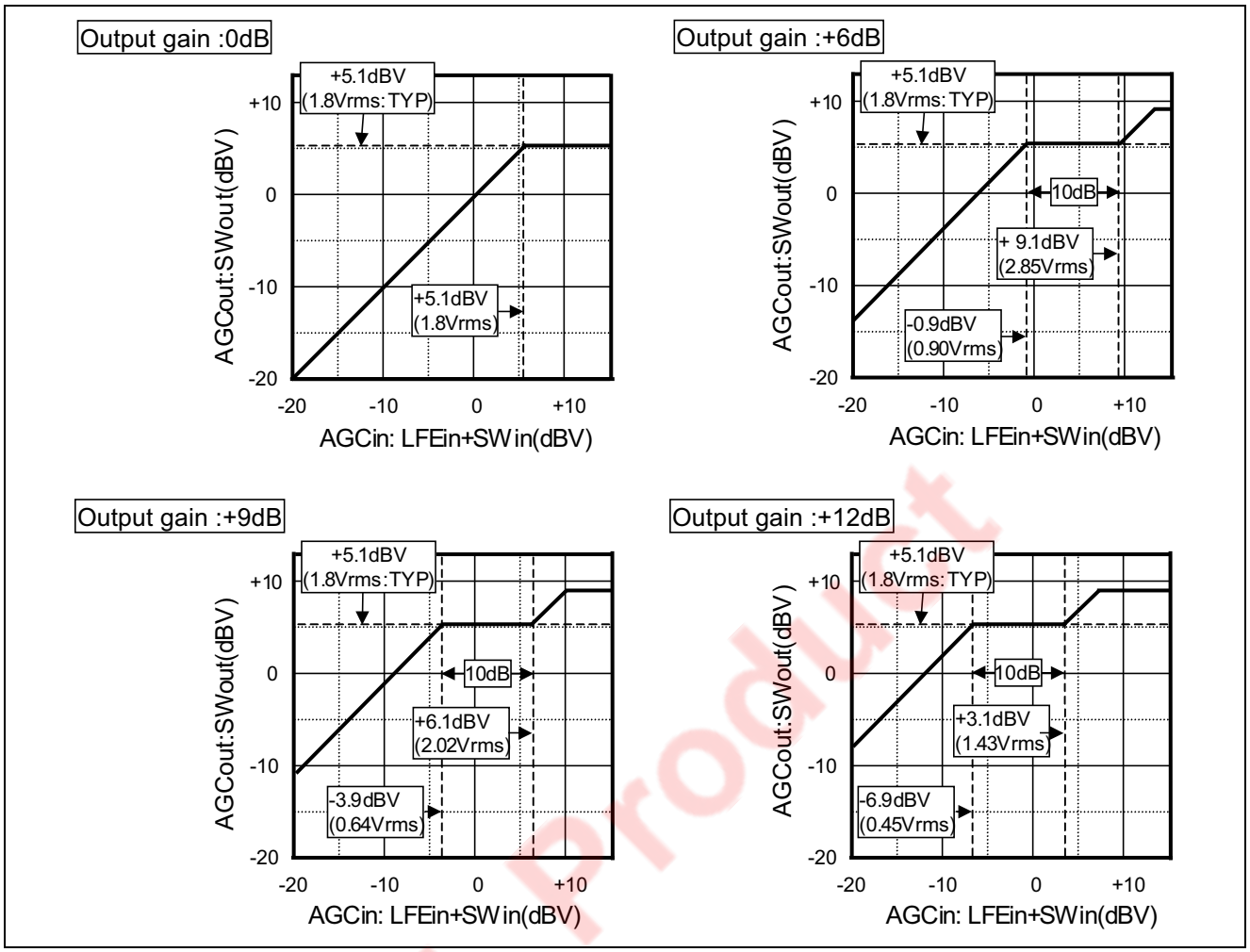
Bass-boost characteristic curve



(2) AGC circuit



Diagrams AGC input/output characteristics



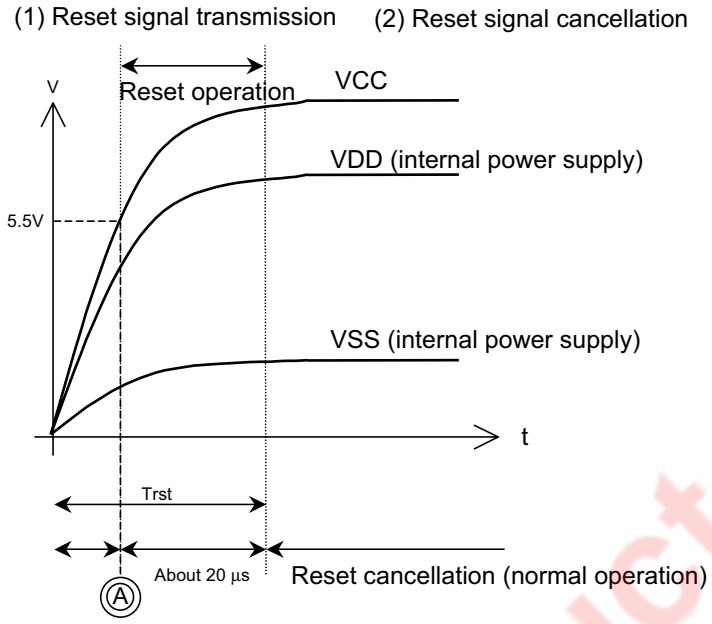
System reset

(a) Power-on operation

Immediately after power is supplied, this IC generates a reset signal.

- Generation of the reset signal is governed by the time constant for the rise in power voltage when power is supplied.
- When VCC rises above roughly 5.5 V (1), the reset signal is transmitted (logic circuit is turned on).
- (1) The reset operation takes place in the period from reset signal transmission to (2) reset signal cancellation.
- Trst = “Timing A + about 20 µs” is the time up to reset cancellation
  (Timing A is time until VCC reaches 5.5 V)

Reset timing diagram

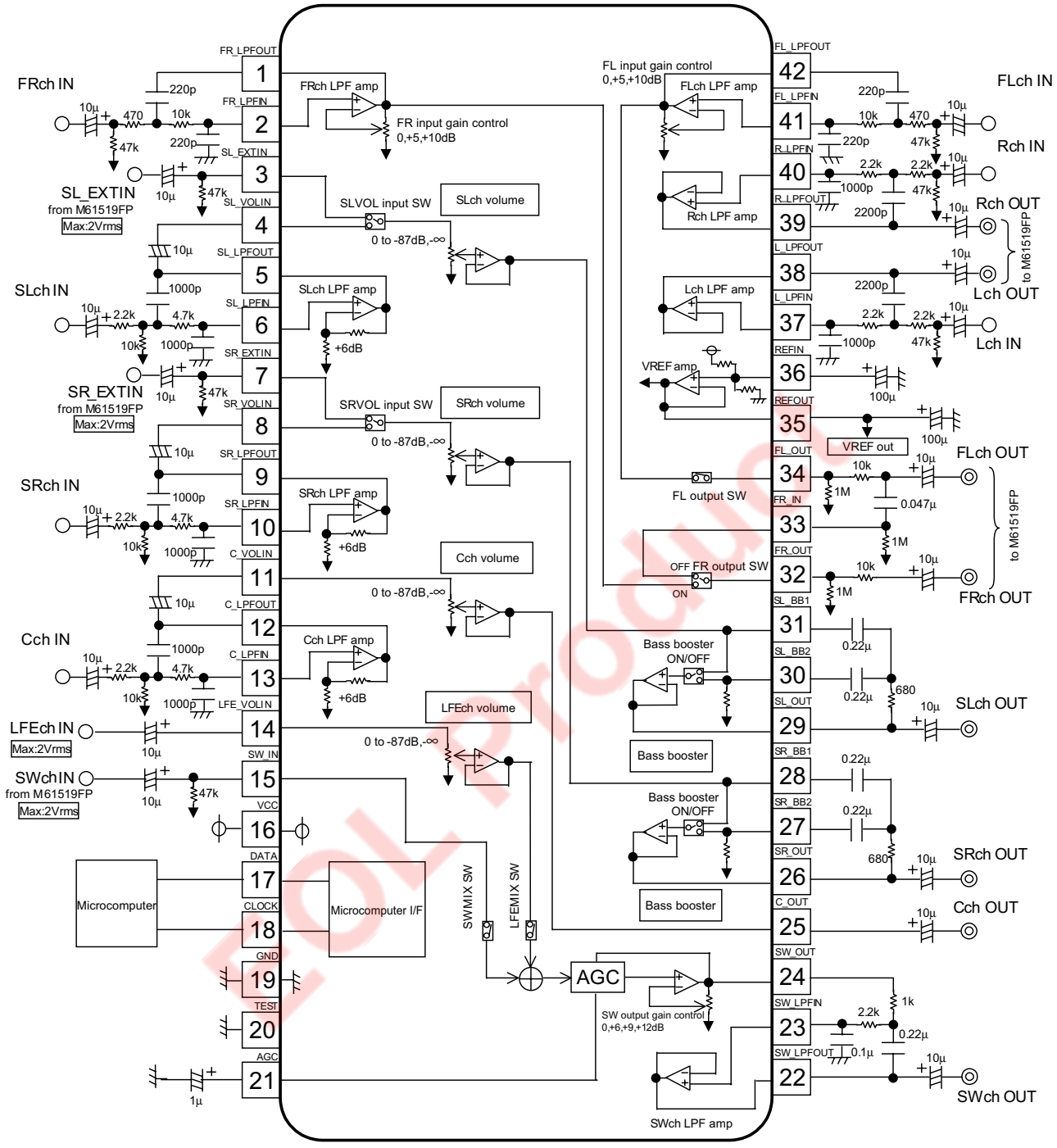


As is shown in the above figure, the reset is cancelled after time Trst after the power-supply voltage has started to rise. The chip is then able to receive serial data.

(b) Power-off operation (for reference)

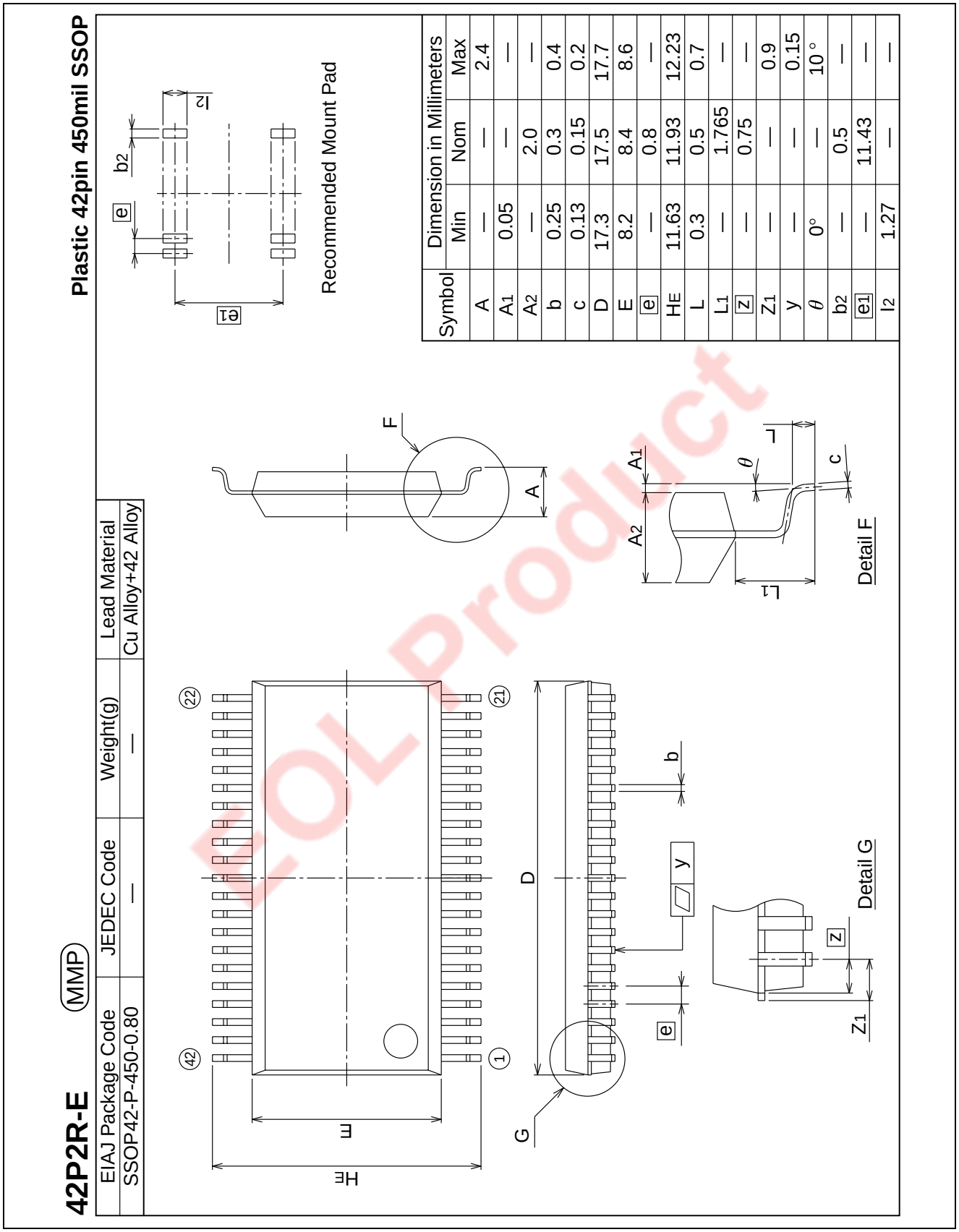
- The internal VDD and VSS voltages fall as VCC falls (the opposite trend to that in the above figure).
- When the logic circuits are turned off, all setting data becomes invalid.

Application Examle



Note: The voltage input to pins 3, 7, 14, and 15 must not exceed the absolute maximum input voltage (2 Vrms).

Package Dimensions



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