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April 1st, 2010
Renesas Electronics Corporation

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M37762M8A/MCA/MFA-XXXGP

16-BIT CMOS MICROCOMPUTER

REJ03B0057-0100Z
Rev.1.00
2003.07.25

1. DESCRIPTION

This microcomputer is a single-chip microcomputer that adopts a high-performance silicon gate CMOS process, and is contained in a 100-pin plastic mold QFP. This single-chip microcomputer is provided with an instruction queue buffer and a data buffer for executing instructions at high speed. The central processing unit runs in a 16-bit parallel processing mode but can be converted into an 8-bit parallel processing mode when necessary. This product has been designed exclusively for video equipment system controls, incorporating a time measuring circuit for VCR servo control, a real-time pattern generating circuit, analog amplifiers, an OSD display circuit, and a data slicer, among its many other peripheral capabilities.

1.1 FEATURES

- Number of basic instructions 103
- Memory size ROM ..... Refer to Figure 2.1.1 Memory Map
  RAM ..... Refer to Figure 2.1.1 Memory Map
- Instruction execution time
  (fastest instruction, 16 MHz high-speed mode) ..... 250 ns
  (fastest instruction, 12 MHz double-speed mode)
  ..... 167 ns
- Single power source
  In 16 MHz high-speed mode
  (OSD/data slicer off) ..... 4.0 V to 5.5 V
  (OSD/data slicer on) ..... 4.75 V to 5.25 V
  In 12 MHz double-speed mode
  (OSD/data slicer off) ..... 4.0 V to 5.5 V
  (OSD/data slicer on) ..... 4.75 V to 5.25 V
  In 32 kHz low-speed mode
  (OSD/data slicer off) ..... 2.6 V to 5.5 V
- OSD power source ..... 4.75 V to 5.25 V
- Interrupt ..... 23 factors, 6 levels
- 16-bit timer 3
- 8-bit timer 3
- Clock-synchronous serial I/O 2
  (one of which can perform automatic 64-byte transfers)
- I^2C-Bus interface (single master) 1
- 8-bit A-D converter.....1 unit (11 channel inputs)
- 8-bit D-A converter 2
- 12/14-bit PWM 2
- 14-bit PWM 1
- Time measurement circuit (TMT)
  One counter for measuring time to generate input signals DRFG, CPFG, CPPG, VSYNG, and GEN
  One counter for measuring time to generate input signals RLS and RLT
- Remote-control noise filter (majority of 4 samplings)
- Real-time pattern (RTP) generation circuit
  Outputs real-time pattern to exterior, RECCTL signal to CTL head control circuit, trigger for start the A-D converter, trigger for starting OSD vertical display
- Amplification circuits
  CTL head control circuit, CTL amplifier, CTL schmidt circuit, drum PG circuit, drum FG circuit, capstan FG circuit, capstan FG amplifier circuit
- Pulse duty detection circuit (VISS and VASS signal detection features embedded) Measures PBCTL signal duty ratio.
- Synchronous signal separation circuit
- EOR output feature (HASW, CROT) ..... 2-bit output
- Watchdog timer
- Programmable I/O ports 69
  (Ports $P0_0$–$P0_6$, $P1_0$, $P1_1$, $P1_5$–$P1_7$, P2, P4– P7, $P8_4$–$P8_7$, P9, P10, $P11_0$, $P11_1$)
- Input ports 10
  (Ports $P0_7$, $P1_2$–$P1_4$, $P3_0$,$P3_1$,$P8_0$–$P8_3$)
- 4 Embedded clock-generating circuits
  Built-in feed-back resistor between X_{IN}–X_{OUT}
  Built-in feed-back resistor between X_{CIN}–X_{COUT}
- CPU double-speed enable (f(X_{IN}) max. 12.0 MHz)
- ROM correction function included
- OSD function
  Display characters ..... 32 characters × 16 lines
  Kinds of characters ..... Composite Output 254 kinds
  RGB Output 285 kinds
  Kinds of character sizes ..... 8 kinds
  Output method ..... Composite video signal, RGB output (PAL, MPAL, NTSC, NPAL)
  Special function ..... Display with background shadow (button display)
  On-chip sync correct circuit (AFC)
- Data slicer
  On-chip slicer for XDS

1.2 APPLICATION

VCR, TVCR

Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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