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Renesas Electronics Corporation

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M35080FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35080FP is a bitmap pattern display control IC can display on the screen. Display frequency can operate in 3.3MHz to 20MHz, and is equipped with the analog RGB output (512 colors / 260k colors) and the digital RGB output (512 colors) function. Moreover, 2 pages (horizontal 128 dot × vertical 96 dots/page) display can be simultaneously performed on 1 screen.It uses a silicon gate CMOS process and it housed in a 24-pin shrink SOP package.

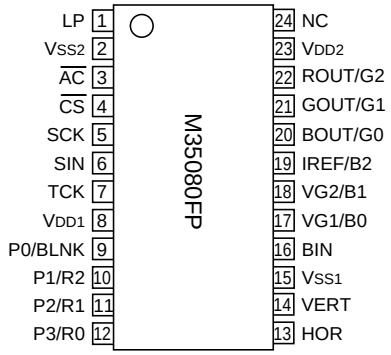
FEATURES

- Pixel composition ..... Eight kinds (Can be chosen from the following)
  - ..... horizontal 128 dots × verical 96 dots × 2 pages
  - ..... horizontal 192 dots × verical 64 dots × 2 pages
  - ..... horizontal 256 dots × verical 48 dots × 2 pages
  - ..... horizontal 384 dots × verical 32 dots × 2 pages
  - ..... horizontal 32 dots × verical 384 dots × 2 pages
  - ..... horizontal 48 dots × verical 256 dots × 2 pages
  - ..... horizontal 64 dots × verical 192 dots × 2 pages
  - ..... horizontal 96 dots × verical 128 dots × 2 pages
- RGB output .....
  - Analog RGB output ..... ROUT, GOUT,BOUT
    - Number of colors displayed .....
      - double-screen display (3 bits each of RGB) : 512 colors
      - one-screen display (6 bits each of RGB) : 260 K colors
  - Digital RGB output ..... R0 to R2, G0 to G2, B0 to B2,
    - Number of colors displayed .....
      - one and double-screen display (3 bits each of RGB) : 512 colors
- Bit map RAM ..... 1000h to 3AFFh
  - ..... 128 × 96 × 9 plans (R, G, B every 3 bit) × 2
  - ..... 221184 bit (27 Kbyte)
- Display input frequency range .....
  - ..... external input F_{OSC} = 3.3 MHz to 20 MHz
- Horizontal synchronous input frequency
  - ..... H.sync = 10 kHz to 20 kHz
- Output ports (Combination port output) .....
  - ..... 4 ports (Switches with R0, R1, R2 and BLNK output)
- DAC ..... 6 bits × 3 (R, G, B)
- Operating voltage ..... 2.7 V to 3.3 V

APPLICATION

Liquid crystal display, Plasma display, Multi-scan monitor

PIN CONFIGURATION (TOP VIEW)

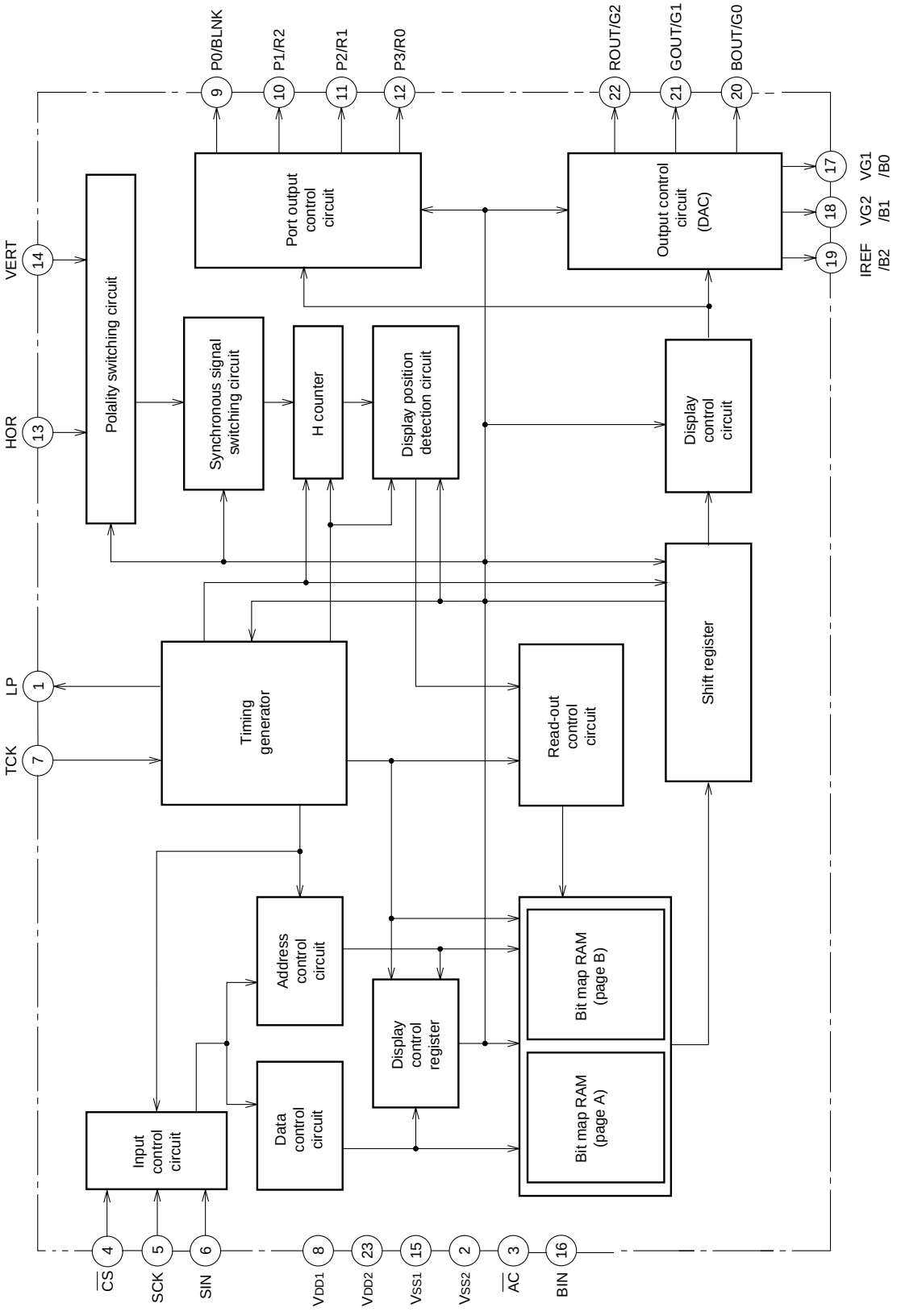


Outline 24P2Q-A

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
LP	Test output	Output	Test pin. Open this pin.
V_{SS2}	Earthing pin	–	Connect to GND.
$\overline{AC}$	Auto-clear input	Input	When “L”, this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
$\overline{CS}$	Chip select input	Input	This is the pin for chip select input. Set “L” level at serial data transmission. Hysteresis input.
SCK	Serial clock input	Input	At $\overline{CS}$ pin is “L” level, SDA pin serial data is taken in when SCL rises. Hysteresis input. Built-in pull-up resistor.
SIN	Serial data input	Input	This is the pin for serial input of display control register and display RAM data. Also, this pin output acknowledge signal. Hysteresis input. Nch open-drain output.
TCK	External clock	Input	This is the pin for external clock input.
V_{DD1}	Power pin	–	Digital power supply. Connect to +3V with the power pin.
P0/BLNK	Port P0 output	Output	This is a general purpose port output at analog RGB output. Outputs port output or BLNK signal.
	BLNK		Outputs BLNK signal at digital RGB output.
P1/R2	Port P1 output	Output	This is the output port output at analog RGB output.
	R2		Outputs R2 signal at digital RGB output.
P2/R1	Port P2 output	Output	This is the output port output at analog RGB output.
	R1		Outputs R1 signal at digital RGB output.
P3/R0	Port P3 output	Output	This is the output port output at analog RGB output.
	R0		Outputs R0 signal at digital RGB output.
HOR	Horizontal synchro-nous signal input	Input	Input horizontal synchronous signal. (Hysteresis input.)
VERT	Vertical synchro-nous signal input	Input	Input vertical synchronous signal. (Hysteresis input.)
V_{SS1}	Earthing pin	–	Connect to GND.
BIN	Test pin	–	Test pin. Connect to GND.
VG1/B0	Reference voltage output 1	Output	Use reference voltage output 1 of DAC for analog RGB output at analog RGB output. Connect to capacitor.
	B0		Output B0 signal at digital RGB output.
VG2/B1	Reference voltage output 1	Output	Use reference voltage output 2 of DAC for analog RGB output at analog RGB output. Connect to capacitor.
	B1		Output B1 signal at digital RGB output.
IREF/B2	Reference voltage output 2	Output	The pin connects resistors which convert voltage current at analog RGB output.
	B2		Output B2 signal at digital RGB output.
BOUT/G0	Analog B signal output	Output	Output analog B signal at analog RGB output(Current output). Connect to load resistance.
	G0		Output G0 signal at digital RGB output.
GOUT/G1	Analog G signal output	Output	Output analog G signal at analog RGB output(Current output). Connect to load resistance.
	G1		Output G1 signal at digital RGB output.
ROUT/G2	Analog R signal output	Output	Output analog R signal at analog RGB output(Current output). Connect to load resistance.
	G2		Output G2 signal at digital RGB output.
V_{DD2}	Power pin	–	Digital power supply. Connect to +3V with the power pin.
NC	NC	–	NC pin. Open.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 0000_{16} to 0007_{16} are assigned to the display RAM, address 1000_{16} to $3AFF_{16}$ are assigned to bitmap RAM. The internal circuit is reset and all display control registers (address 0000_{16} to 0007_{16}) are set to "0" when the AC pin level is "L". And then, bit map RAM is not erased and be undefinited. This memory has 2-page composition (an address is Page A and page B community) of the memory for page A, and the memory for page B. Registers PAGEONA and PAGEONB perform page control at the time of writing in data. For detail, refer to "DATA INPUT EXAMPLE". Memory constitution is shown in Figure 1 to 10.

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0000_{16}	–	–	–	–	–	–	–	–	–	–	–	–	–	–	PAGEONB	PAGEONA
0001_{16}	–	–	–	–	–	YM2	YM1	YM0	BLANK1	BLANK0	ALLON	DSPON	–	WIDTH2	WIDTH1	WIDTH0
0002_{16}	–	VSIZE1	VSIZE0	–	–	–	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
0003_{16}	–	–	–	–	–	–	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
0004_{16}	–	ANADIG2	ANADIG1	ANADIG0	SYNCCK	TEST	–	–	–	–	–	POLV	POLH	MODE2	MODE1	MODE0
0005_{16}	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
0006_{16}	–	DACON	–	–	–	–	–	–	–	–	–	–	–	–	–	–
0007_{16}	–	–	–	–	–	–	–	–	SBLANK3	SBLANK2	SBLANK1	SBLANK0	PTD3	PTD2	PTD1	PTD0

Fig.1 Memory constitution (Display Control register)

Note : Address 0000_{16} and 0004_{16} to 0007_{16} are Page A and B common registers. The writing of data is made regardless of registers PAGEONA and PAGEONB. As for addresses 0001_{16} to 0003_{16}, register of Page A and Page B exists for every page (common to an address.)
When write data in the memory for page A, and write data in the memory for page B, set it as register PAGEONA = “1” at register PAGEONB = “1.”
When both of PAGEONA and PAGEONB are set to “1”, data can be simultaneously written in both the memory for page A, and the memory for page B.
Address $0XXX_{16}$ other than addresses 0000_{16} to 0007_{16} are write-protected.

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
1000_{16}	Bit map RAM (R0) data																Dot 1 to 16 of line 1
1001_{16}																	Dot 17 to 32 of line 1
1002_{16}																	Dot 33 to 48 of line 1
1003_{16}																	Dot 49 to 64 of line 1
1004_{16}																	Dot 65 to 80 of line 1
1005_{16}																	Dot 81 to 96 of line 1
1006_{16}																	Dot 97 to 112 of line 1
1007_{16}																	Dot 113 to 128 of line 1
1008_{16}																	Dot 1 to 16 of line 2
1009_{16}																	Dot 17 to 32 of line 2
$100A_{16}$																	Dot 33 to 48 of line 2
⋮																	⋮
1206_{16}																	Dot 81 to 96 of line 95
1207_{16}																	Dot 97 to 112 of line 95
1208_{16}																	Dot 113 to 128 of line 95
$12F9_{16}$																	Dot 1 to 16 of line 96
$12FA_{16}$																	Dot 17 to 32 of line 96
$12FB_{16}$																	Dot 33 to 48 of line 96
$12FC_{16}$																	Dot 49 to 64 of line 96
$12FD_{16}$																	Dot 65 to 80 of line 96
$12FE_{16}$																	Dot 81 to 96 of line 96
$12FF_{16}$																	Dot 97 to 112 of line 96
1300_{16} ⋮ $13FF_{16}$	unused area																—

Fig.2 Memory constitution (Bit map RAM (R0))

Notes : Bit map RAM (Addresses 1000_{16} to $3AFF_{16}$) has 2-page composition of the memory for page A, and the memory for page B.
When write data in the memory for page A, and write data in the memory for page B, set it as register PAGEONA = "1" at register PAGEONB = "1."
When both of PAGEONA and PAGEONB are set to "1", data can be simultaneously written in both the memory for page A, and the memory for page B.

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
1400_{16}	Bit map RAM (R1) data																Dot 1 to 16 of line 1
1401_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$16FE_{16}$																	Dot 81 to 96 of line 96
$16FF_{16}$																	Dot 97 to 112 of line 96
1700_{16} ⋮ $17FF_{16}$	unused area																—

Fig.3 Memory constitution (Bit map RAM (R1))

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
1800_{16}	Bit map RAM (R2) data																Dot 1 to 16 of line 1
1801_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$1AFE_{16}$																	Dot 81 to 96 of line 96
$1AFF_{16}$																	Dot 97 to 112 of line 96
$1B00_{16}$ ⋮ $1FFF_{16}$	unused area																—

Fig.4 Memory constitution (Bit map RAM (R2))

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
2000_{16}	Bit map RAM (G0) data																Dot 1 to 16 of line 1
2001_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$22FE_{16}$																	Dot 81 to 96 of line 96
$22FF_{16}$																	Dot 97 to 112 of line 96
2300_{16} ⋮ $23FF_{16}$	unused area																—

Fig.5 Memory constitution (Bit map RAM (G0))

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
2400_{16}	Bit map RAM (G1) data																Dot 1 to 16 of line 1
2401_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$26FE_{16}$																	Dot 81 to 96 of line 96
$26FF_{16}$																	Dot 97 to 112 of line 96
2700_{16} ⋮ $27FF_{16}$	unused area																—

Fig.6 Memory constitution (Bit map RAM (G1))

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
2800_{16}	Bit map RAM (G2) data																Dot 1 to 16 of line 1
2801_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$2AFE_{16}$																	Dot 81 to 96 of line 96
$2AFF_{16}$																	Dot 97 to 112 of line 96
$2B00_{16}$ ⋮ $2FFF_{16}$	unused area																

Fig.7 Memory constitution (Bit map RAM (G2))

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
3000_{16}	Bit map RAM (B0) data																Dot 1 to 16 of line 1
3001_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$32FE_{16}$																	Dot 81 to 96 of line 96
$32FF_{16}$																	Dot 97 to 112 of line 96
3300_{16} ⋮ $33FF_{16}$	unused area																—

Fig.8 Memory constitution (Bit map RAM (B0))

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
3400_{16}	Bit map RAM (B1) data																Dot 1 to 16 of line 1
3401_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$36FE_{16}$																	Dot 81 to 96 of line 96
$36FF_{16}$																	Dot 97 to 112 of line 96
3700_{16} ⋮ $37FF_{16}$	unused area																—

Fig.9 Memory constitution (Bit map RAM (B1))

Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Dot composition (DAF to DA0) at 128 dots × 96 dots
3800_{16}	Bit map RAM (B2) data																Dot 1 to 16 of line 1
3801_{16}																	Dot 17 to 32 of line 1
⋮																	⋮
$3AFE_{16}$																	Dot 81 to 96 of line 96
$3AFF_{16}$																	Dot 97 to 112 of line 96
$3B00_{16}$ ⋮ $3FFF_{16}$	unused area																—

Fig.10 Memory constitution (Bit map RAM (B2))

Pixel composition

Each bit of a bit map display consists of nine bit map RAM (R0 to R2, G0 to G2, and B0 to B2.) Color setup can be specified out of 512 kinds per dot. The bit map RAM address corresponding to dot composition in case pixel composition is 128 dot x 96 dot is shown in Fig. 11. And, the bit map RAM address corresponding to dot composition in case pixel composition is 64 dot x192 dot is shown in Fig. 12. In other pixel composition, the bit map RAM is similarly assigned in an order from the dots 1 to 16 of line 1.

Lines \ Dots	1 to 16	17 to 32	33 to 48	49 to 64	65 to 80	81 to 96	97 to 112	113 to 128
1	000_{16}	001_{16}	002_{16}	003_{16}	004_{16}	005_{16}	006_{16}	007_{16}
2	008_{16}	009_{16}	$00A_{16}$	$00B_{16}$	$00C_{16}$	$00D_{16}$	$00E_{16}$	$00F_{16}$
3	010_{16}	011_{16}	012_{16}	013_{16}	014_{16}	015_{16}	016_{16}	017_{16}
4	018_{16}	019_{16}	$01A_{16}$	$01B_{16}$	$01C_{16}$	$01D_{16}$	$01E_{16}$	$01F_{16}$
5	020_{16}	021_{16}	022_{16}	023_{16}	024_{16}	025_{16}	026_{16}	027_{16}
6	028_{16}	029_{16}	$02A_{16}$	$02B_{16}$	$02C_{16}$	$02D_{16}$	$02E_{16}$	$02F_{16}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
91	$2D0_{16}$	$2D1_{16}$	$2D2_{16}$	$2D3_{16}$	$2D4_{16}$	$2D5_{16}$	$2D6_{16}$	$2D7_{16}$
92	$2D8_{16}$	$2D9_{16}$	$2DA_{16}$	$2DB_{16}$	$2DC_{16}$	$2DD_{16}$	$2DE_{16}$	$2DF_{16}$
93	$2E0_{16}$	$2E2_{E6}$	$2E2_{16}$	$2E3_{16}$	$2E4_{16}$	$2E5_{16}$	$2E6_{16}$	$2E7_{16}$
94	$2E8_{16}$	$2E9_{16}$	$2EA_{16}$	$2EB_{16}$	$2EC_{16}$	$2ED_{16}$	$2EE_{16}$	$2EF_{16}$
95	$2F0_{16}$	$2F1_{16}$	$2F2_{16}$	$2F3_{16}$	$2F4_{16}$	$2F5_{16}$	$2F6_{16}$	$2F7_{16}$
96	$2F8_{16}$	$2F9_{16}$	$2FA_{16}$	$2FB_{16}$	$2FC_{16}$	$2FD_{16}$	$2FE_{16}$	$2FF_{16}$

* The numerical value in a thick frame corresponds to lower 10-bits of bit map RAM (R0 to R2, G0 to G2, B0 to B2) address. (n RAM character number : 0 to 7)
Dot composition in 1 address (16 bits) is MSB.....LSB

Fig.11 Pixel composition (at 128 dots × 96 dots)

Lines \ Dots	1 to 16	17 to 32	33 to 48	49 to 64
1	000_{16}	001_{16}	002_{16}	003_{16}
2	004_{16}	005_{16}	006_{16}	007_{16}
3	008_{16}	009_{16}	$00A_{16}$	$00B_{16}$
4	$00C_{16}$	$00D_{16}$	$00E_{16}$	$00F_{16}$
5	010_{16}	011_{16}	012_{16}	013_{16}
6	014_{16}	015_{16}	016_{16}	017_{16}
⋮	⋮	⋮	⋮	⋮
187	$2E8_{16}$	$2E9_{16}$	$2EA_{16}$	$2EB_{16}$
188	$2EC_{16}$	$2ED_{16}$	$2EE_{16}$	$2EF_{16}$
189	$2F0_{16}$	$2F1_{16}$	$2F2_{16}$	$2F3_{16}$
190	$2F4_{16}$	$2F5_{16}$	$2F6_{16}$	$2F7_{16}$
191	$2F8_{16}$	$2F9_{16}$	$2FA_{16}$	$2FB_{16}$
192	$2FC_{16}$	$2FD_{16}$	$2FE_{16}$	$2FF_{16}$

* The numerical value in a thick frame corresponds to lower 10-bits of bit map RAM (R0 to R2, G0 to G2, B0 to B2) address. (n RAM character number : 0 to 7)
Dot composition in 1 address (16 bits) is MSB.....LSB

Fig.12 Pixel composition (at 64 dots × 192 dots)

Register

Address 000016

DA	Register	Contents		Remarks
		Status	Function	
0	PAGEONA	⓪	Writing to the memory(display control registers and Bit map RAM) for page A is disapproval.	Memory writing control for page A.
		1	Writing to the memory(display control registers and Bit map RAM) for page A is permission.	
1	PAGEONB	⓪	Writing to the memory(display control registers and Bit map RAM) for page B is disapproval.	Memory writing control for page B.
		1	Writing to the memory(display control registers and Bit map RAM) for page B is permission.	
2	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
3	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
4	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
5	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
6	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
7	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
8	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
9	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
A	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
B	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
C	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
D	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
E	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
F	–	⓪	Set "0" to this bit.	
		1	Can not be used.	

Address 000116

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td rowspan="2">WIDTH0</td><td>⓪</td><td rowspan="8"><table><tr><th>WIDTH2</th><th>WIDTH1</th><th>WIDTH0</th><th>Pixel (Horizontal × Vertical)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>128 × 96 dots</td></tr><tr><td>0</td><td>0</td><td>1</td><td>192 × 64 dots</td></tr><tr><td>0</td><td>1</td><td>0</td><td>256 × 48 dots</td></tr><tr><td>0</td><td>1</td><td>1</td><td>384 × 32 dots</td></tr><tr><td>1</td><td>0</td><td>0</td><td>32 × 384 dots</td></tr><tr><td>1</td><td>0</td><td>1</td><td>48 × 256 dots</td></tr><tr><td>1</td><td>1</td><td>0</td><td>64 × 192 dots</td></tr><tr><td>1</td><td>1</td><td>1</td><td>96 × 128 dots</td></tr></table></td><td rowspan="8">Set the pixel composition.

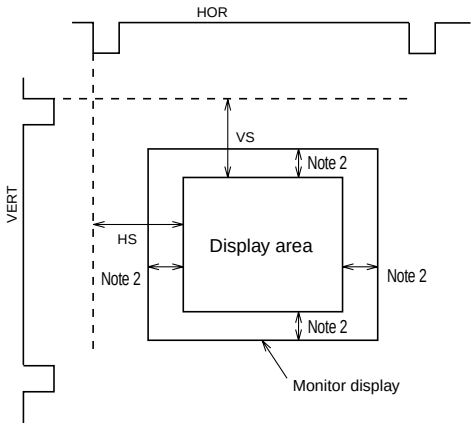
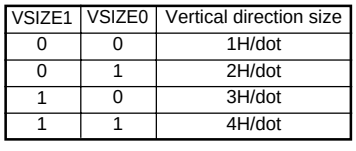
The BLNK signal of the range set up by this register is outputted at the time of BLANK1, 0 = 0, and 0 (normal) setup.</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>1</td><td rowspan="2">WIDTH1</td><td>⓪</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td rowspan="2">WIDTH2</td><td>⓪</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>3</td><td rowspan="2">–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>4</td><td rowspan="2">DSPON</td><td>⓪</td><td>Display OFF</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td>5</td><td rowspan="2">–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2">The measure against a character bend (test bit)</td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>6</td><td rowspan="2">BLANK0</td><td>⓪</td><td rowspan="4"><table><tr><th>BLANK1</th><th>BLANK0</th><th>Blank signal</th></tr><tr><td>0</td><td>0</td><td>Normal(Control by register WIDTH 0 to 2)</td></tr><tr><td>0</td><td>1</td><td>Control by Bit map RAM(R0)</td></tr><tr><td>1</td><td>0</td><td>Control by Bit map RAM(G0)</td></tr><tr><td>1</td><td>1</td><td>Control by Bit map RAM(B0)</td></tr></table></td><td rowspan="4">Control of blank signal.
(a blank setup in a bit unit is possible).
Note 2</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>7</td><td rowspan="2">BLANK1</td><td>⓪</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>8</td><td rowspan="2">YM0</td><td>⓪</td><td rowspan="6">$R = \sum_{n=0}^{2} 2^n R_n - \sum_{n=0}^{2} 2^n YM_n$

when set to R < 0, R = 0.

Same as G output and B output.</td><td rowspan="6">Control of R, G and B output luminosity</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>9</td><td rowspan="2">YM1</td><td>⓪</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>A</td><td rowspan="2">YM2</td><td>⓪</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>B</td><td rowspan="2">–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>C</td><td rowspan="2">–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>D</td><td rowspan="2">–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>E</td><td rowspan="2">–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
<tr><td>F</td><td rowspan="2">–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Can not be used.</td></tr>
</table>

Notes 1 : This register is consisted of 2 pages (address community) of the register for page A, and the register for page B.
Writing control to each page is performed by registers PAGEONA and PAGEONB (address 000016).
2 : The bit map RAM used for blank signal control is not applicable to color setup.

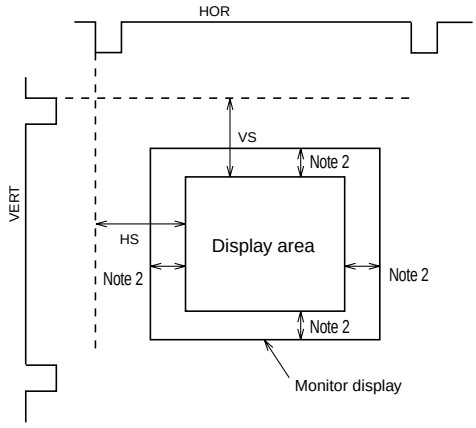
Address 0002_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	VP0	⓪	If VS is the vertical display start location, $VS = H \times \sum_{n=0}^{9} 2^n VP_n$ H: Cycle with the horizonal synchronizing pulse  	Setting vertical start location
		1		
1	VP1	⓪		
		1		
2	VP2	⓪		
		1		
3	VP3	⓪		
		1		
4	VP4	⓪		
		1		
5	VP5	⓪		
		1		
6	VP6	⓪		
		1		
7	VP7	⓪		
		1		
8	VP8	⓪		
		1		
9	VP9	⓪		
		1		
A	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
B	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
C	VSIZE0	⓪	 H : Synchronous of horizontal direction pulse	Setting vertical direction dot size
		1		
D	VSIZE1	⓪		
		1		
E	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
F	–	⓪	It should be fixed to "0".	
		1	Can not be used.	

Notes 1 : This register is consisted of 2 pages (address community) of the register for page A, and the register for page B. Writing control to each page is performed by registers PAGEONA and PAGEONB (address 0000_{16}).

2 : Set up the horizontal and vertical display start location so that display range may not exceed it. Set the character code "$1FF_{16}$" (blank without background) for the display RAM of the part which the display range exceeds.

Address 0003_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	HP0	⓪	If HS is the horizontal display start location, $HS = T \times \sum_{n=0}^{9} 2^n HP_n$ T: Display clock  	Setting horizontal start location
		1		
1	HP1	⓪		
		1		
2	HP2	⓪		
		1		
3	HP3	⓪		
		1		
4	HP4	⓪		
		1		
5	HP5	⓪		
		1		
6	HP6	⓪		
		1		
7	HP7	⓪		
		1		
8	HP8	⓪		
		1		
9	HP9	⓪		
		1		
A	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
B	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
C	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
D	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
E	–	⓪	It should be fixed to "0".	
		1	Can not be used.	
F	–	⓪	It should be fixed to "0".	
		1	Can not be used.	

Notes 1 : This register is consisted of 2 pages (address community) of the register for page A, and the register for page B. Writing control to each page is performed by registers PAGEONA and PAGEONB (address 0000_{16}).

2 : Set up the horizontal and vertical display start location so that display range may not exceed it.
Set the character code "$1FF_{16}$" (blank without background) for the display RAM of the part which the display range exceeds.

Address 000416

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>MODE0</td><td>⓪</td><td rowspan="2"><table><tr><th>MODE1</th><th>MODE0</th><th>Display mode</th></tr><tr><td>0</td><td>0</td><td>Priority is given to Page A</td></tr><tr><td>0</td><td>1</td><td>Priority is given to Page B</td></tr><tr><td>1</td><td>0</td><td>260 K colors display</td></tr><tr><td>1</td><td>1</td><td>The average of Page A and Page B</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>1</td><td>MODE1</td><td>⓪</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>2</td><td>–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>3</td><td>POLH</td><td>⓪</td><td>HOR pin is negative polarity</td><td rowspan="2">Polarity of HOR pin</td></tr>
<tr><td></td><td></td><td>1</td><td>HOR pin is positive polarity</td></tr>
<tr><td>4</td><td>POLV</td><td>⓪</td><td>VERT pin is negative polarity</td><td rowspan="2">Polarity of VERT pin</td></tr>
<tr><td></td><td></td><td>1</td><td>VERT pin is positive polarity</td></tr>
<tr><td>5</td><td>–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>6</td><td>–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>7</td><td>–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>8</td><td>–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>9</td><td>–</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>A</td><td>TEST</td><td>⓪</td><td>Set "0" to this bit.</td><td rowspan="2">Test bit</td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>B</td><td>SBLANK0</td><td>⓪</td><td>It synchronizes with a display CK rising and is port output (at the time of digital output setup).</td><td rowspan="2">BLNK signal output timing control (BLNK signal). Effective at the time of SBLANK1, 2 = 1, and 1 (BLNK output) setup.</td></tr>
<tr><td></td><td></td><td>1</td><td>It synchronizes with a display CK falling and is port output (at the time of analog output setup).</td></tr>
<tr><td>C</td><td>SBLANK1</td><td>0</td><td rowspan="2"><table><tr><th>SBLANK1</th><th>SBLANK2</th><th>P0/BLNK pin output</th></tr><tr><td>0</td><td>0</td><td>Port P0 output</td></tr><tr><td>0</td><td>1</td><td>Can not be used</td></tr><tr><td>1</td><td>0</td><td>Can not be used</td></tr><tr><td>1</td><td>1</td><td>BLNK output</td></tr></table></td><td rowspan="2">P0/BLNK pin output control.
SBLANK2 : address 000716</td></tr>
<tr><td></td><td></td><td>①</td></tr>
<tr><td>D</td><td>PTC13</td><td>0</td><td>Port P1 to P3 output (at the time of analog RGB output setup "L" fixation)</td><td rowspan="2">P1 to P3 output control</td></tr>
<tr><td></td><td></td><td>①</td><td>R0 to R2 output (at the time of digital RGB output setup "H" fixation)</td></tr>
<tr><td>E</td><td>–</td><td>0</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>①</td><td>Can not be used.</td></tr>
<tr><td>F</td><td>–</td><td>0</td><td>Set "0" to this bit.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>①</td><td>Can not be used.</td></tr>
</table>

Address 000516

DA	Register	Contents		Remarks
		Status	Function	
0	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
1	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
2	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
3	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
4	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
5	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
6	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
7	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
8	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
9	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
A	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
B	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
C	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
D	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
E	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
F	–	⓪	Set "0" to this bit.	
		1	Can not be used.	

Address 000616

DA	Register	Contents		Remarks
		Status	Function	
0	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
1	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
2	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
3	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
4	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
5	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
6	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
7	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
8	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
9	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
A	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
B	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
C	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
D	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
E	DACON	⓪	DAC OFF (at the time of digital RGB output setup "L" fixation) Digital RGB output mode (G0 to G2, B0 to B2 signal output)	DAC ON/OFF, and digital RGB/analog RGB output change
		1	DAC ON (at the time of analog RGB output setup "H" fixation). Analog RGB output mode (VG1, VG2, IREF, ROUT, GOUT, and BOUT signal output)	
F	–	⓪	Set "0" to this bit.	
		1	Can not be used.	

Address 000716

DA	Register	Contents		Remarks
		Status	Function	
0	PTD0	⓪	"L" fixation at port output, negative polarity at BLNK output.	Data control of P0 pin
		1	"H" fixation at port output, positive polarity at BLNK output.	
1	PTD1	⓪	"L" fixation at port output.	Data control of P1 pin
		1	"H" fixation at port output.	
2	PTD2	⓪	"L" fixation at port output.	Data control of P2 pin
		1	"H" fixation at port output.	
3	PTD3	⓪	"L" fixation at port output.	Data control of P3 pin
		1	"H" fixation at port output.	
4	SBLANK2	⓪	Refer to SBLANK1(000416).	Output control of P0/BLNK pin
		1		
5	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
6	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
7	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
8	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
9	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
A	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
B	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
C	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
D	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
E	–	⓪	Set "0" to this bit.	
		1	Can not be used.	
F	–	⓪	Set "0" to this bit.	
		1	Can not be used.	

DISPLAY FORM

M35080FP can display two pages, Page A and Page B, simultaneously, as shown in Figure 13.
And,1 page of 260K color display can be displayed by piling up two pages completely.

(Page A: register PAGEONA (address 0000_{16}) Set up by = "1."
Page B: register PAGEONB (address 0000_{16}) Set up by = "1.")

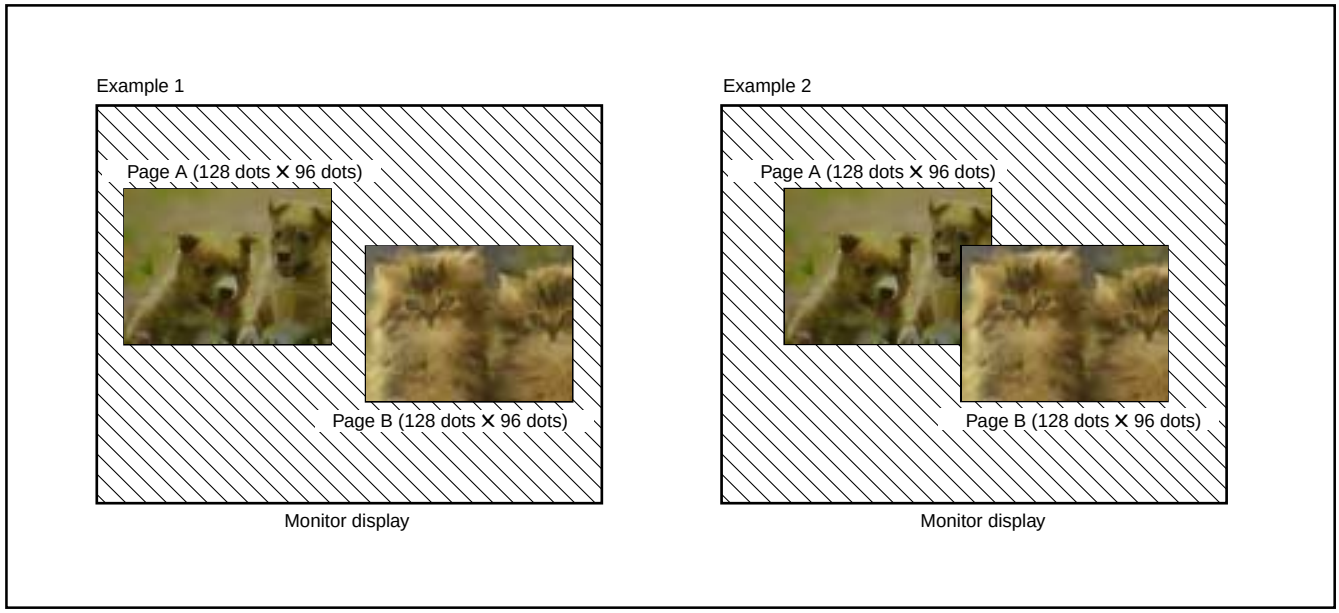


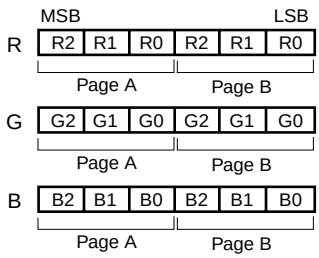
Fig. 13 The example of a display at the time of a 2-page display

Notes 1: Setup of display position, display size, etc. can be freely performed for every page. Two pages can be displayed side by side vertically and horizon tally.
2: when the display area of two pages overlaps on the monitoring screen, registers MODE0 and MODE1 (address 0004_{16}) can perform four displays as follows.

MODE1	MODE0	Display mode	Display number of pages
0	0	Priority is given to Page A	2 pages
0	1	Priority is given to Page B	2 pages
1	0	260 K colors display(Note 1)	1 page
1	1	The average of Page A and Page B	2 pages

(1) Priority is given to Page A ..... The overlaped part gives priority to Page A, and Page B is not displayed.
(2) Priority is given to Page B ..... The overlaped part gives priority to Page B, and Page A is not displayed.
(3) 260 K colors display ..... By overlaping two pages completely, 1 page of 260K color is displayed. RGB output is 6-bit(Note 2)each setup.
(4) The average of Page A and Page B ... The overlaped part averages and outputs the RGB output of two pages.

Notes 1. It becomes 512 color displays at the time of digital RGB output setup.
2. Assignment of 6 bits each of RGB is as follows.



DATA INPUT EXAMPLE

Data of Bit map RAM and display control registers can be set by the 16-bit serial input function. Example of data setting is shown in Figure 14.

Address/Data	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks
Address 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
Data 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	Page A and B writing setting (Note 1)
Data 0001_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Page A and B display OFF
Address 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
Data 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Page A writing setting
Data 0002_{16}	0	VSIZE1	VSIZE0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Page A: Vertical display location setting
Data 0003_{16}	0	0	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Page A: Horizontal display location setting
Data 0004_{16}	0	0	0	0	0	0	0	0	0	0	0	POLV	POLH	MODE2	MODE1	MODE0	Display form setting
Data 0005_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
Data 0006_{16}	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC setting
Data 0007_{16}	0	0	0	0	0	0	0	0	SBLANK	3	SBLANK	2	SBLANK	1	SBLANK	0 PTD3	Port output setting
Address 1000_{16}	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
Data 1000_{16}	Bit map RAM (Page A) (R0,R1,R2,G0,G1,G2,B0,B1,B2)																Page A: Bit map setting
Data 1001_{16}																	
⋮																	
Data $3AFE_{16}$																	
Data $3AFF_{16}$																	
Address 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
Data 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	Page B writing setting
Data 0002_{16}	0	VSIZE1	VSIZE0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Page B: Vertical display location setting
Data 0003_{16}	0	0	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Page B: Horizontal display location setting
Address 1000_{16}	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
Data 1000_{16}	Bit map RAM (PageB) (R0,R1,R2,G0,G1,G2,B0,B1,B2)																Page B: Bit map setting
Data 1001_{16}																	
⋮																	
Data $3AFF_{16}$																	
Data $3AFF_{16}$																	
Address 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address setting
Data 0000_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	Page A and B writing setting
Data 0001_{16}	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	Display ON

Notes 1. Registers PAGEONA and PAGEONB perform writing control of data.
2. Input the clock with which the cycle was fixed and continued from the TCK pin. Moreover, input horizontal synchronized signal into HOR pin, and input vertical synchronized signal into VERT pin.

Fig. 14 Example of data setting

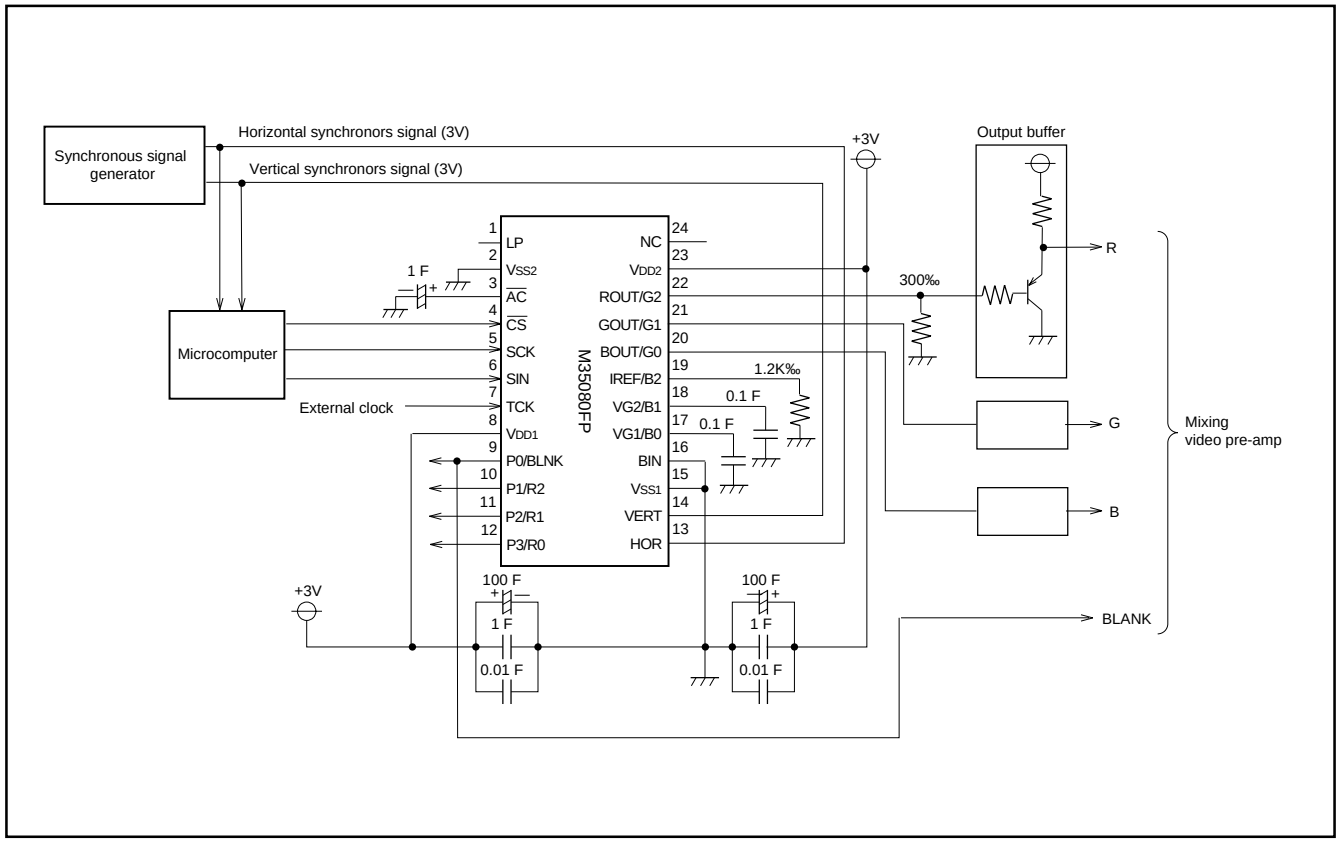


Fig.15 Example of the M35080FP peripheral circuit (at analog RGB output setting)

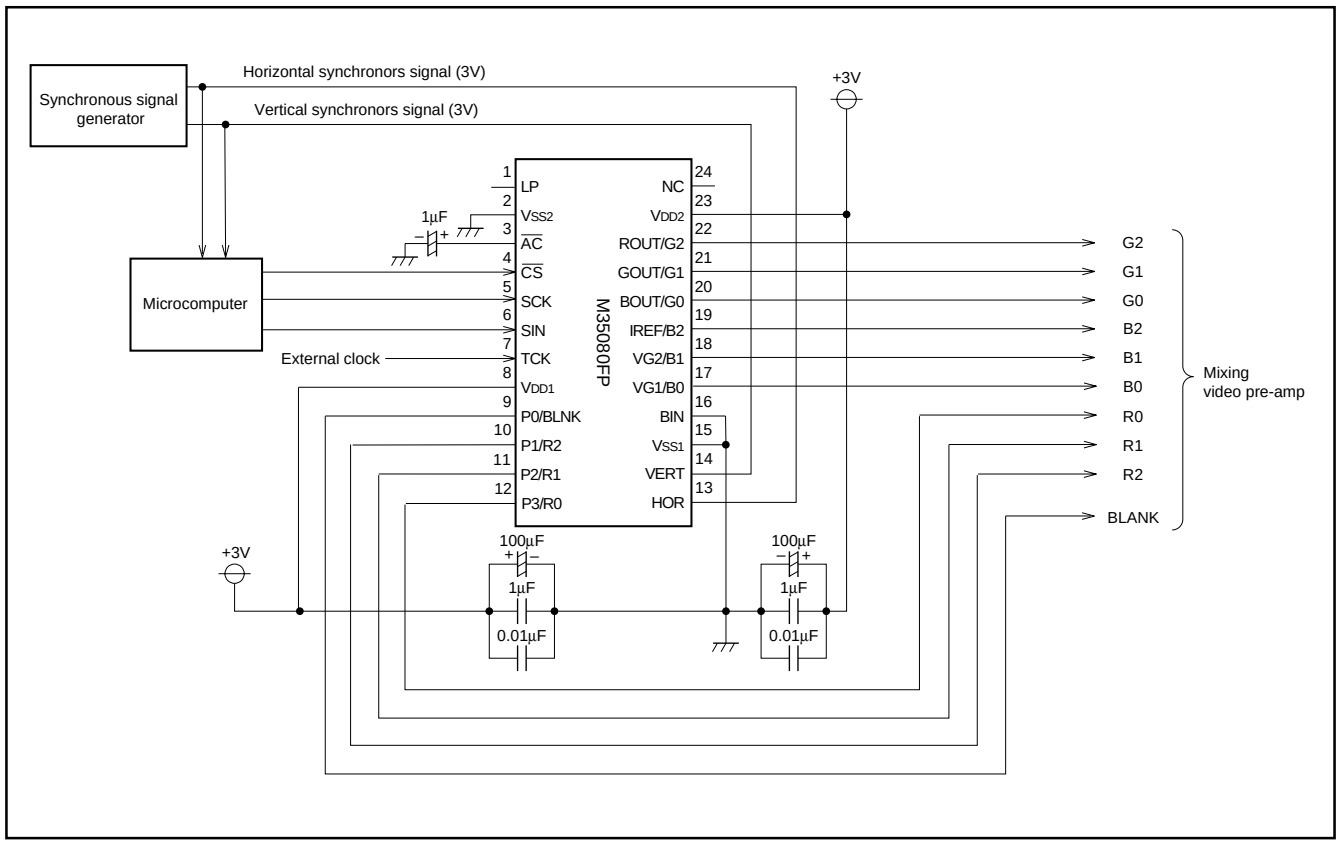


Fig.16 Example of the M35080FP peripheral circuit (at digital RGB output setting)

DATA INPUT

SERIAL DATA INPUT TIMING

(1) Serial data should be input with the LSB first.
(2) The address consists of 16 bits.
(3) The data consists of 16 bits.
(4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits. Therefore, it is not necessary to input the address from the second data.

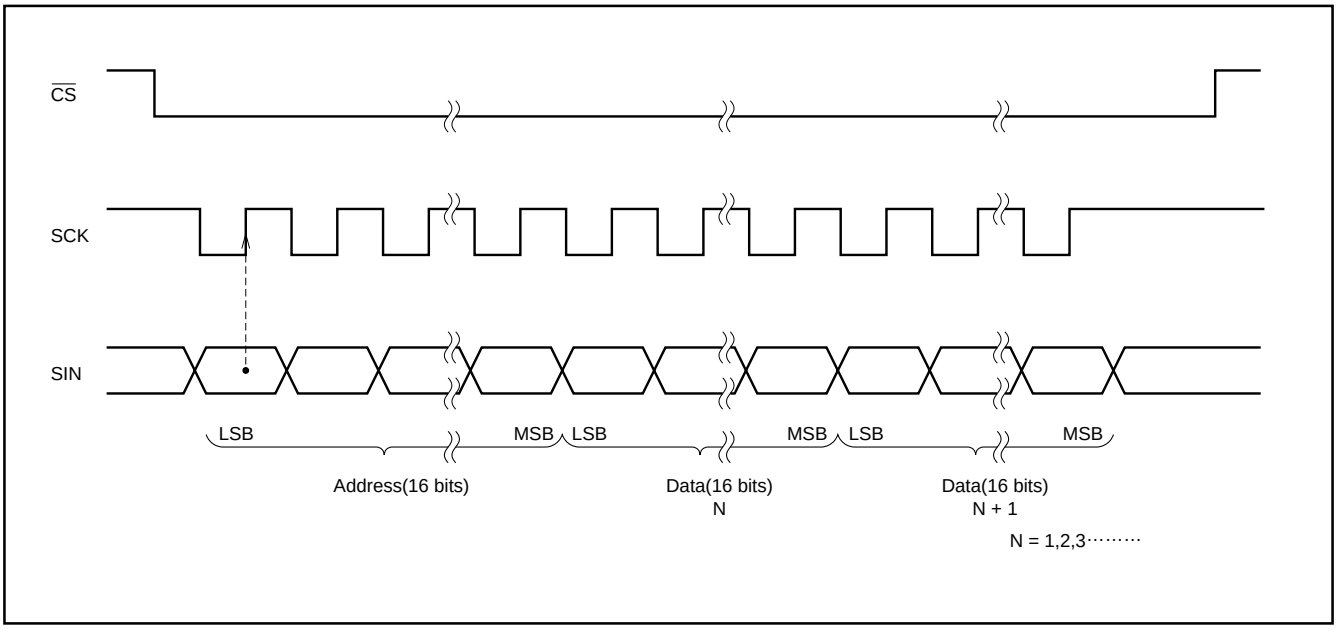


Fig.17 Serial input timing

TIMING REQUIREMENTS (V_{DD} = 3 ± 0.30 V, Ta = –20 to +85°C, unless otherwise noted)

Serial data input

Symbol	Parameter	Limits			Unit	Remarks
		Max.	Typ.	Max.		
tw(SCK)	SCK width	200	–	–	ns	Refer to fig 18
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	–	–	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	–	–	µs	
tsu(SIN)	SIN setup time	200	–	–	ns	
th(SIN)	SIN hold time	200	–	–	ns	
tword	1 word write time	10	–	–	µs	

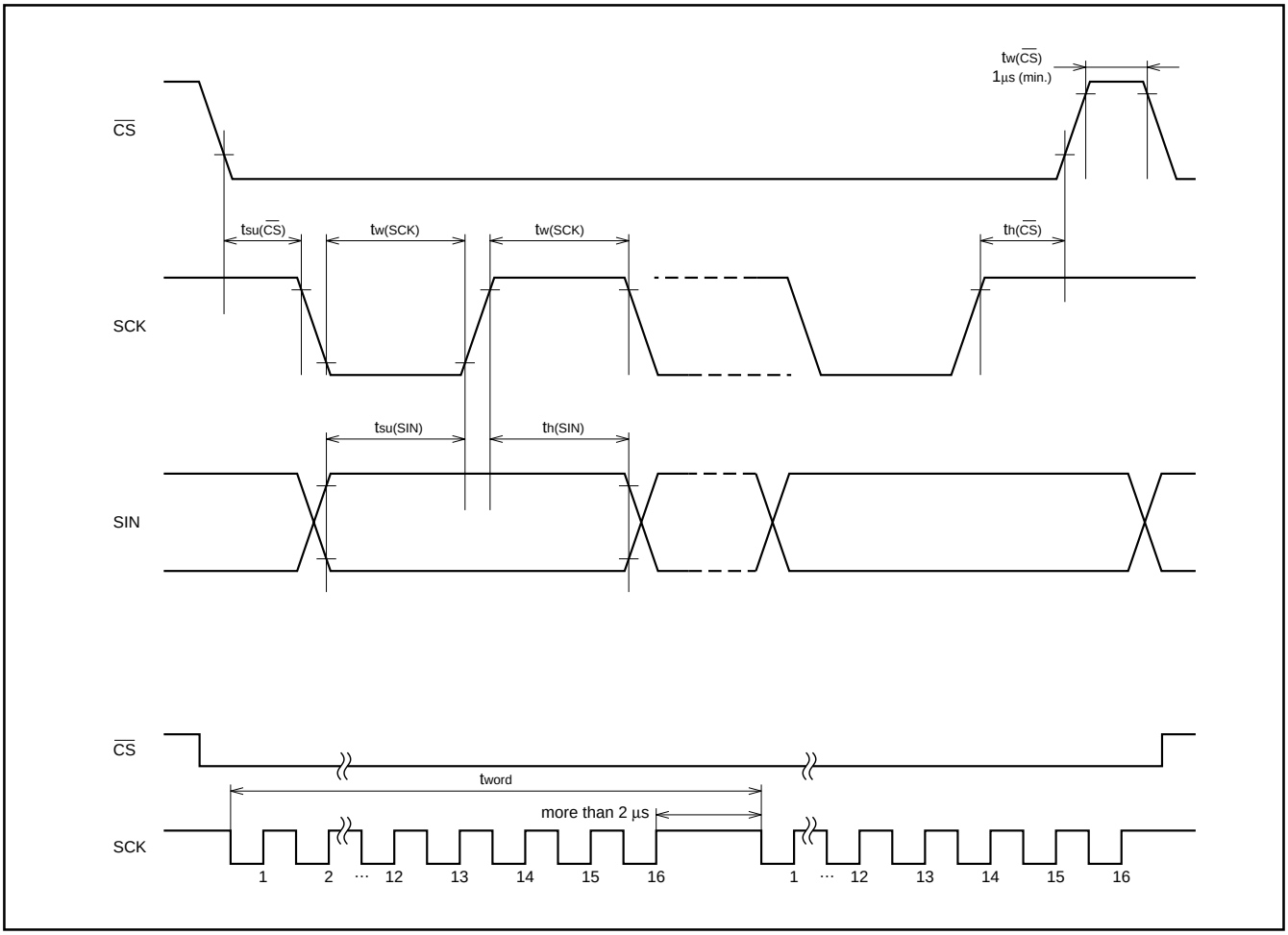


Fig.18 Serial input timing

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 3.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	–0.3 to +4.2	V
V_I	Input voltage		V_{SS} –0.3 ≤ V_I ≤ V_{DD} +0.3	V
V_O	Output voltage		V_{SS} ≤ V_O ≤ V_{DD}	V
P_d	Power dissipation	Ta = +25 °C	+70	mW
T_{opr}	Operating temperature		–20 to +85	°C
T_{stg}	Storage temperature		–40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 3.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		2.7	3.00	3.3	V
V_{IH}	"H" level input voltage	SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR, VERT	0.8 × V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage	SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR, VERT	0	0	0.2 × V_{DD}	V
F_{OSC}	Oscillating frequency for display		10.0	–	20.0	MHz
H.sync	Horizontal synchronous signal input frequeney		10.0	–	20.0	kHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.00V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		Ta = –20 to +70°C	2.70	3.00	3.30	V
I_{DD}	Supply current (at analog output)		V_{DD} = 3.00V	–	15	25	mA
V_{OH}	“H” level output voltage	P0 to P7,R0 to R2 G0 to G2,B0 to B2	V_{DD} = 2.70V, I_{OH} = –1mA	2.2	–	–	V
V_{OL}	“L” level output voltage	P0 to P7,R0 to R2 G0 to G2,B0 to B2	V_{DD} = 2.70V, I_{OL} = 1mA	–	–	0.5	V
R_I	Pull-up resistance $\overline{AC}$		V_{DD} = 3.00V	10	–	100	kΩ
V_{TCK}	External clock input width			0.7 × V_{DD}	–	V_{DD}	V
V_{DAO}	Full scale width	ROUT,GOUT,BOUT	R_{IREF}=1.2KΩ, R_L=300Ω	–	1.0	–	Vp-p
N_L	Nonlinear nature error	ROUT,GOUT,BOUT	R_{IREF}=1.2KΩ, R_L=300Ω	–	–	±2.0	LSB

NOTE FOR SUPPLYING POWER

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35080FP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor.

The timing about power supplying of $\overline{AC}$ pin is shown in Figure below.

After supplying the power (V_{DD} and V_{SS}) to M35080FP and the supply voltage becomes more than 0.8 × V_{DD}, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than 0.8 × V_{DD} and keeping 200ms wait time.

(2) Timing of power supplying to V_{DD1} and V_{DD2}.

Supply power to V_{DD1} and V_{DD2} at the same time.

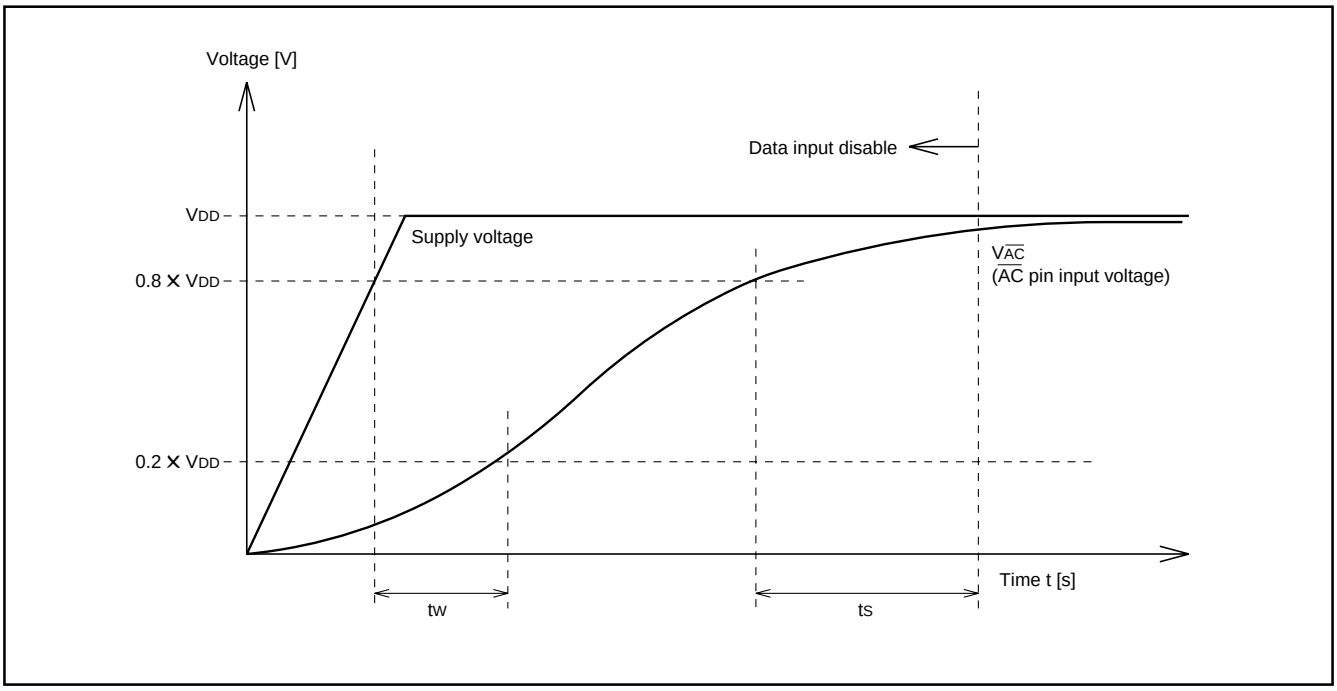


Fig.19 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor (≈0.1µF) directly between the V_{DD1} pin and V_{SS1} pin, and the V_{DD2} pin and V_{SS2} pin using a heavy wire.

Notes on the time of external clock input to TCK pin

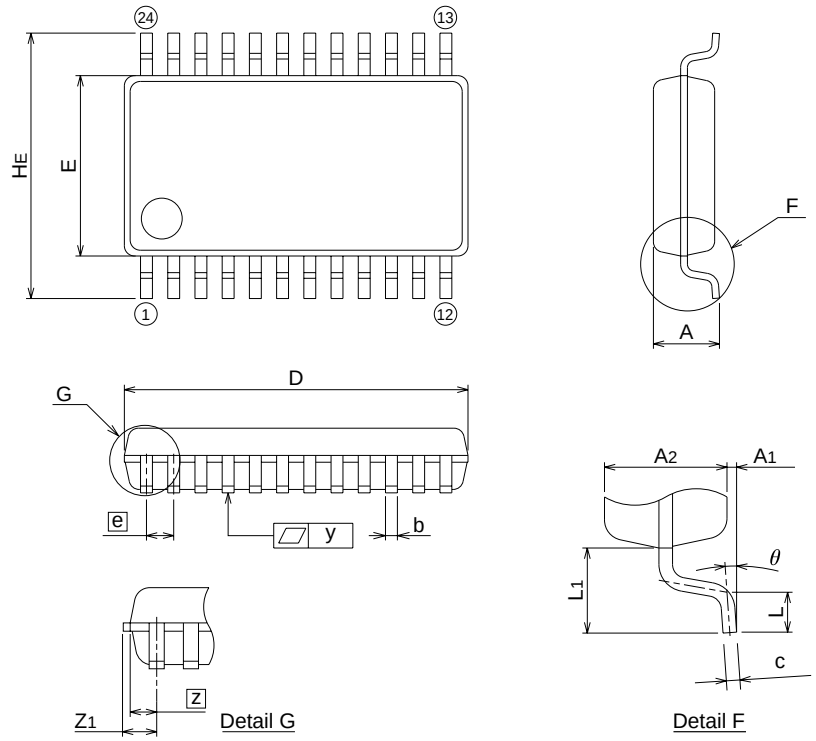
Input the continuous external clock which cycle is fixed and synchronized with horizontal synchronized signal from TCK pin. And, input continuous horizontal synchronized signal which cycle is fixed from HOR pin. Do not stop clock input absolutely during display.

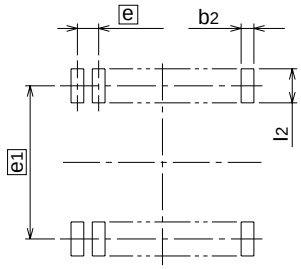
PACKAGE OUTLINE

24P2Q-A (MMP)

Plastic 24pin 300mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP24-P-300-0.80	–	0.2	Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A1	0	0.1	0.2
A2	–	1.8	–
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	–	0.8	–
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	–	1.25	–
z	–	0.65	–
Z1	–	–	0.8
y	–	–	0.1
θ	0°	–	8°
b2	–	0.5	–
e1	–	7.62	–
l2	1.27	–	–

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Rev. No.	Revision Description	Rev. date
1.0	First Edition	0203