ISL89400, ISL89401

100V, 1.25A Peak, High Frequency Half-Bridge Drivers

FN6614
Rev 3.00
December 4, 2015

The ISL89400, ISL89401 are 100V, high frequency, half-bridge N-Channel power MOSFET driver ICs. They are based on the popular HIP2100, HIP2101 half-bridge drivers, but offer several performance improvements. The ISL89400 has additional input hysteresis for superior operation in noisy environments and the inputs of the ISL89401 (like those of the ISL89400) can now safely swing to the V_{DD} supply rail. Finally, both parts are available in a very compact 9 Ld DFN package and an 8 Ld SOIC to minimize the required PCB footprint.

Applications

- Telecom half-bridge converters
- Telecom full-bridge converters
- Two-switch forward converters
- Active-clamp forward converters
- Class-D audio amplifiers

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	INPUT THRESHOLDS
ISL89400	CMOS Compatible
ISL89401	3.3V/TTL Compatible

Features

- Drives N-channel MOSFET half-bridge
- Space saving DFN package
- DFN package compliant with 100V conductor spacing guidelines per IPC-2221
- Pb-free (RoHS compliant)
- Bootstrap supply maximum voltage to 114VDC
- On-chip 1Ω bootstrap diode
- Fast propagation times for multi-MHz circuits
- Drives 1nF load with typical rise/fall times of 16ns
- CMOS compatible input thresholds (ISL89400)
- 3.3V/TTL compatible input thresholds (ISL89401)
- Independent inputs provide flexibility
- No start-up problems
- Outputs unaffected by supply glitches, HS ringing below ground or HS slewing at high dV/dt
- Low power consumption
- Wide supply voltage range (9V to 14V)
- Supply undervoltage protection
- 4.0Ω typical output pull-up/pull-down resistance

Application Block Diagram

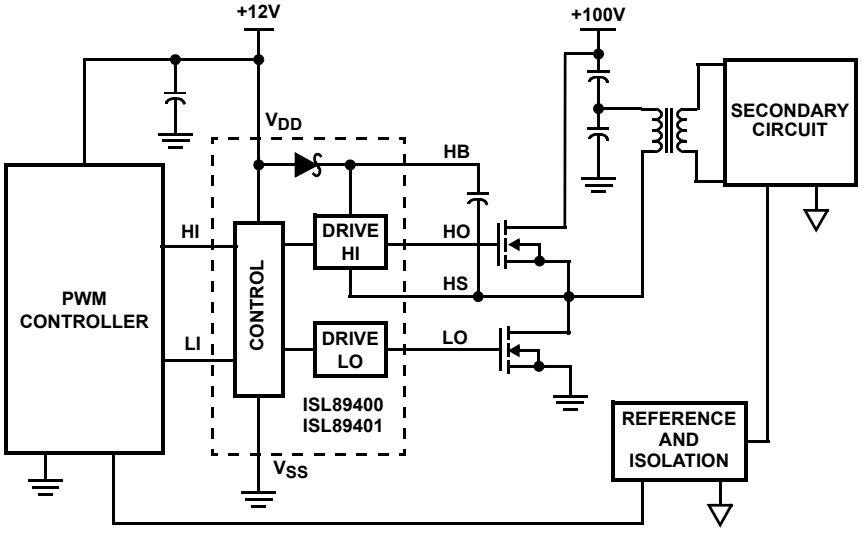


FIGURE 1. APPLICATION BLOCK DIAGRAM

Ordering Information

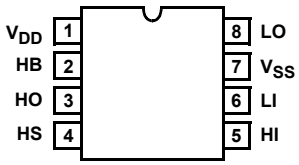
PART NUMBER (Notes 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL89400AR3Z (Note 1)	9400	-40 to +125	9 Ld 3x3 DFN	L9.3x3
ISL89401AR3Z (Note 1)	9401	-40 to +125	9 Ld 3x3 DFN	L9.3x3
ISL89400ABZ (Note 2)	89400 ABZ	-40 to +125	8 Ld SOIC	M8.15
ISL89401ABZ (Note 2)	89401 ABZ	-40 to +125	8 Ld SOIC	M8.15

NOTES:

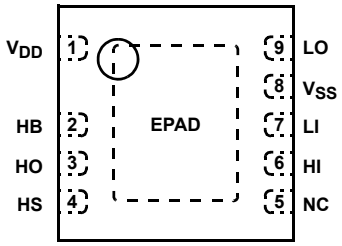
1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Add “-T” suffix for 2.5k unit or add “-TK” suffix for 1k unit tape and reel. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for ISL89400, ISL89401. For more information on MSL, please see tech brief TB363.

Pin Configurations

ISL89400, ISL89401
(8 LD SOIC)
TOP VIEW



ISL89400, ISL89401
(9 LD DFN)
TOP VIEW

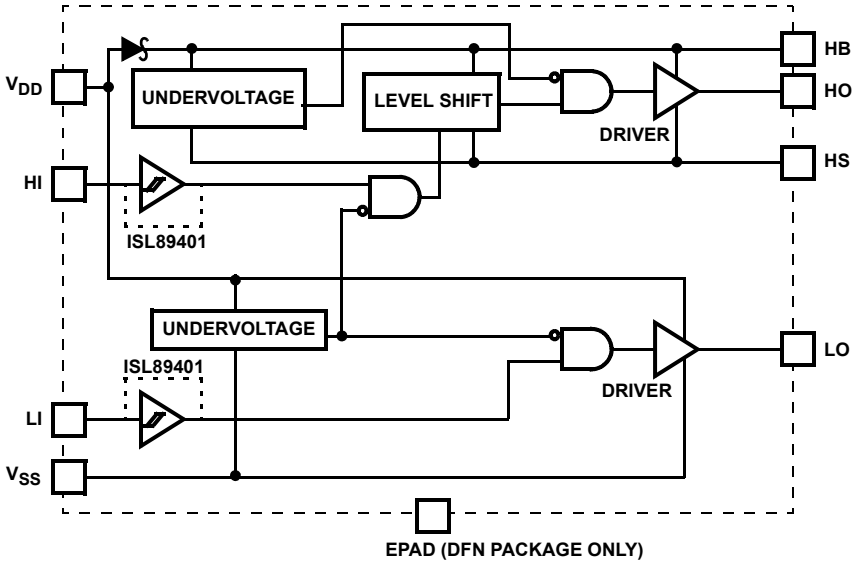


NOTE: EPAD = Exposed PAD.

Pin Descriptions

SYMBOL	DESCRIPTION
V_{DD}	Positive supply to lower gate driver. Bypass this pin to V_{SS}.
HB	High-side bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
HO	High-side output. Connect to gate of high-side power MOSFET.
HS	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	High-side input.
LI	Low-side input.
V_{SS}	Chip negative supply, which will generally be ground.
LO	Low-side output. Connect to gate of low-side power MOSFET.
NC	No connect.
EPAD	Exposed pad. Connect to ground or float. The EPAD is electrically isolated from all other pins.

Functional Block Diagram



*EPAD = EXPOSED PAD. THE EPAD IS ELECTRICALLY ISOLATED FROM ALL OTHER PINS. FOR BEST THERMAL PERFORMANCE, CONNECT THE EPAD TO THE PCB POWER GROUND PLANE.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

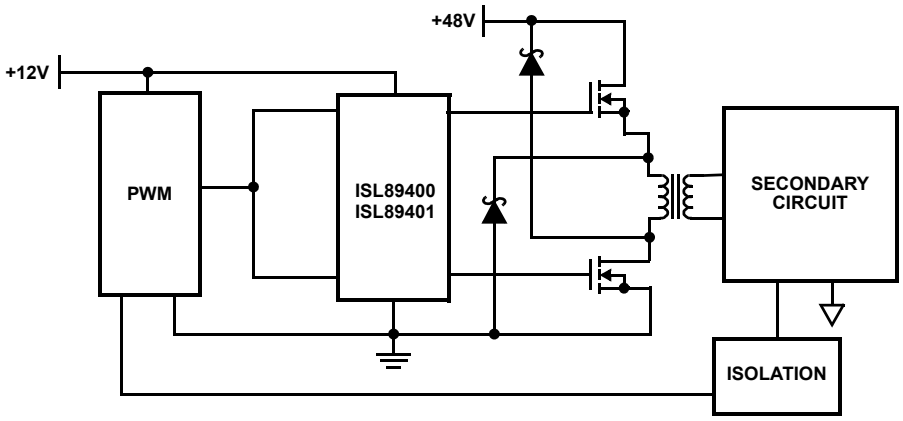


FIGURE 3. TWO-SWITCH FORWARD CONVERTER

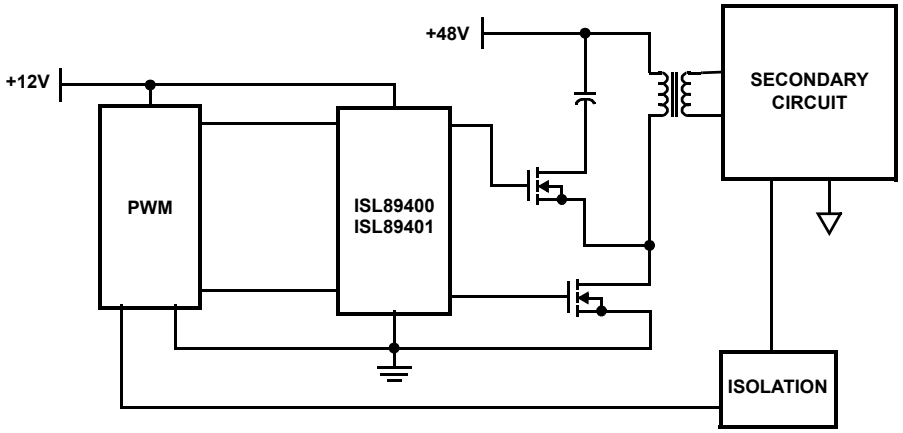


FIGURE 4. FORWARD CONVERTER WITH AN ACTIVE-CLAMP

Absolute Maximum Ratings

Supply Voltage, $V_{DD, VHB - VHS}$ (Note 6) ..... -0.3V to 18V
LI and HI Voltages (Note 6) ..... -0.3V to V_{DD} + 0.3V
Voltage on LO (Note 6) ..... -0.3V to V_{DD} + 0.3V
Voltage on HO (Note 6) ..... V_{HS} - 0.3V to V_{HB} + 0.3V
Voltage on HS (Continuous) (Note 6) ..... -1V to 110V
Voltage on HB (Note 6) 118V
Average Current in V_{DD} to HB Diode 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
9 Ld DFN (Notes 7, 9)	55	3.5
8 Ld SOIC (Notes 8, 10)	107	50

Max Power Dissipation at +25°C in Free Air (Note 7) 2.27W
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature Range ..... -55°C to +150°C
Pb-free reflow profile ..... see link TB493

Maximum Recommended Operating Conditions

Supply Voltage, V_{DD} (Note 5) ..... 9V to 14V
Voltage on HS ..... -1V to 100V
Voltage on HS ..... (Repetitive Transient) -5V to 105V
Voltage on HB ..... V_{HS} + 8V to V_{HS} + 14V and V_{DD} - 1V to V_{DD} + 100V
HS Slew Rate ..... <50V/ns

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. The ISL89400 and ISL89401 are capable of derated operation at supply voltages exceeding 14V. Figure 24 shows the high-side voltage derating curve for this mode of operation.
6. All voltages referenced to V_{SS}, unless otherwise specified.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.See Tech Brief TB379.
8. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
9. For θ_{JC}, the “case temp” is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379 for details.
10. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications

$V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits at –40°C and +125°C are established by characterization and are not production tested.

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS								
V_{DD} Quiescent Current	I_{DD}	ISL89400; LI = HI = 0V	-	0.1	0.25	-	0.3	mA
V_{DD} Quiescent Current	I_{DD}	ISL89401; LI = HI = 0V	-	0.3	0.45	-	0.55	mA
V_{DD} Operating Current	I_{DDO}	ISL89400; f = 500kHz	-	1.6	2.2	-	2.7	mA
V_{DD} Operating Current	I_{DDO}	ISL89401; f = 500kHz	-	1.9	2.5	-	3	mA
Total HB Quiescent Current	I_{HB}	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
Total HB Operating Current	I_{HBO}	f = 500kHz	-	2.0	2.5	-	3	mA
HB to V_{SS} Current, Quiescent	I_{HBS}	LI = HI = 0V; $V_{HB} = V_{HS}$ = 114V	-	0.05	1	-	10	µA
HB to V_{SS} Current, Operating	I_{HBSO}	f = 500kHz; $V_{HB} = V_{HS}$ = 114V	-	0.9	-	-	-	mA
INPUT PINS								
Low Level Input Voltage Threshold	V_{IL}	ISL89400	3.7	4.4	-	2.7	-	V
Low Level Input Voltage Threshold	V_{IL}	ISL89401	1.4	1.8	-	1.2	-	V
High Level Input Voltage Threshold	V_{IH}	ISL89400	-	6.6	7.4	-	8.4	V
High Level Input Voltage Threshold	V_{IH}	ISL89401	-	1.8	2.2	-	2.4	V
Input Voltage Hysteresis	V_{IHYS}	ISL89400	-	2.2	-	-	-	V
Input Pull-Down Resistance	R_I		-	210	-	100	500	kΩ

Electrical Specifications

$V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits at –40°C and +125°C are established by characterization and are not production tested. **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
UNDERVOLTAGE PROTECTION								
V_{DD} Rising Threshold	VDDR		6.8	7.3	7.8	6.5	8.1	V
V_{DD} Threshold Hysteresis	VDDH		-	0.6	-	-	-	V
HB Rising Threshold	VHBR		6.2	6.9	7.5	5.9	7.8	V
HB Threshold Hysteresis	VHBH		-	0.6	-	-	-	V
BOOTSTRAP DIODE								
Low Current Forward Voltage	V_{DL}	I_{VDD-HB} = 100µA	-	0.5	0.6	-	0.7	V
High Current Forward Voltage	V_{DH}	I_{VDD-HB} = 100mA	-	0.7	0.9	-	1	V
Dynamic Resistance	R_D	I_{VDD-HB} = 100mA	-	0.8	1	-	1.5	Ω
LO GATE DRIVER								
Low Level Output Voltage	V_{OLL}	I_{LO} = 100mA	-	0.4	0.5	-	0.7	V
High Level Output Voltage	V_{OHL}	I_{LO} = -100mA, $V_{OHL} = V_{DD} - V_{LO}$	-	0.4	0.5	-	0.7	V
Peak Pull-Up Current	I_{OHL}	V_{LO} = 0V	-	1.25	-	-	-	A
Peak Pull-Down Current	I_{OLL}	V_{LO} = 12V	-	1.25	-	-	-	A
HO GATE DRIVER								
Low Level Output Voltage	V_{OLH}	I_{HO} = 100mA	-	0.4	0.5	-	0.7	V
High Level Output Voltage	V_{OHH}	I_{HO} = -100mA, $V_{OHH} = V_{HB} - V_{HO}$	-	0.4	0.5	-	0.7	V
Peak Pull-Up Current	I_{OHH}	V_{HO} = 0V	-	1.25	-	-	-	A
Peak Pull-Down Current	I_{OLH}	V_{HO} = 12V	-	1.25	-	-	-	A

Switching Specifications

$V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits at –40°C and +125°C are established by characterization and are not production tested.

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	34	50	-	60	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	31	50	-	60	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	39	50	-	60	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	39	50	-	60	ns
Delay Matching: Upper Turn-Off to Lower Turn-On	t_{MON}		1	8	-	-	16	ns
Delay Matching: Lower Turn-Off to Upper Turn-On	t_{MOFF}		1	6	-	-	16	ns
Either Output Rise/Fall Time (10% to 90%/90% to 10%)	t_{RC}, t_{FC}	C_L = 1nF	-	16	-	-	-	ns
Either Output Rise/Fall Time (3V to 9V/9V to 3V)	t_R, t_F	C_L = 0.1µF	-	0.8	1.0	-	1.2	µs
Minimum Input Pulse Width that Changes the Output	t_{PW}		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	-	-	ns

Timing Diagrams

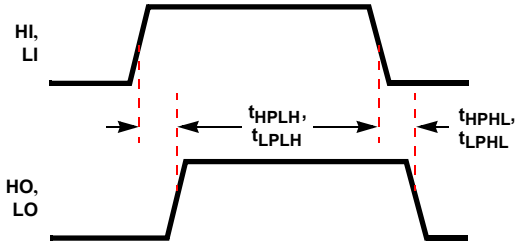


FIGURE 5. PROPAGATION DELAYS

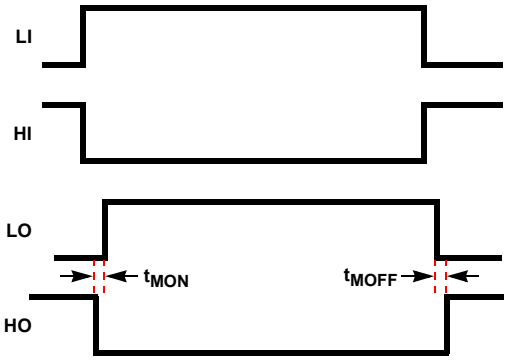


FIGURE 6. DELAY MATCHING

Typical Performance Curves

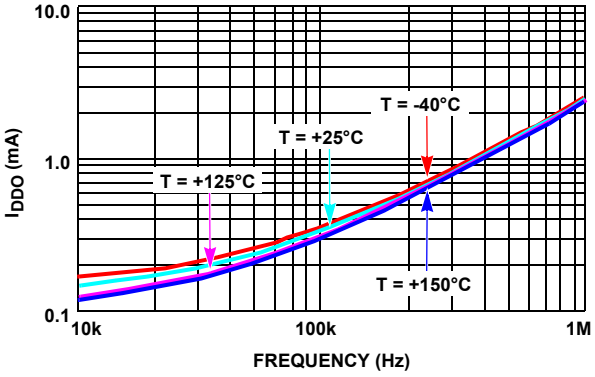


FIGURE 7. ISL89400 I_{DD} OPERATING CURRENT vs FREQUENCY

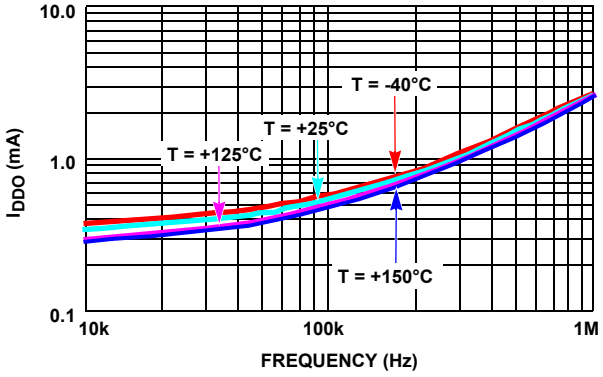


FIGURE 8. ISL89401 I_{DD} OPERATING CURRENT vs FREQUENCY

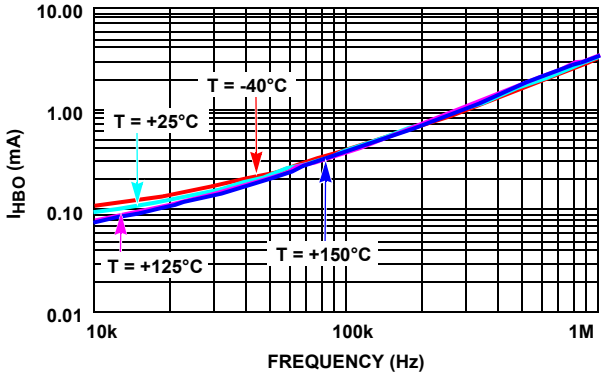


FIGURE 9. I_{HB} OPERATING CURRENT vs FREQUENCY

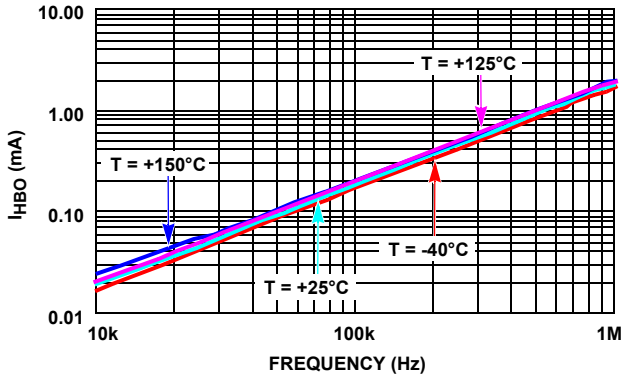


FIGURE 10. I_{HBS} OPERATING CURRENT vs FREQUENCY

Typical Performance Curves (Continued)

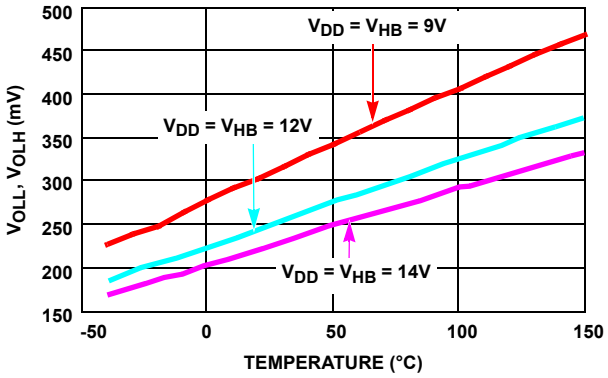


FIGURE 11. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

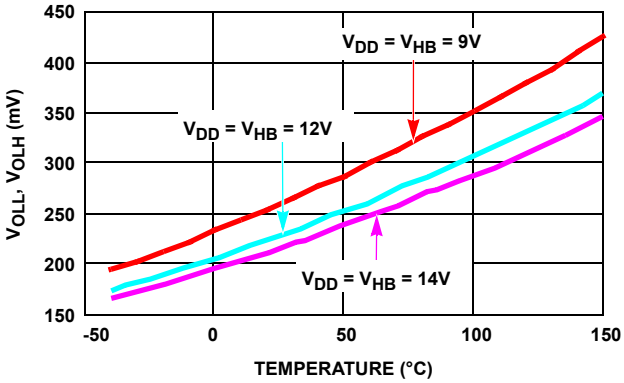


FIGURE 12. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

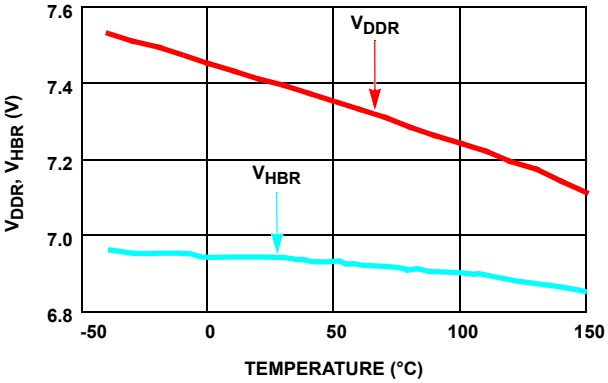


FIGURE 13. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

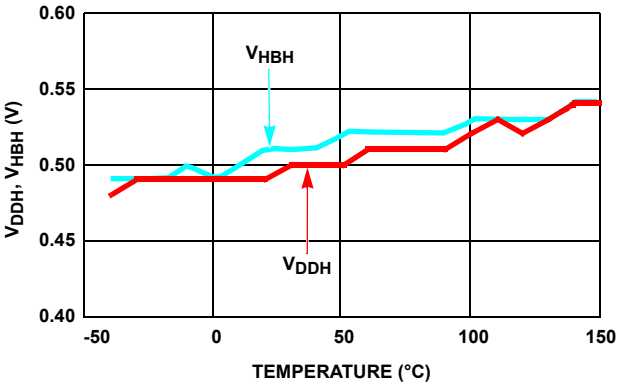


FIGURE 14. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

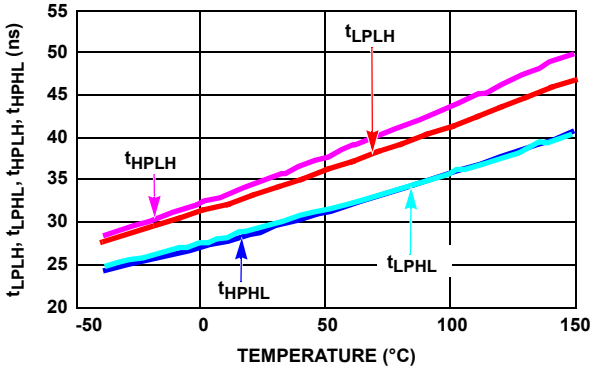


FIGURE 15. ISL89400 PROPAGATION DELAYS vs TEMPERATURE

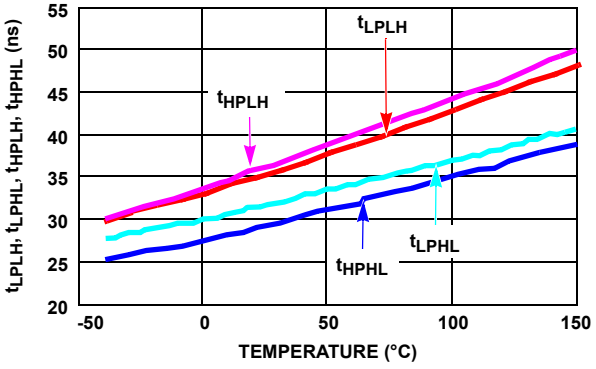


FIGURE 16. ISL89401 PROPAGATION DELAYS vs TEMPERATURE

Typical Performance Curves (Continued)

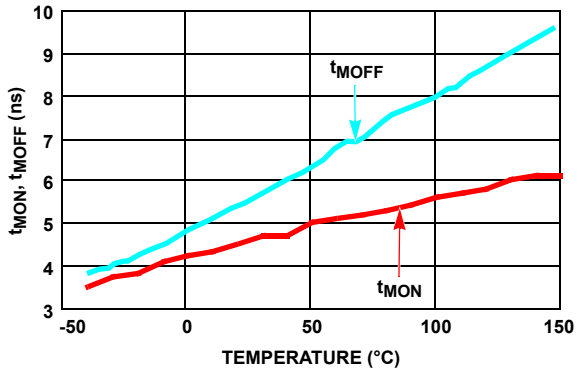


FIGURE 17. ISL89400 DELAY MATCHING vs TEMPERATURE

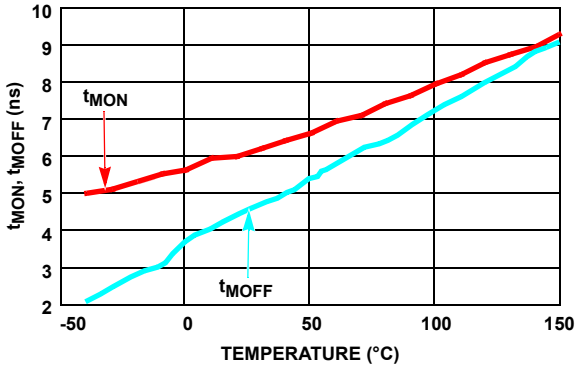


FIGURE 18. ISL89401 DELAY MATCHING vs TEMPERATURE

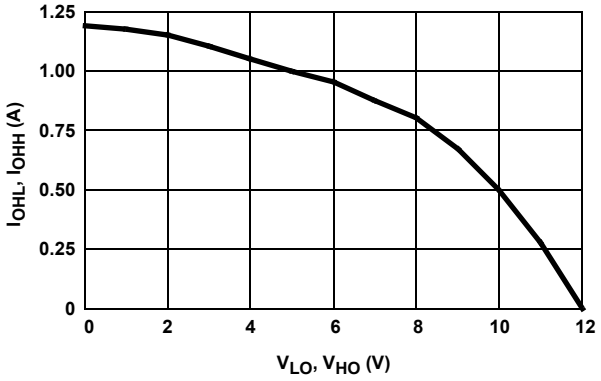


FIGURE 19. PEAK PULL-UP CURRENT vs OUTPUT VOLTAGE

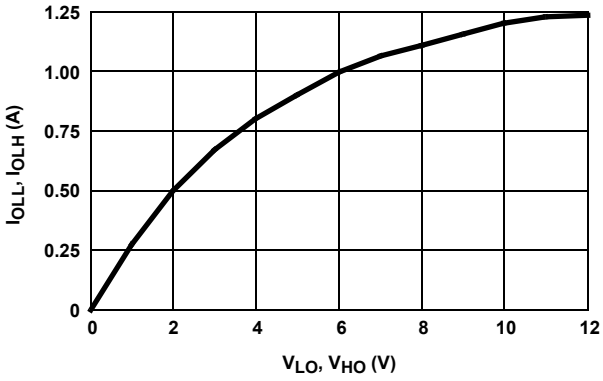


FIGURE 20. PEAK PULL-DOWN CURRENT vs OUTPUT VOLTAGE

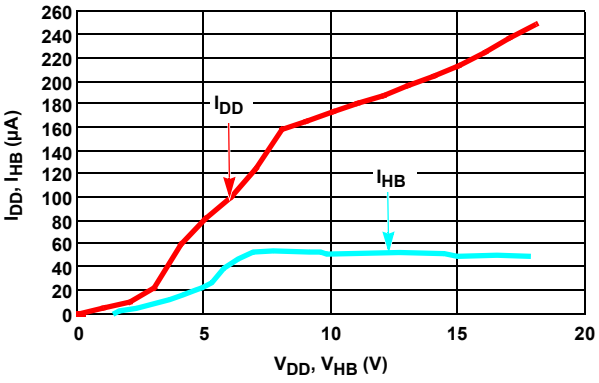


FIGURE 21. ISL89400 QUIESCENT CURRENT vs VOLTAGE

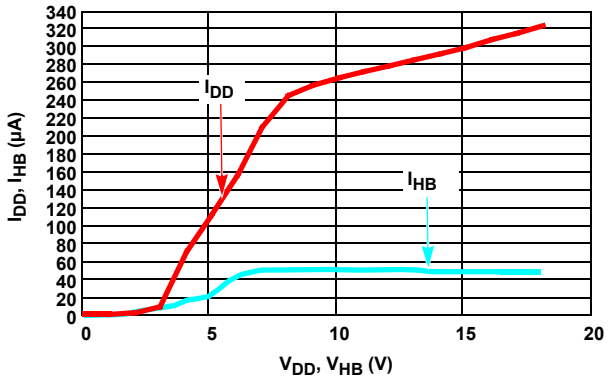


FIGURE 22. ISL89401 QUIESCENT CURRENT vs VOLTAGE

Typical Performance Curves (Continued)

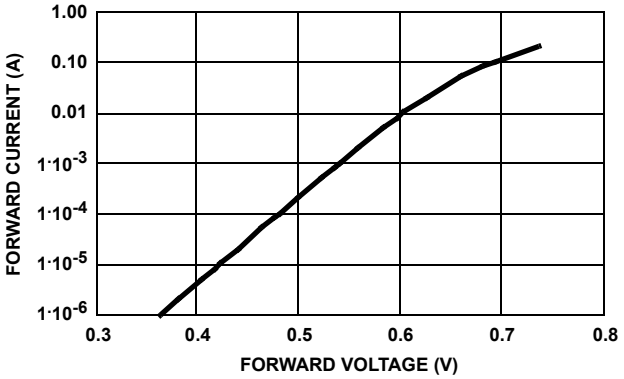


FIGURE 23. BOOTSTRAP DIODE I-V CHARACTERISTICS

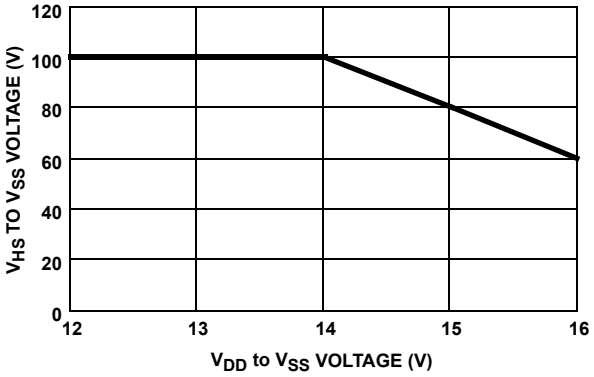


FIGURE 24. V_{HS} VOLTAGE vs V_{DD} VOLTAGE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 4, 2015	FN6614.3	Updated datasheet to the latest Intersil standards. Moved Note 5 from “Absolute Maximum Ratings” section to “Maximum Recommended Operating Conditions”section. Updated Theta JC on page 5 for DFN from “7.5” to “3.5”. Added Theta JC on page 5 for SOIC. Updated Theta JA on page 5 for SOIC from “115” to “107”. Added Note 10 on page 5. Updated last sentence in the “Electrical Specifications” table title area. Added more verbiage to “Switching Specifications” table title area. Added Revision History and About Intersil sections Updated package outline drawings to the latest revisions. Changes are as follows: M8.15 -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Changed Note 1 “1982” to “1994” L9.3x3 -Tiebar Note 9 added: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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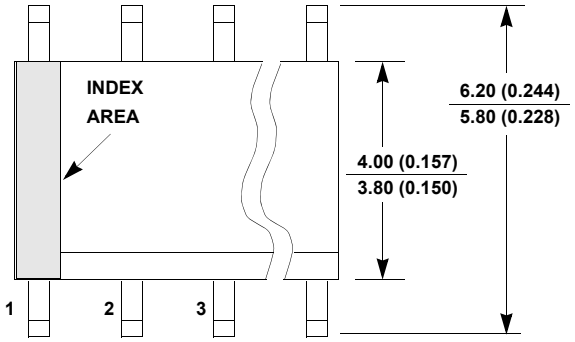
Package Outline Drawing

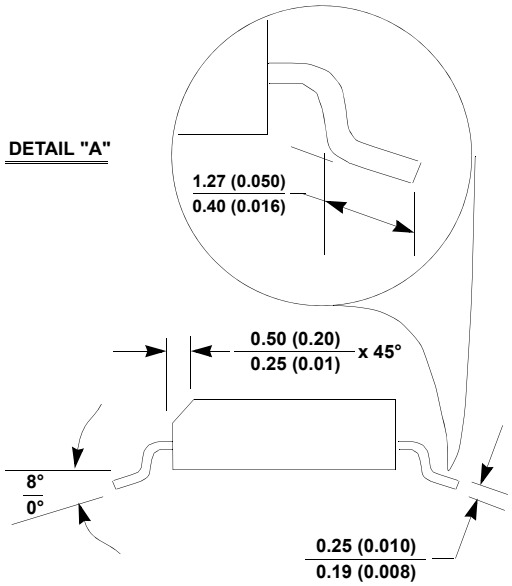
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

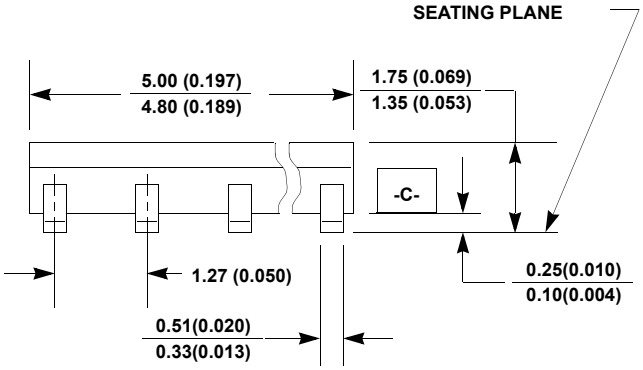
Rev 4, 1/12



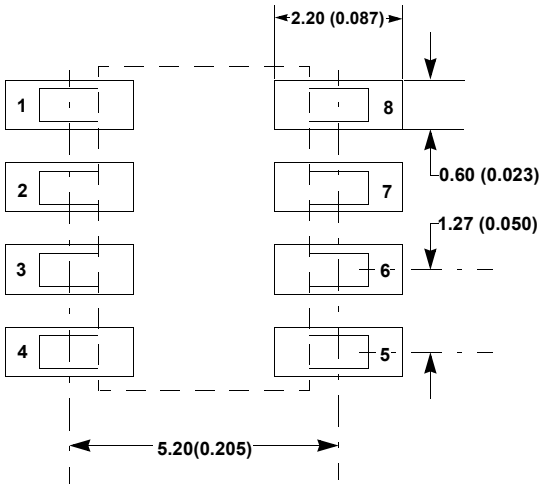
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

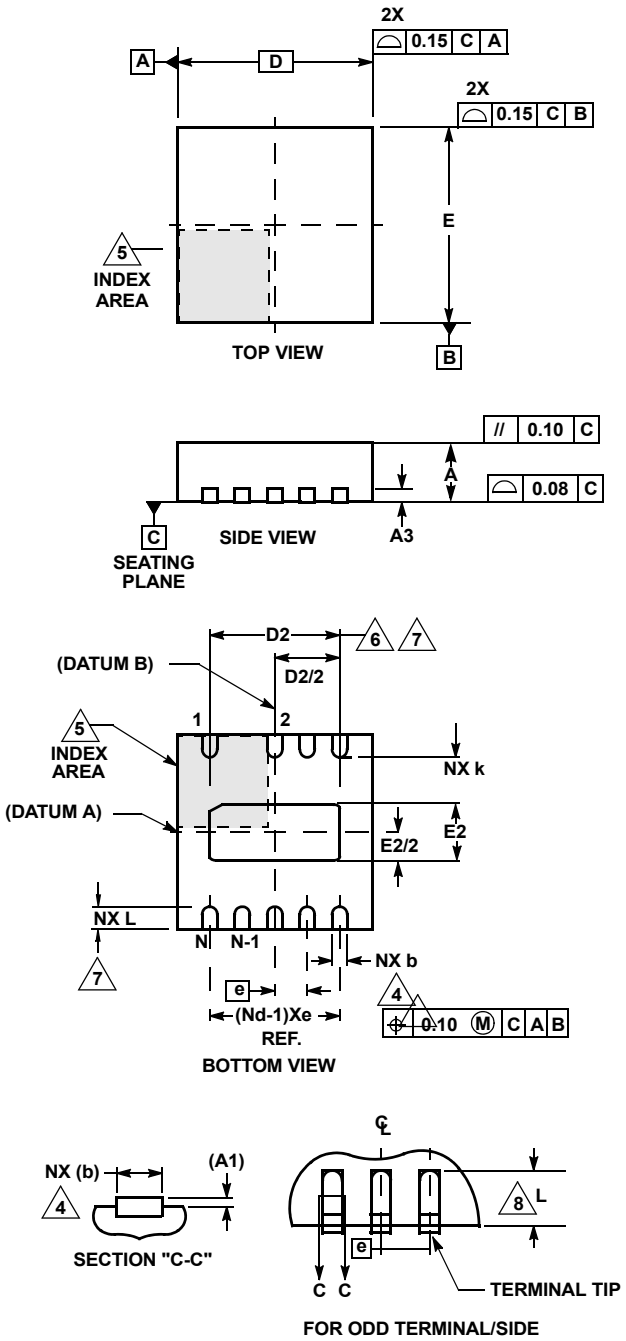


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Dual Flat No-Lead Plastic Package (DFN)



L9.3x3

9 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	4, 7
D		3.00 BSC		-
D2	1.85	2.00	2.10	6, 7
E		3.00 BSC		-
E2	0.80	0.95	1.05	6, 7
e		0.50 BSC		-
k	0.60	-	-	-
L	0.25	0.35	0.45	7
N		9		2

Rev. 1 3/15

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. All dimensions are in millimeters. Angles are in degrees.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
7. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
8. Compliant to JEDEC MO-229-WEED-3 except for dimensions E2 & D2.
9. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).