# ISL84467

## Ultra Low ON-Resistance, +1.65V to +4.5V, Single Supply, Quad SPDT (Dual DPDT) Analog Switch

The ISL84467 device is a low ON-resistance, low voltage, bidirectional, Quad SPDT (Dual DPDT) analog switch designed to operate from a single +1.65V to +4.5V supply. Targeted applications include battery powered equipment that benefit from low $r_{ON}$ (0.39Ω) and fast switching speeds ($t_{ON}$ = 33ns, $t_{OFF}$ = 16ns). The digital logic input is 1.8V logic-compatible when using a single +3V supply. With a supply voltage of 4.2V and logic high voltage of 2.85V at both logic inputs, the part draws only 12µA max of ICC current.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This part may be used to "mux-in" additional functionality while reducing ASIC design risk. The ISL84467 is offered in small form factor package, alleviating board space limitations.

The ISL84467 consists of four SPDT switches. It is configured as a dual double-pole/double-throw (DPDT) device with two logic control inputs that control two SPDT switches each. The configuration can be used as a dual differential 2-to-1 multiplexer/demultiplexer.

### TABLE 1. FEATURES AT A GLANCE

| ISL84467 | |
|---|---|
| Number of Switches | 4 |
| SW | Quad SPDT (Dual DPDT) |
| 4.3V $r_{ON}$ | 0.39Ω |
| 4.3V $t_{ON}/t_{OFF}$ | 33ns/16ns |
| 3.0V $r_{ON}$ | 0.45Ω |
| 3.0V $t_{ON}/t_{OFF}$ | 34ns/18ns |
| 1.8V $r_{ON}$ | 0.65Ω |
| 1.8V $t_{ON}/t_{OFF}$ | 50ns/25ns |
| Package | 16 Ld 3x3 TQFN, 16 Ld TSSOP |

## Features

- ON-Resistance ($r_{ON}$)
  - V+ = +4.3V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.39Ω
  - V+ = +3.0V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.45Ω
  - V+ = +1.8V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.65Ω
- $r_{ON}$ Matching Between Channels . . . . . . . . . . . . . . . . .0.05Ω
- $r_{ON}$ Flatness Across Signal Range . . . . . . . . . . . . . . .0.05Ω
- Single Supply Operation. . . . . . . . . . . . . . . . . +1.65V to +4.5V
- Low Power Consumption (PD). . . . . . . . . . . . . . . . . <0.68µW
- Fast Switching Action (V+ = +4.3V)
  - $t_{ON}$ · · · · · · · · · · · · · · · · · · · · · · · · · · · · · · · 33ns
  - $t_{OFF}$ · · · · · · · · · · · · · · · · · · · · · · · · · · · · · · 16ns
- Break-Before-Make
- 1.8V Logic Compatible (+3V supply)
- Low ICC Current when VinH is not at the V+ Rail
- Available in 16 Ld 3x3 TQFN and 16 Ld TSSOP Packages
- ESD HBM Rating
  - COM Pins . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9kV
  - All Othe r Pins. . . . . . . . . . . . . . . . . . . . . . . . . . . . 6kV
- Pb-Free (RoHS compliant)

## Applications

- Battery-Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

## Related Literature

- Technical Brief TB363, *Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)*
- Application Note AN557, *Recommended Test Procedures for Analog Switches*

## Pinouts (Note 1)

**ISL84467
(16 LD TQFN)
TOP VIEW**



**ISL84467
(16 LD TSSOP)
TOP VIEW**
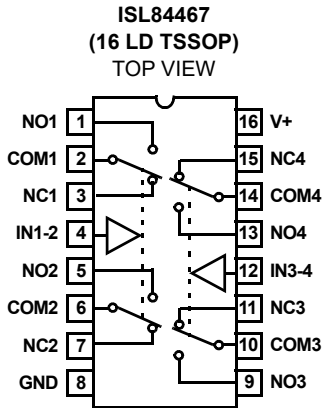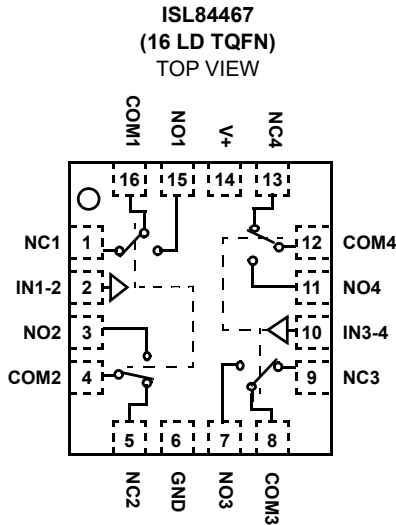


## Truth Table

| LOGIC | NC SW | NO SW |
|-------|-------|-------|
| 0 | ON | OFF |
| 1 | OFF | ON |

NOTE:   Logic "0" ≤0.5V.  Logic "1" ≥1.4V with a 3V supply.

## Pin Descriptions

| PIN | FUNCTION |
|-----|----------|
| V+ | System Power Supply Input (+1.65V to +4.5V) |
| GND | Ground Connection |
| IN | Digital Control Input |
| COM | Analog Switch Common Pin |
| NO | Analog Switch Normally Open Pin |
| NC | Analog Switch Normally Closed Pin |

NOTE:

1. Switches Shown for Logic "0" Input.

## Ordering Information

| PART NUMBER (Note 1) | PART MARKING | PACKAGE DESCRIPTION (RoHS Compliant) | PKG. DWG. # | CARRIER TYPE (Note 2) | TEMP. RANGE |
|---|---|---|---|---|---|
| ISL84467IRTZ | 67TZ | 16 Ld 3x3 TQFN | L16.3x3A | Tube | -40 to +85°C |
| ISL84467IRTZ-T | | | | Reel, 6k | |
| ISL84467IVZ | 84467 IVZ | 16 Ld TSSOP | M16.173 | Tube | -40 to +85°C |
| ISL84467IVZ-T | | | | Reel, 2.5k | |

NOTES:

1. These Pb-Free plastic packaged products employ special Pb-Free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-Free soldering operations). Pb-Free products are MSL classified at Pb-Free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

2. See TB347 for details about reel specifications.

## Absolute Maximum Ratings

V+ to GND . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5 to 5.5V
Input Voltages
  NO, NC, IN (Note 3) . . . . . . . . . . . . . . . . . . . -0.5 to ((V+) + 0.5V)
Output Voltages
  COM (Note 3) . . . . . . . . . . . . . . . . . . . . . . . . -0.5 to ((V+) + 0.5V)
Continuous Current NO, NC, or COM . . . . . . . . . . . . . . . . ±300mA
Peak Current NO, NC, or COM
  (Pulsed 1ms, 10% Duty Cycle, Max) . . . . . . . . . . . . . . . ±500mA
ESD Rating:
  Human Body Model ($COM_X$) . . . . . . . . . . . . . . . . . . . . . . . . . >9kV
  Human Body Model ($NO_X$, $NC_X$, $IN_X$, V+, GND) . . . . . . . . . >6kV
  Machine Model ($COM_X$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . >700V
  Machine Model ($NO_X$, $NC_X$, $IN_X$, V+, GND). . . . . . . . . . . . >300V
  Charged Device Model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . >1kV

## Thermal Information

Thermal Resistance (Typical)          $\theta_{JA}$ (°C/W)
  TQFN Package (Note 4) . . . . . . . . . . . . . . . . . . . . . .   70
  TSSOP Package (Note 5) . . . . . . . . . . . . . . . . . . . .   115
Maximum Storage Temperature Range . . . . . . . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . . . . . . . . . . . . . . . . . . . . . . . . .see TB493

## Operating Conditions

Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . . -40°C to +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

3. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

5. $\theta_{JA}$ is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, $V_{INH}$ = 1.6V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified.

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 10) | TYP | MAX (Notes 7, 10) | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON-Resistance, $r_{ON}$ | V+ = 3.9V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+ (See Figure 5, Note 11) | 25 | - | 0.4 | - | Ω |
| | | Full | - | 0.45 | - | Ω |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$ | V+ = 3.9V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = Voltage at max $r_{ON}$ (Notes 9, 11) | 25 | - | 0.05 | - | Ω |
| | | Full | - | 0.06 | - | Ω |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$ | V+ = 3.9V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+ (Notes 8, 11) | 25 | - | 0.05 | - | Ω |
| | | Full | - | 0.05 | - | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 4.5V, $V_{COM}$ = 0.3V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 0.3V | 25 | -70 | - | 70 | nA |
| | | Full | -165 | - | 165 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 4.5V, $V_{COM}$ = 0.3V, 3V, or $V_{NO}$ or $V_{NC}$ = 0.3V, 3V | 25 | -70 | - | 70 | nA |
| | | Full | -165 | - | 165 | nA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | V+ = 3.9V, $V_{NO}$ or $V_{NC}$ = 3.0V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 1) | 25 | - | 33 | - | ns |
| | | Full | - | 38 | - | ns |
| Turn-OFF Time, $t_{OFF}$ | V+ = 3.9V, $V_{NO}$ or $V_{NC}$ = 3.0V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 1) | 25 | - | 16 | - | ns |
| | | Full | - | 21 | - | ns |
| Break-Before-Make Time Delay, $t_D$ | V+ = 4.5V, $V_{NO}$ or $V_{NC}$ = 3.0V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 3) | Full | - | 3 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (See Figure 2) | 25 | - | 248 | - | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$ (See Figure 4) | 25 | - | 65 | - | dB |

## Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, $V_{INH}$ = 1.6V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified. **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 10) | TYP | MAX (Notes 7, 10) | UNIT |
|---|---|---|---|---|---|---|
| Crosstalk (Channel-to-Channel) | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$ (See Figure 6) | 25 | - | -85 | - | dB |
| Total Harmonic Distortion | f = 20Hz to 20kHz, $V_{COM}$ = 2$V_{P-P}$, $R_L$ = 600Ω | 25 | - | 0.008 | - | % |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) | 25 | - | 38 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) | 25 | - | 102 | - | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | | Full | 1.65 | - | 4.5 | V |
| Positive Supply Current, I+ | V+ = +4.5V, $V_{IN}$ = 0V or V+ | 25 | - | - | 0.15 | µA |
| | | Full | - | - | 1.4 | µA |
| Positive Supply Current, I+ | V+ = +4.2V, $V_{IN}$ = 2.85V | 25 | - | - | 13 | µA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage Low, $V_{INL}$ | | Full | - | - | 0.5 | V |
| Input Voltage High, $V_{INH}$ | | Full | 1.6 | - | - | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 4.5V, $V_{IN}$ = 0V or V+ | Full | -0.5 | - | 0.5 | µA |

## Electrical Specifications - 3.0V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, $V_{INH}$ = 1.4V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified.

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 10) | TYP | MAX (Notes 7, 10) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON-Resistance, $r_{ON}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+ (See Figure 5, Note 11) | 25 | - | 0.55 | 0.75 | Ω |
| | | Full | - | - | 0.85 | Ω |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = Voltage at max $r_{ON}$ (Notes 9, 11) | 25 | - | 0.08 | 0.19 | Ω |
| | | Full | - | - | 0.22 | Ω |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+ (Notes 8, 11) | 25 | - | 0.07 | 0.15 | Ω |
| | | Full | - | - | 0.15 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 3.3V, $V_{COM}$ = 0.3V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 0.3V | 25 | - | 1.1 | - | nA |
| | | Full | - | 30 | - | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 3.3V, $V_{COM}$ = 0.3V, 3V, or $V_{NO}$ or $V_{NC}$ = 0.3V, 3V, or Floating | 25 | - | 1.5 | - | nA |
| | | Full | - | 45 | - | nA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | V+ = 2.7V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 1) | 25 | - | 34 | - | ns |
| | | Full | - | 39 | - | ns |
| Turn-OFF Time, $t_{OFF}$ | V+ = 2.7V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 1) | 25 | - | 18 | - | ns |
| | | Full | - | 23 | - | ns |
| Break-Before-Make Time Delay, $t_D$ | V+ = 3.3V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 3) | Full | - | 3 | - | ns |

**Electrical Specifications - 3.0V Supply** Test Conditions:  V+ = +2.7V to +3.3V, GND = 0V, $V_{INH}$ = 1.4V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified. **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 10) | TYP | MAX (Notes 7, 10) | UNITS |
|---|---|---|---|---|---|---|
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (See Figure 2) | 25 | - | 126 | - | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$ (See Figure 4) | 25 | - | 65 | - | dB |
| Crosstalk (Channel-to-Channel) | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$ (See Figure 6) | 25 | - | -85 | - | dB |
| Total Harmonic Distortion | f = 20Hz to 20kHz, $V_{COM}$ = 2$V_{P-P}$, $R_L$ = 600Ω | 25 | - | 0.012 | - | % |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) | 25 | - | 38 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (See Figure 7) | 25 | - | 102 | - | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Positive Supply Current, I+ | V+ = 3.6V, $V_{IN}$ = 0V or V+ | 25 | - | 0.021 | - | µA |
| | | Full | - | 0.72 | - | µA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage Low, $V_{INL}$ | | Full | - | - | 0.5 | V |
| Input Voltage High, $V_{INH}$ | | Full | 1.4 | - | - | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 3.6V, $V_{IN}$ = 0V or V+ | Full | -0.5 | - | 0.5 | µA |

**Electrical Specifications - 1.8V Supply** Test Conditions:  V+ = +1.65V to +2V, GND = 0V, $V_{INH}$ = 1.0V, $V_{INL}$ = 0.4V (Note 6), Unless Otherwise Specified.

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 10) | TYP | MAX (Notes 7, 10) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON-Resistance, $r_{ON}$ | V+ = 1.8V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+ (See Figure 5, Note 11) | 25 | - | 0.7 | 0.9 | Ω |
| | | Full | - | - | 0.95 | Ω |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | V+ = 1.65V, $V_{NO}$ or $V_{NC}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 1) | 25 | - | 50 | - | ns |
| | | Full | - | 55 | - | ns |
| Turn-OFF Time, $t_{OFF}$ | V+ = 1.65V, $V_{NO}$ or $V_{NC}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 1) | 25 | - | 25 | - | ns |
| | | Full | - | 30 | - | ns |
| Break-Before-Make Time Delay, $t_D$ | V+ = 2.0V, $V_{NO}$ or $V_{NC}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF (See Figure 3) | Full | - | 8 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (See Figure 2) | 25 | - | 48 | - | pC |

**Electrical Specifications - 1.8V Supply**   Test Conditions:  V+ = +1.65V to +2V, GND = 0V, $V_{INH}$ = 1.0V, $V_{INL}$ = 0.4V (Note 6), Unless Otherwise Specified. **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 10) | TYP | MAX (Notes 7, 10) | UNITS |
|---|---|---|---|---|---|---|
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Low, $V_{INL}$ | | Full | - | - | 0.4 | V |
| Input Voltage High, $V_{INH}$ | | Full | 1.0 | - | - | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 2.0V, $V_{IN}$ = 0V or V+ | Full | -0.5 | - | 0.5 | µA |

NOTES:

6.  $V_{IN}$ = input voltage to perform proper function.

7.  The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

8.  Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.

9.  $r_{ON}$ matching between channels is calculated by subtracting the channel with the highest max $r_{ON}$ value from the channel with lowest max $r_{ON}$ value, between NC1 and NC2, NC3 and NC4 or between NO1 and NO2, NO3 and NO4.

10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

11. Limits established by characterization and are not production tested.

## *Test Circuits and Waveforms*
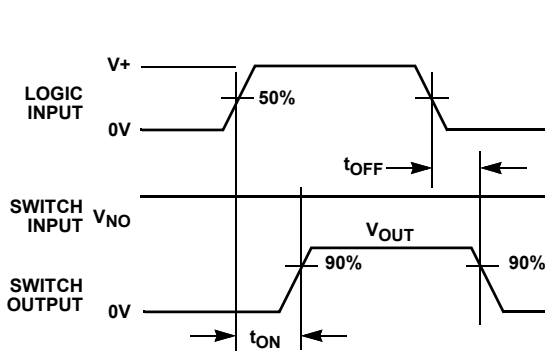


Logic input waveform is inverted for switches that have the opposite logic sense.

**FIGURE 1A.  MEASUREMENT POINTS**
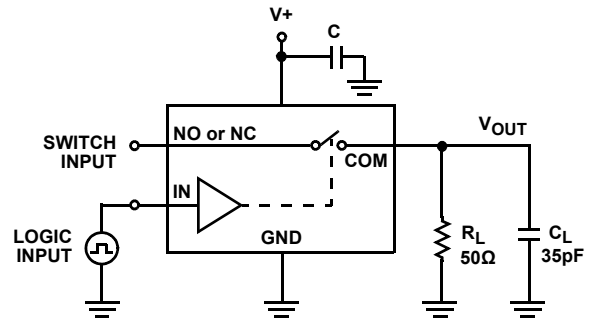


Repeat test for all switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

**FIGURE 1B.  TEST CIRCUIT**

**FIGURE 1.  SWITCHING TIMES**



$$Q = DV_{OUT} \times C_L$$
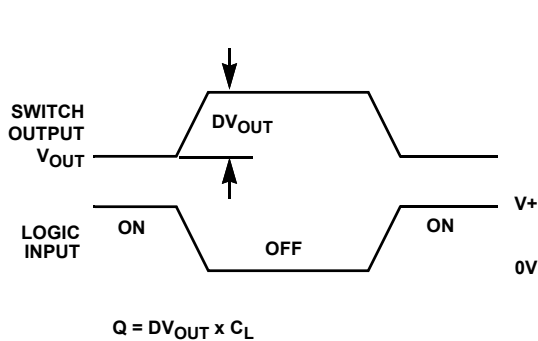
**FIGURE 2A.  MEASUREMENT POINTS**
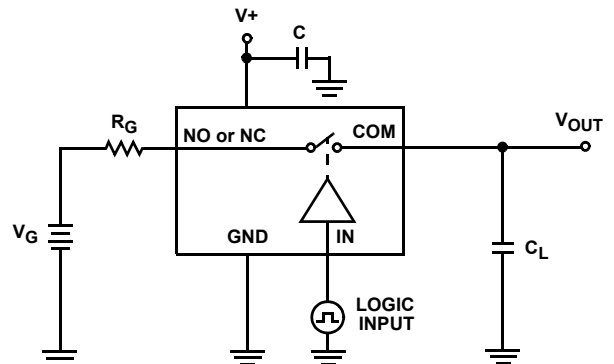


**FIGURE 2B.  TEST CIRCUIT**

## *Test Circuits and Waveforms* (Continued)

**FIGURE 2. CHARGE INJECTION**





$C_L$ includes fixture and stray capacitance.
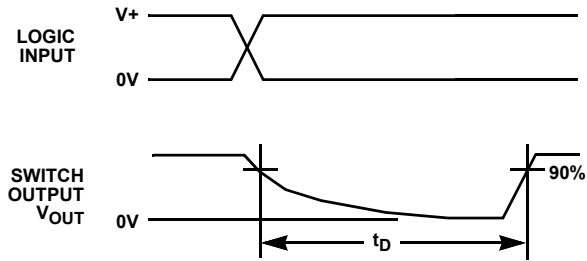
**FIGURE 3A. MEASUREMENT POINTS**

**FIGURE 3B. TEST CIRCUIT**

**FIGURE 3. BREAK-BEFORE-MAKE TIME**
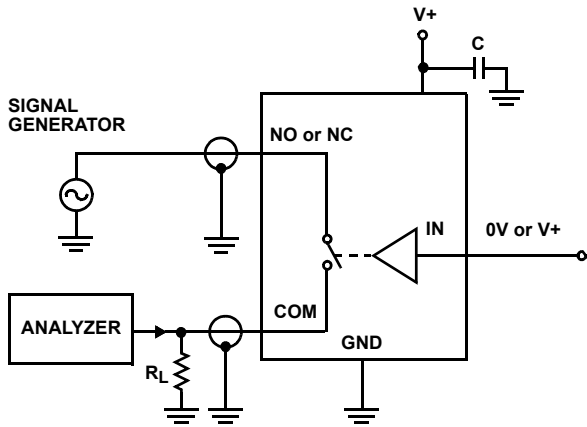




**FIGURE 4. OFF ISOLATION TEST CIRCUIT**
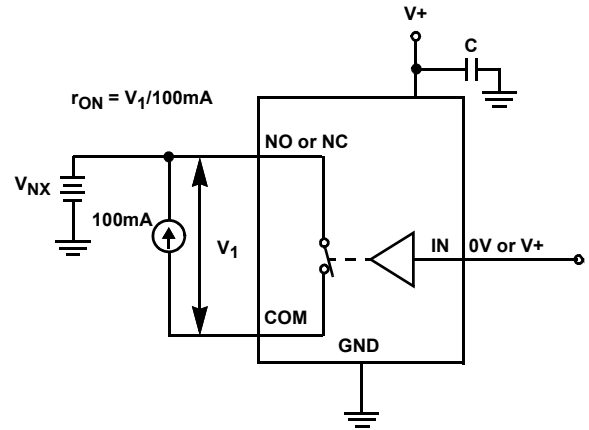
**FIGURE 5. $r_{ON}$ TEST CIRCUIT**
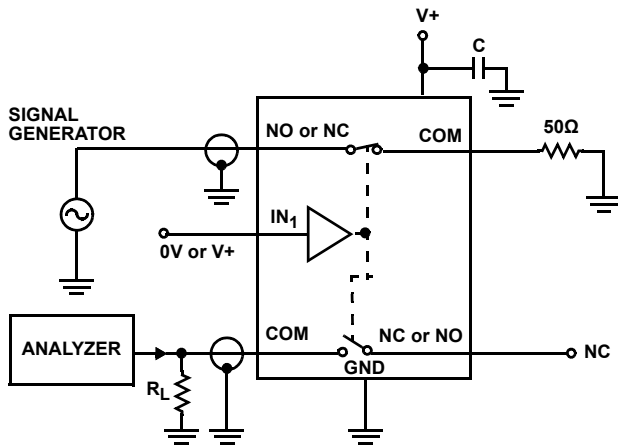




**FIGURE 6. CROSSTALK TEST CIRCUIT**
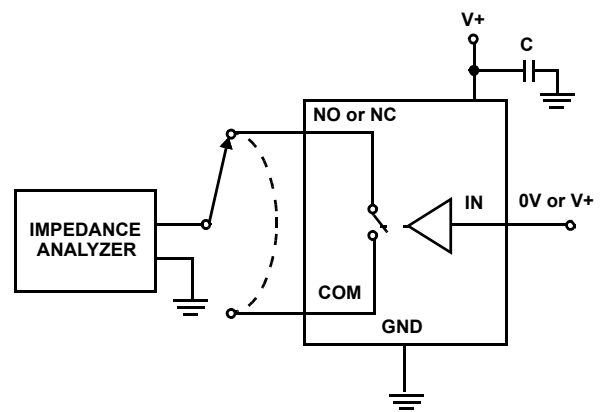
**FIGURE 7. CAPACITANCE TEST CIRCUIT**

## Typical Performance Curves $T_A$ = +25°C, unless otherwise specified.
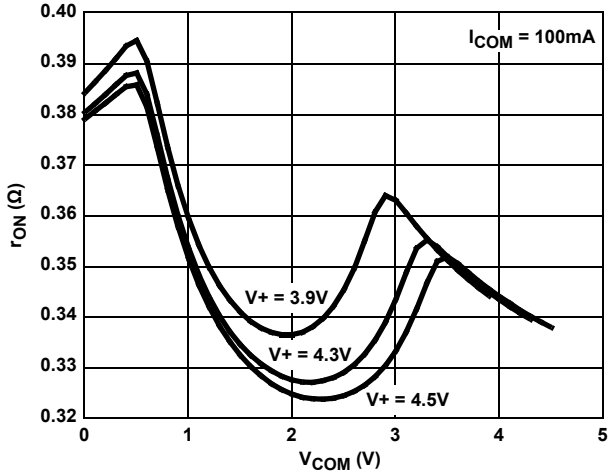


FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE
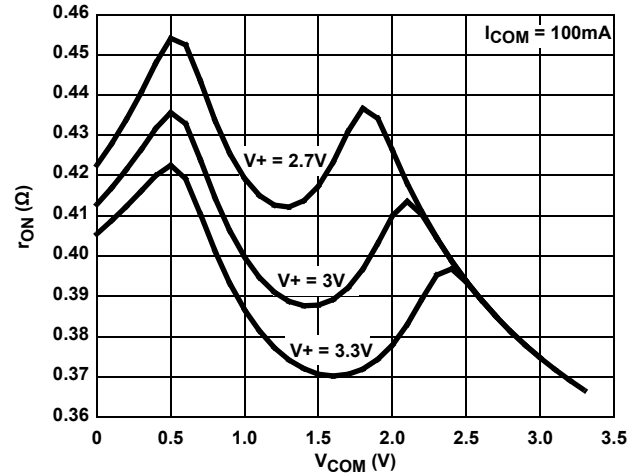
FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE
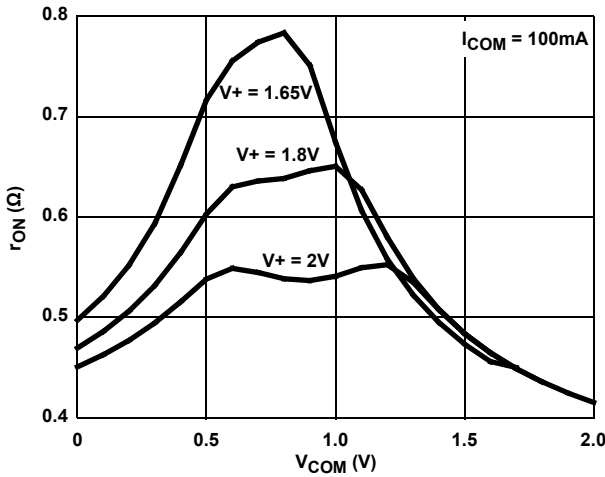
FIGURE 10. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE
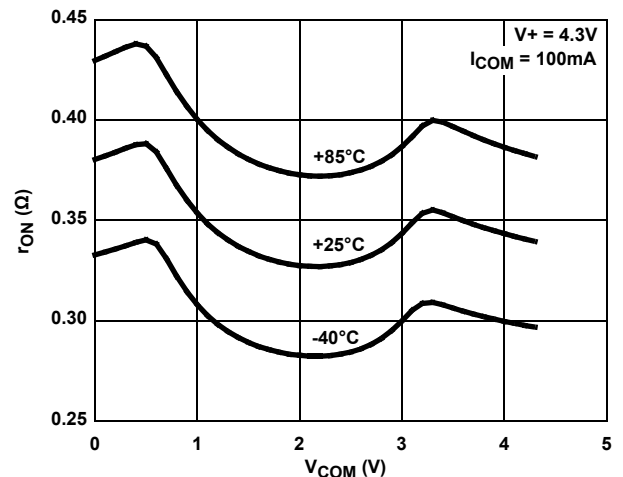
FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE
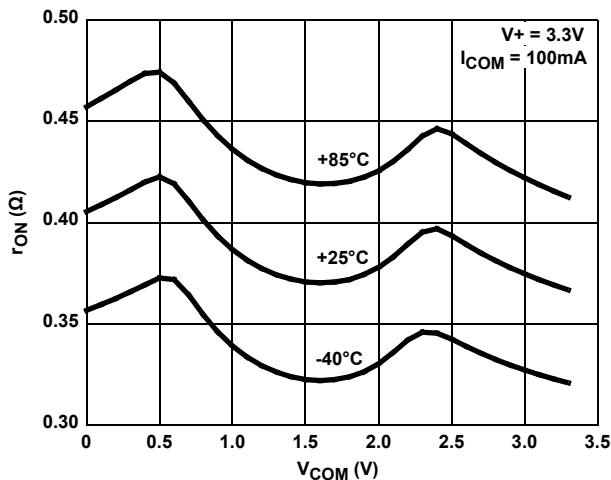
FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE
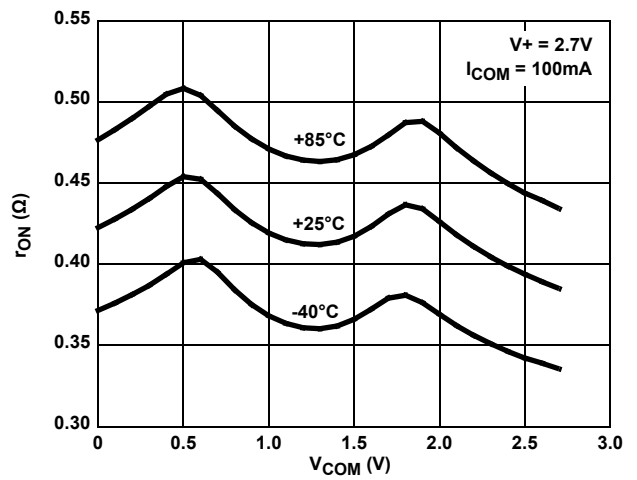
FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE

*Typical Performance Curves* $T_A$ = +25°C, unless otherwise specified. **(Continued)**
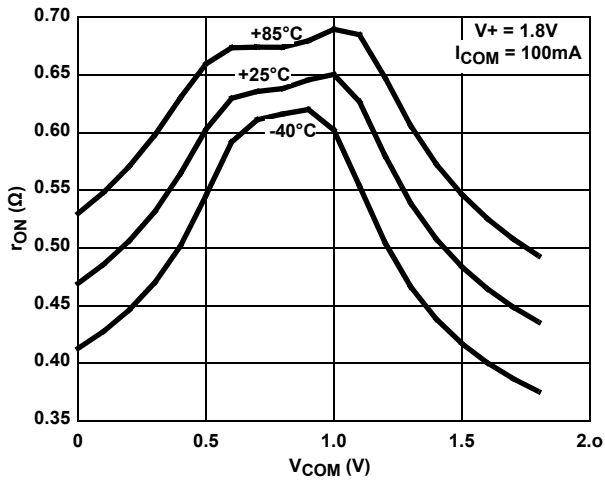


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE
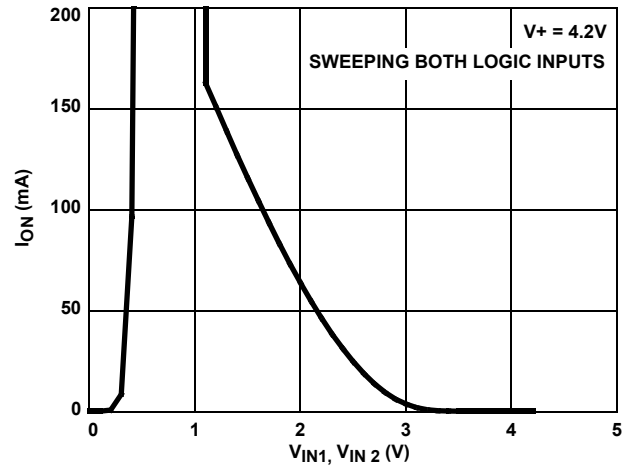


FIGURE 15. SUPPLY CURRENT vs VLOGIC VOLTAGE
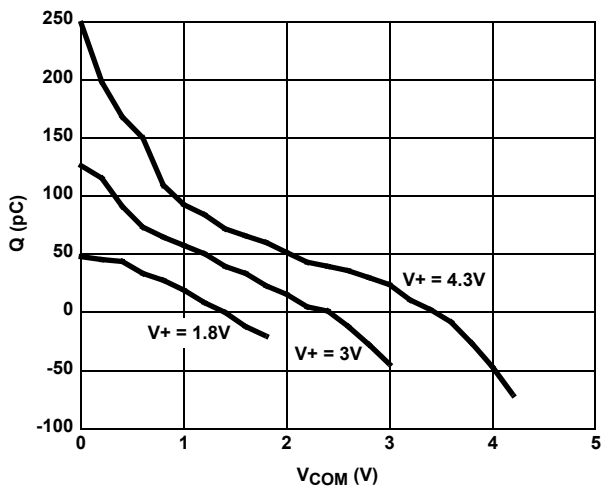


FIGURE 16. CHARGE INJECTION vs SWITCH VOLTAGE
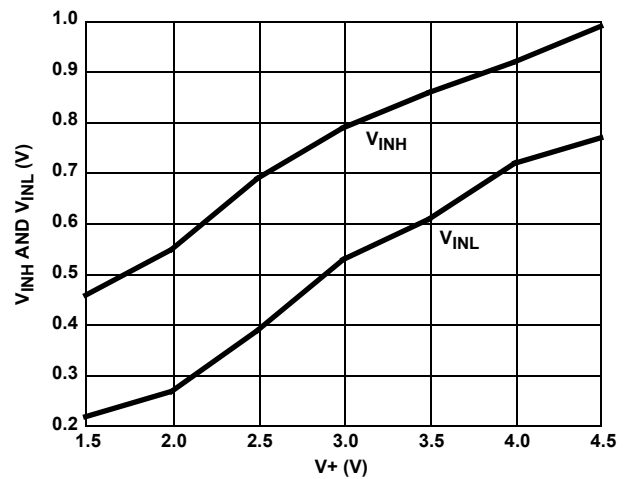


FIGURE 17. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE
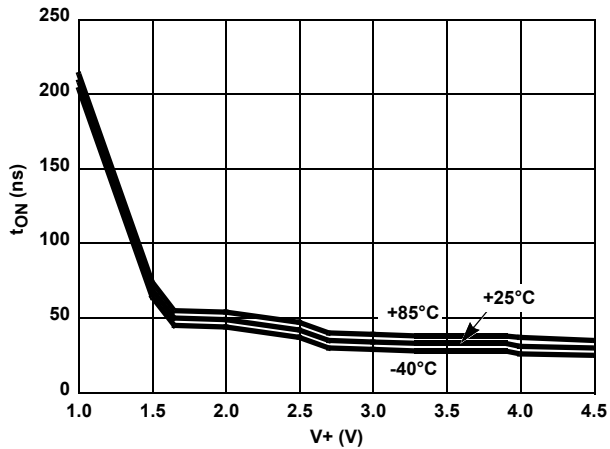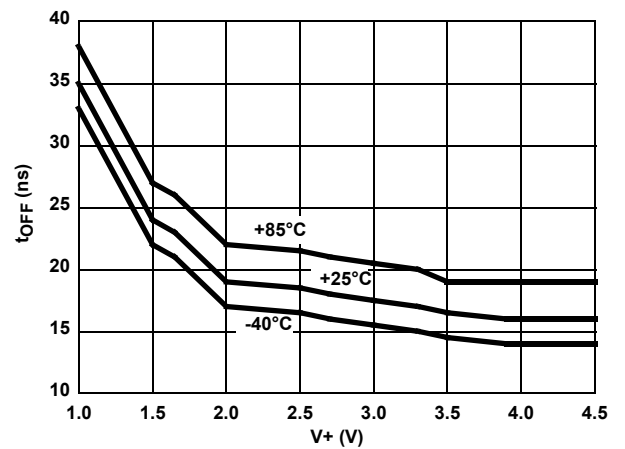


FIGURE 18. TURN-ON TIME vs SUPPLY VOLTAGE



FIGURE 19. TURN-OFF TIME vs SUPPLY VOLTAGE

## *Typical Performance Curves* $T_A$ = +25°C, unless otherwise specified. **(Continued)**
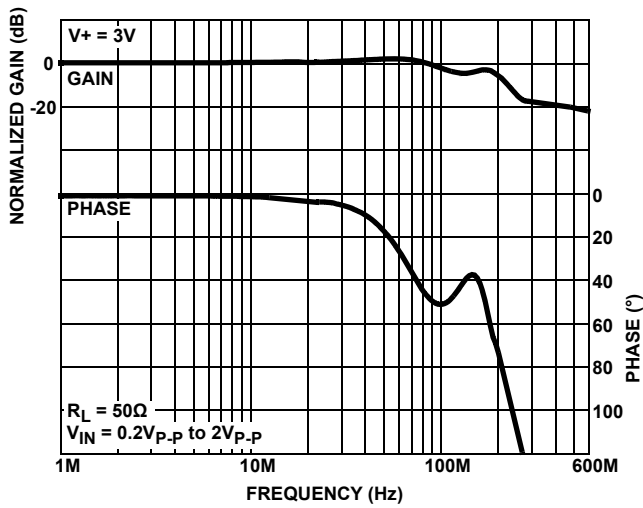

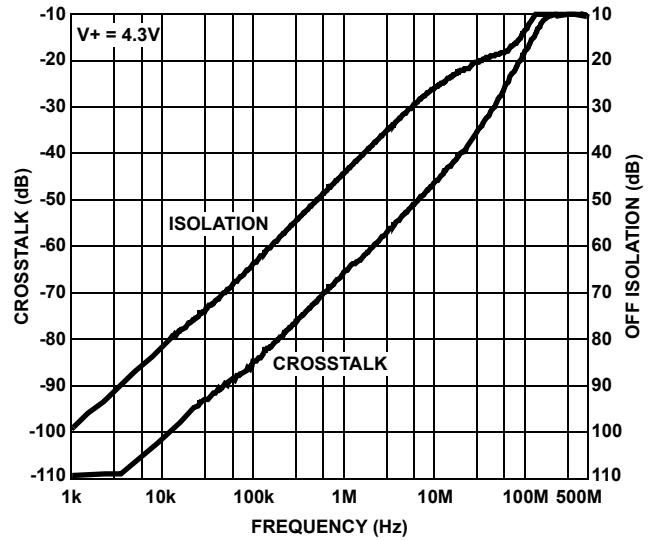
FIGURE 20.  FREQUENCY RESPONSE



FIGURE 21.  CROSSTALK AND OFF ISOLATION

## *Die Characteristics*

### SUBSTRATE POTENTIAL (POWERED UP):

GND (QFN Paddle Connection: To Ground or Float)

### TRANSISTOR COUNT:

228

### PROCESS:

Si Gate CMOS

## *Detailed Description*

The ISL84467 is a bidirectional, quad single pole/double throw (SPDT) analog switch that offers precise switching capability from a single 1.65V to 4.5V supply with low ON-resistance (0.39$\Omega$) and high speed operation ($t_{ON}$ = 33ns, $t_{OFF}$ = 16ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.65V), low power consumption (6.3$\mu$W max), low leakage currents (165nA max), and the tiny TQFN package. The ultra low ON-resistance and $r_{ON}$ flatness provide very low insertion loss and distortion to applications that require signal reproduction.

### *External V+ Series Resistor*

For improved ESD and latch-up immunity, Renesas recommends adding a 100$\Omega$ resistor in series with the V+ power supply pin of the ISL84467 IC (see Figure 22).

During an overvoltage transient event, such as occurs during system level IEC 61000 ESD testing, substrate currents can be generated in the IC that can trigger parasitic SCR structures to turn ON, creating a low impedance path from the V+ power supply to ground. This will result in a significant amount of current flow in the IC which can potentially create a latch-up state or permanently damage the IC. The external V+ resistor limits the current during this over-stress situation and has been found to prevent latch-up or destructive damage for many overvoltage transient events.

Under normal operation, the sub-microamp IDD current of the IC produces an insignificant voltage drop across the 100$\Omega$ series resistor resulting in no impact to switch operation or performance.
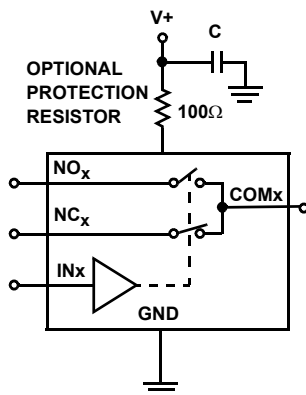


**FIGURE 22. V+ SERIES RESISTOR FOR ENHANCED ESD AND LATCH-UP IMMUNITY**

### *Supply Sequencing and Overvoltage Protection*

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 23). To prevent forward biasing these diodes, V+ must

be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provide additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1k$\Omega$ resistor in series with the logic input (see Figure 23). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low $r_{ON}$ switch. Connecting Schottky diodes to the signal pins (as shown in Figure 23) will shunt the fault current to the supply or to ground, thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current.
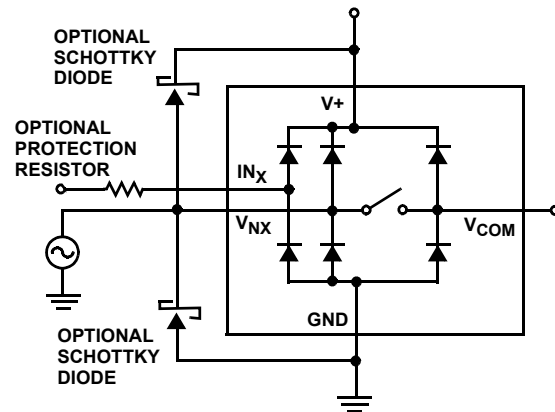


**FIGURE 23. OVERVOLTAGE PROTECTION**

### *Power-Supply Considerations*

The ISL84467 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4.7V maximum supply voltage, the ISL84467 5.5V maximum supply voltage provides plenty of room for the 10% tolerance of 4.3V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.65V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the "Electrical Specifications" tables starting on page 3 and the "Typical Performance Curves" starting on page 8 for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

### Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 3.0V to 4.5V (see Figure 17). At 3.0V the $V_{IL}$ level is about 0.53V. This is still above the 1.8V CMOS guaranteed low output maximum level of 0.5V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

The ISL84467 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example, driving the device with 2.85V logic (0V to 2.85V) while operating with a 4.2V supply the device draws only 12µA of current (see Figure 15 for $V_{IN}$ = 2.85V).

### High-Frequency Performance

In 50Ω systems, the ISL84467 has a -3dB bandwidth of 104MHz (see Figure 20). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off isolation is the resistance to this feedthrough, while crosstalk indicates the amount of feedthrough from one switch to another. Figure 21 details the high off isolation and crosstalk rejection provided by this part. At 100kHz, off isolation is about 65dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation and crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

### Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog signal path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

## *Package Outline Drawings*

For the most recent package outline drawing, see M16.173.

M16.173
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10

**TOP VIEW**

**END VIEW**

**SIDE VIEW**
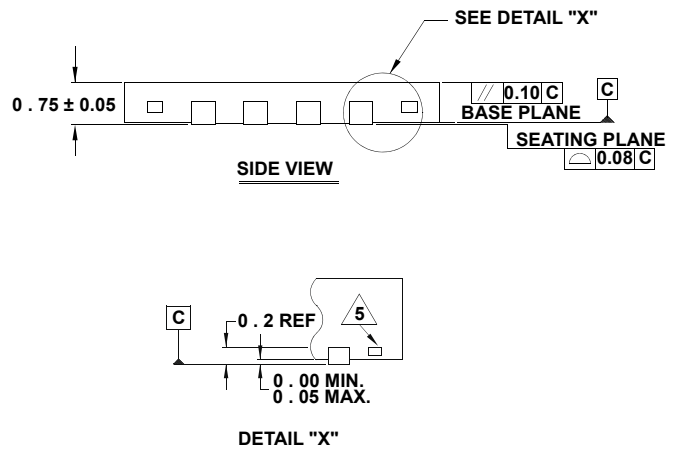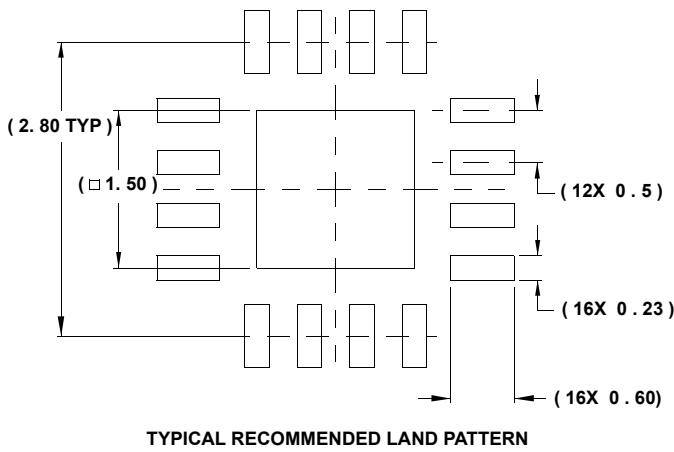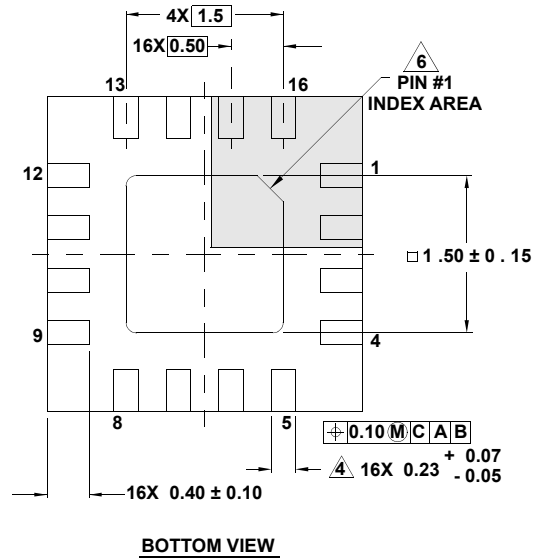
**DETAIL "X"**

**TYPICAL RECOMMENDED LAND PATTERN**
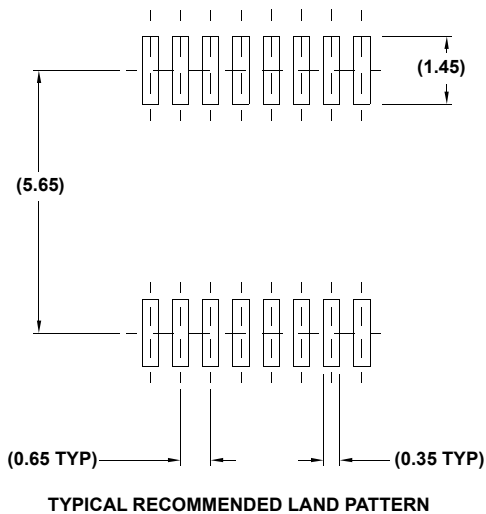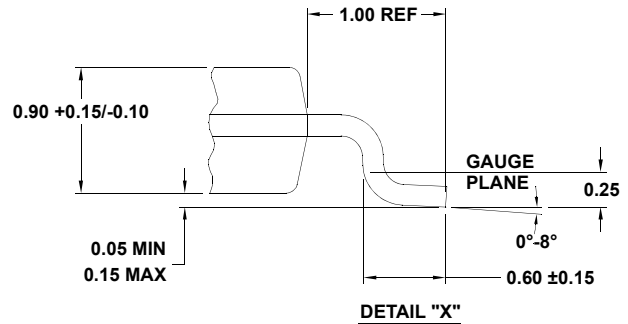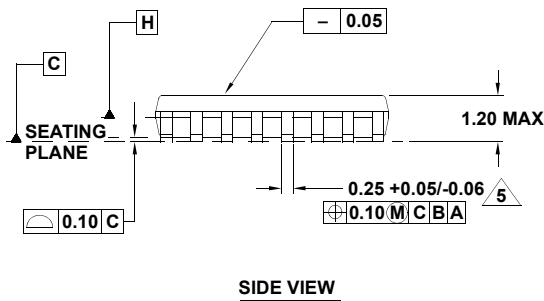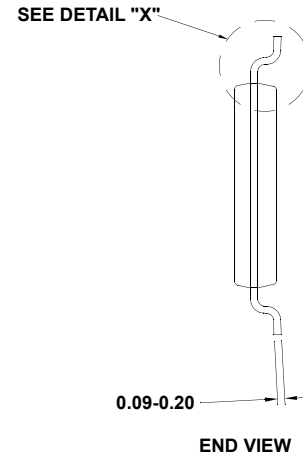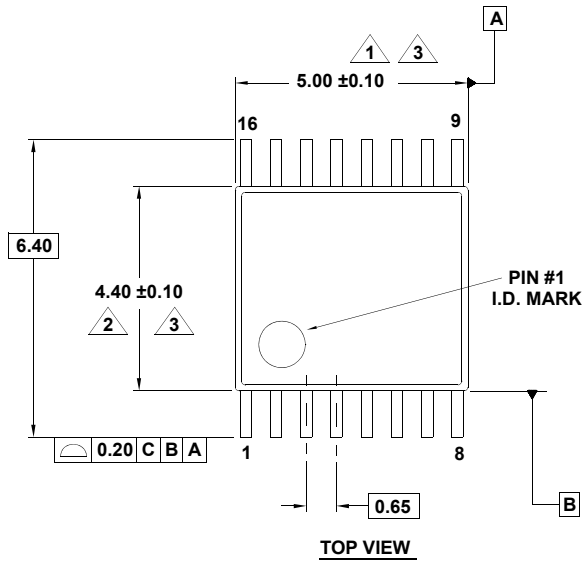
NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.

2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.

3. Dimensions are measured at datum plane H.

4. Dimensioning and tolerancing per ASME Y14.5M-1994.

5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.

6. Dimension in ( ) are for reference only.

7. Conforms to JEDEC MO-153.

For the most recent package outline drawing, see L16.3x3A.

L16.3x3A
16 Lead Thin Quad Flat No-Lead Plastic Package
Rev 1, 7/11

**TOP VIEW**

3.00

A
B

6
PIN 1
INDEX AREA

3.00

(4X) 0.15

**BOTTOM VIEW**

4X 1.5
16X 0.50

13       16

6
PIN #1
INDEX AREA

12

1

1.50 ± 0.15

9

4

8       5

0.10 M C A B

16X 0.23 + 0.07 - 0.05

4

16X 0.40 ± 0.10

**TYPICAL RECOMMENDED LAND PATTERN**

( 2.80 TYP )

( 1.50 )

( 12X 0.5 )

( 16X 0.23 )

( 16X 0.60)

**SIDE VIEW**

SEE DETAIL "X"

0.75 ± 0.05

0.10 C

BASE PLANE

C

SEATING PLANE

0.08 C

**DETAIL "X"**

C

0.2 REF

5

0.00 MIN.
0.05 MAX.
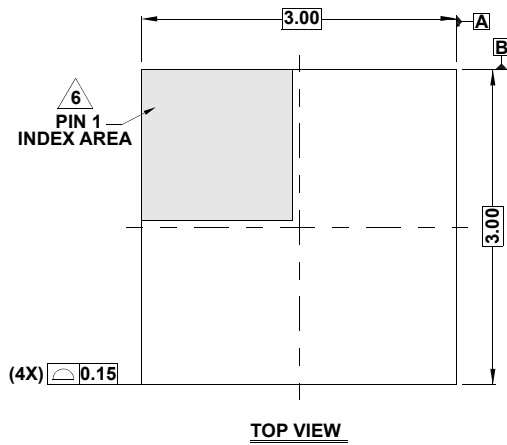
NOTES:

1. Dimensions are in millimeters.
   Dimensions in (   ) for Reference Only.

2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

3. Unless otherwise specified, tolerance: Decimal ± 0.05

4. Dimension applies to the metallized terminal and is measured
   between 0.15mm and 0.30mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be
   located within the zone indicated. The pin #1 identifier may be
   either a mold or mark feature.

RENESAS

## *Revision History*

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| REVISION | DATE | CHANGE |
|----------|------|--------|
| 2.00 | Dec 18, 2025 | Added Revision History section.<br>Updated Ordering Information table.<br>Updated POD M16.173 to the latest version; changes are as follows:<br>- Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.<br>Updated POD L16.3X3A to the latest version; changes are as follows:<br>- Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. |
| 1.00 | Jul 23, 2008 | Added TSSOP package and note 10 to RON. |
| 0.00 | Jul 17, 2007 | Initial release |

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Koto-ku, Tokyo 135-0061, Japan
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