NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL8200AM

# ISL8200M

Complete Current Share 10A DC/DC Power Module

FN6727
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The ISL8200M is a simple and easy to use high power, current-sharing DC\DC power module for Datacom\Telecom\ FPGA power hungry applications. All that is needed is the ISL8200M, a few passive components and one $V_{OUT}$ setting resistor to have a complete 10A design ready for market.

The ease of use virtually eliminates the design and manufacturing risks while dramatically improving time to market.

Need more output current? Parallel up to six ISL8200M modules to scale up to a 60A solution (see Figure 6 on page 10).

The simplicity of the ISL8200M is in its "Off The Shelf", unassisted implementation versus a discrete implementation. Patented current sharing in multi-phase operation greatly reduces ripple currents, BOM cost and complexity. For example, parallel 2 for 20A and up to 6 for 60A. The output voltage can be precisely regulated to as low as 0.6V with ±1% output voltage regulation over line, load, and temperature variations.

The ISL8200M's thermally enhanced, compact QFN package, operates at full load and over temperature, without requiring forced air cooling. It's so thin it can even fit on the back side of the PCB. Easy access to all pins with few external components, reduces the PCB design to a component layer and a simple ground layer.

## Features

- Complete switch mode power supply in one package
- Patented current share architecture reduces layout sensitivity when modules are paralleled
- Programmable phase shift (1- to 6-phase)
- Extremely low profile (2.2mm height)
- Input voltage range +4.5V to +20V at 10A, current share up to 60A
- A single resistor sets $V_{OUT}$ from +0.6V to +6V
- Output overvoltage, overcurrent and over-temperature protection and undervoltage indication
- RoHS compliant

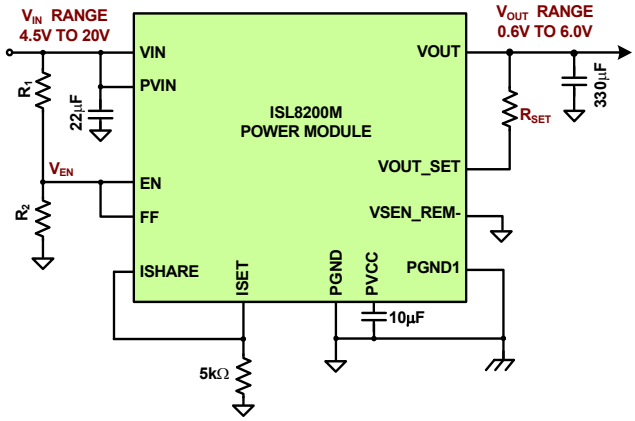
## Applications

- Servers, Telecom and Datacom applications
- Industrial and medical equipment
- Point of load regulation

## Related Literature

- AN1655 ISL8200MEVAL1PHZ Evaluation Board User's Guide
- iSim Model - (See Product Information page at www.intersil.com/products/ISL8200M
- AN1786 Reducing the Switching Frequency of the ISL8200M and ISL8200AM Power Modules

## Complete Functional Schematic




**NOTE:** For input voltage higher than 4.5V, $V_{IN}$ can be tied to $P_{VIN}$ directly (see Figure 22 for details).

**FIGURE 1. COMPLETE 10A DESIGN, JUST SELECT $R_{SET}$ FOR THE DESIRED $V_{OUT}$**

## ISL8200M Package

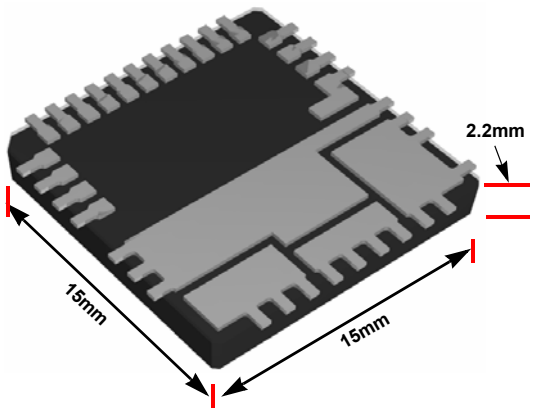



**FIGURE 2. THE 2.2mm HEIGHT IS IDEAL FOR THE BACKSIDE OF PCBS WHEN SPACE AND HEIGHT IS A PREMIUM**

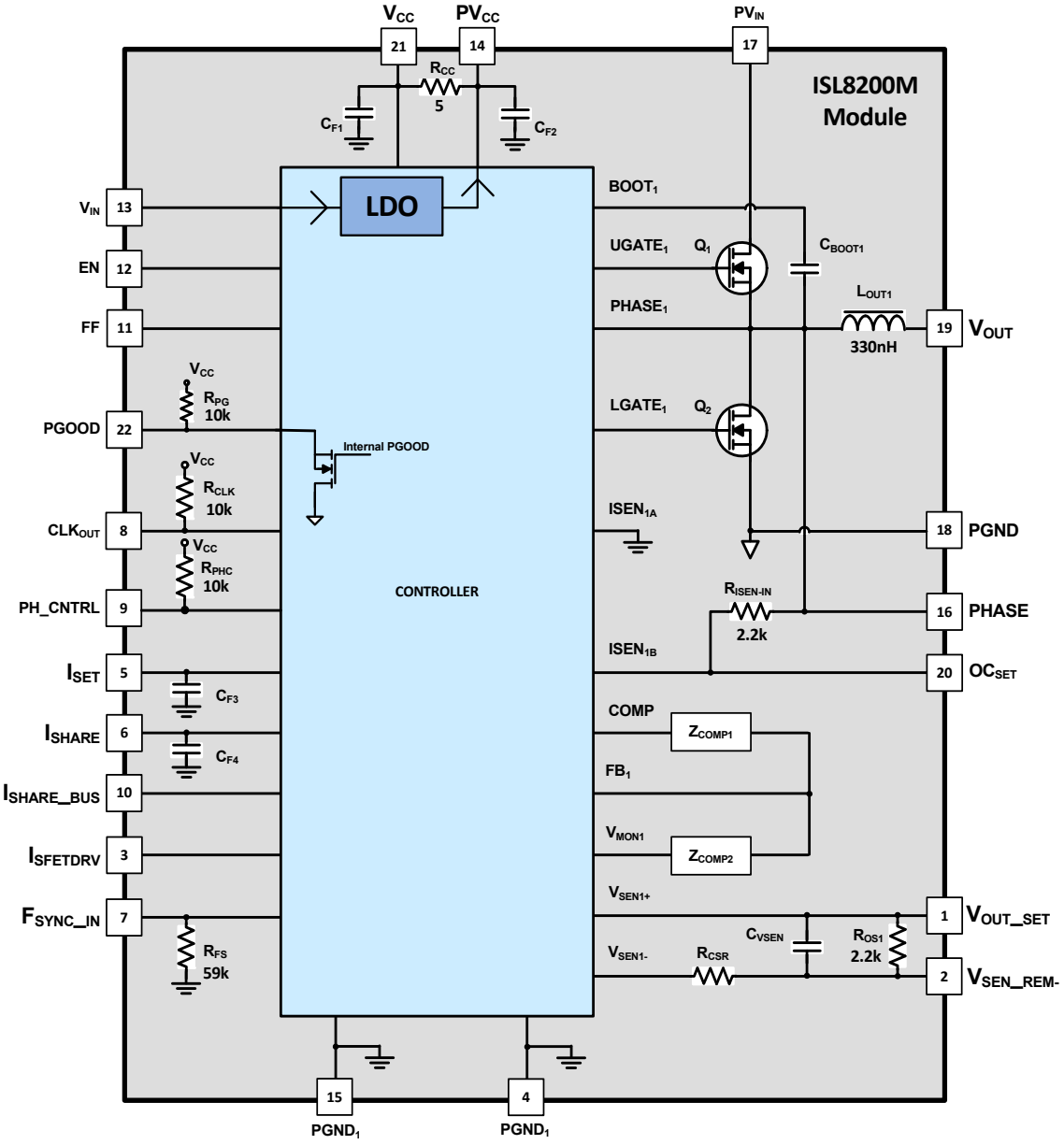
# Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|
| ISL8200MIRZ | ISL8200M | -40 to +85 | 23 Ld QFN | L23.15x15 |
| ISL8200MEVAL1PHZ | Evaluation Board | | | |

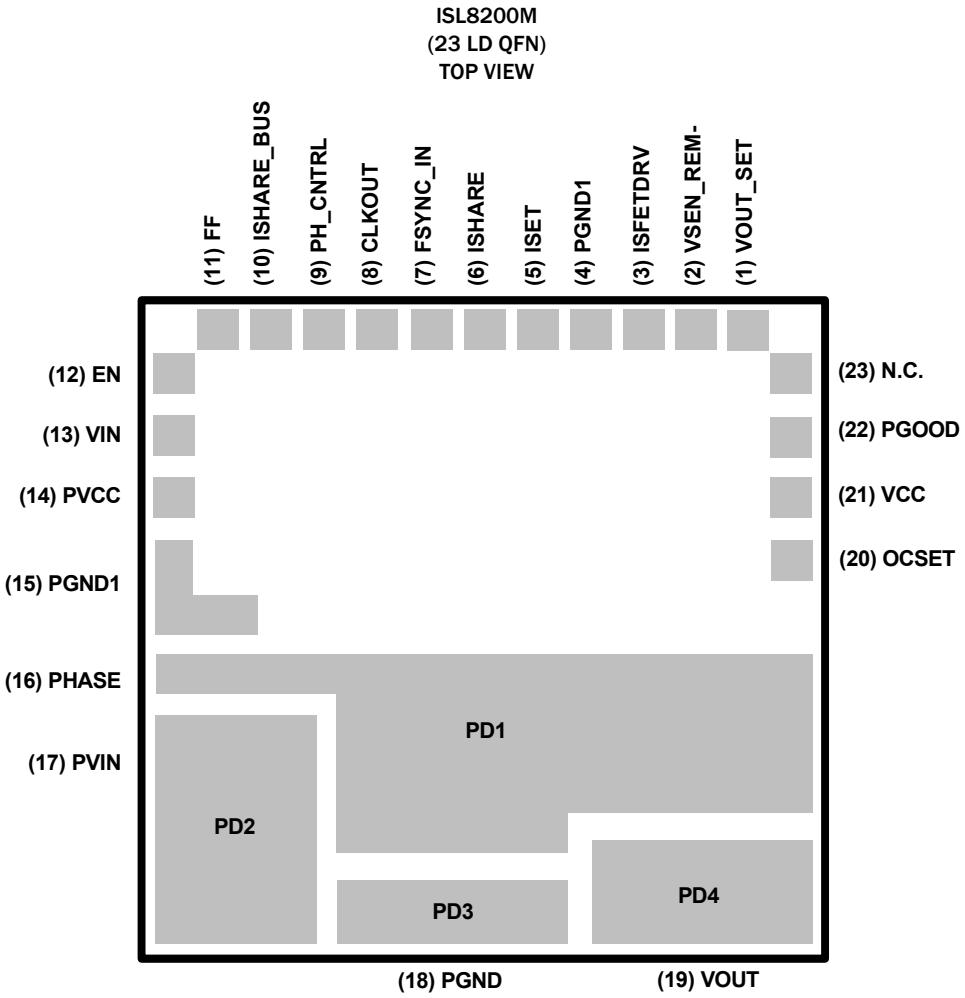
NOTES:

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil plastic packaged products employ special material sets, molding compounds and 100% matte tin plate plus anneal (e3) termination finish, These products do contain Pb but they are RoHs compliant by exemption 5 (Pb in piezoelectric elements). These Intersil RoHs compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8200M. For more information on MSL please see techbrief TB363.

# Pinout Internal Circuit



# Pin Configuration




# Pin Descriptions

| PIN # | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| 1 | VOUT_SET | Analog Voltage Input - Used with $V_{OUT}$ to program the regulator output voltage. The typical input impedance of VOUT_SET with respect to VSEN_REM- is 600kΩ. The typical input voltage is 0.6V. |
| 2 | VSEN_REM- | Analog Voltage Input - This pin is the negative input of standard unity gain operational amplifier for differential remote sense for the regulator, and should connect to the negative rail of the load/processor. This pin can be used for $V_{OUT}$ trimming by connecting a resistor from this pin to the VOUT_SET pin. |
| 3 | ISFETDRV | Digital Output - This pin is used to drive an optional NFET, which will connect ISHARE with the system ISHARE bus upon completing a pre-bias startup. The output voltage range is 0V to 5V. |
| 4, 15 | PGND1 | Normal Ground - All voltage levels are referenced to this pad. This pad provides a return path for the low side MOSFET drives and internal power circuitries as well as all analog signals. PGND and PGND1 should be connected together with a ground plane. |
| 5 | ISET | Analog Current Output - This pin, along with the ISHARE pin, is used for multiple ISL8200M current sharing purposes. This pin sources a 15µA offset current plus Channel 1's average current. The voltage (VISET) set by an external resistor (RISET) represents the average current level of the local active module. For full-scale current, RISET should be ~10kΩ. The output current range is 15µA to 123µA typ. In the single module configuration, this pin can be tied to the ISHARE pin. |

## Pin Descriptions (Continued)

| PIN # | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| 6 | ISHARE | Analog Current Output - Cascaded system level overcurrent shutdown pin. This pin is used where you have multiple modules configured for current sharing and is used with a common current share bus. The bus sums each of the modules' average current contribution to the load to protect for an overcurrent condition at the load. The pin sources 15µA plus average module's output current. The shared bus voltage ($V_{ISHARE}$) is developed across an external resistor ($R_{ISHARE}$). $V_{ISHARE}$ represents the average current of all active channel(s) that are connected together.<br>The ISHARE bus voltage is compared with each module's internal reference voltage set by each module's $R_{ISET}$ resistor. This will generate an individual current share error signal in each cascaded controller. The share bus impedance $R_{ISHARE}$ should be set as $R_{ISET}$/NCTRL, $R_{ISET}$ divided by the number of active current sharing controllers. The output current from this pin generates a voltage across the external resistor. This voltage, $V_{ISHARE}$, is compared to an internal 1.2V threshold for average overcurrent protection. For full-scale current, $R_{ISHARE}$ should be ~10kΩ. Typically 10kΩ is used for $R_{SHARE}$ and $R_{SET}$. The output current range is 15µA to 123µA typ. |
| 7 | FSYNC_IN | Analog Input Control Pin - An optional external resistor (RFS-ext) connected to this pin and ground will increase the oscillator switching frequency. It has an internal 59kΩ resistor for a default frequency of 700kHz. The internal oscillator will lock to an external frequency source when connected to a square waveform. The external source is typically the CLKOUT signal from another ISL8200M or an external clock. The internal oscillator synchronizes with the leading positive edge of the input signal. The input voltage range from an external source is a 0V to 5V square wave. When not synchronized to an external clock, a 100pF capacitor between FSYNC_IN and PGND1 is recommended. |
| 8 | CLKOUT | Digital Voltage Output - This pin provides a clock signal to synchronize with other ISL8200M(s). When there is more than one ISL8200M in the system, the two independent regulators can be programmed via PH_CNTRL for different degrees of phase delay. |
| 9 | PH_CNTRL | Analog Input - The voltage level on this pin is used to program the phase shift of the CLKOUT clock signal to synchronize with other module(s). |
| 10 | ISHARE_BUS | Open pin until first PWM pulse is generated. Then, via an internal FET, this pin connects the module's ISHARE to the system's ISHARE bus after pre-bias is complete and soft-start is initiated. |
| 11 | FF | Analog Voltage Input - The voltage on this pin is fed into the controller, adjusting the sawtooth amplitude to generate the feed-forward function. The input voltage range is 0.8V to $V_{CC}$. Typically, FF is connected to EN. |
| 12 | EN | This is a double function pin: Analog Input Voltage - The input voltage to this pin is compared with a precision 0.8V reference and enables the digital soft-start. The input voltage range is 0V to $V_{CC}$ or $V_{IN}$ through a pull-up resistor maintaining a typical current of 5mA.<br>Analog Voltage Output - This pin can be used as a voltage monitor for input bus undervoltage lockout. The hysteresis levels of the lockout can be programmed via this pin using a resistor divider network. Furthermore, during fault conditions (such as overvoltage, overcurrent, and over-temperature), this pin is used to communicate the information to other cascaded modules by pulling low the wired OR as it is an Open Drain. The output voltage range is 0V to $V_{CC}$. |
| 13 | VIN | Analog Voltage Input - This pin should be tied directly to the input rail when using the internal linear regulator. It provides power to the internal linear drive circuitry. When used with an external 5V supply, this pin should be tied directly to PVCC. The internal linear device is protected against the reversed bias generated by the remaining charge of the decoupling capacitor at VCC when losing the input rail. The input voltage range is 4.5V to 20V. |
| 14 | PVCC | Analog Output - This pin is the output of the internal series linear regulator. It provides the bias for both low-side and high-side drives. Its operational voltage range is 4.5V to 5.6V. The decoupling ceramic capacitor in the PVCC pin is 10µF. |
| 16 | PHASE | Analog Output - This pin is the phase node of the regulator. The output voltage range is 0V to 30V. |
| 17 | PVIN | Analog Input - This input voltage is applied to the power FETs with the FET's ground being the PGND pin. It is recommended to place input decoupling capacitance, 22µF, directly between the PVIN pin and the PGND pin, as close as possible to the module. The input voltage range is 3V to 20V. |
| 18 | PGND | All voltage levels are referenced to this pad. This is the low side MOSFET ground. PGND and PGND1 should be connected together with a ground plane. |
| 19 | VOUT | Output voltage from the module. The output voltage range is 0.6V to 6V. |
| 20 | OCSET | Analog Input - This pin is used with the PHASE pin to set the current limit of the module. The input voltage range is 0V to 30V. |
| 21 | VCC | Analog Input - This pin provides bias power for the analog circuitry. It's operational range is 4.5V to 5.6V. In 3.3V applications, VCC, PVCC and VIN should be shorted to allow operation at the low end input as it relates to the $V_{CC}$ falling threshold limit. This pin can be powered either by the internal linear regulator or by an external voltage source. |
| 22 | PGOOD | Analog Output - This pin, pulled up to VCC via an internal 10kΩ resistor, provides a Power Good signal when the output is within 9% of nominal output regulation point with 4% hysteresis (13%/9%), and soft-start is complete. An external pull-up is not required. PGOOD monitors the outputs (VMON1) of the internal differential amplifiers. The output voltage range is 0V to $V_{CC}$. |

## Pin Descriptions (Continued)

| PIN # | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| 23 | NC | Not internal connected |
| PD1 | Phase Thermal Pad | Used for both the PHASE pin (Pin # 16) and for heat removal connecting to heat dissipation layers using Vias. Connect this pad to a copper island on the PCB board with the same shape as the PHASE thermal pad. This pad is electrically connected to the PHASE pin. |
| PD2 | $PV_{IN}$ Thermal Pad | Used for both the PVIN pin (Pin # 17) and for heat removal connecting to heat dissipation layers using Vias. Connect this pad to a copper island on the PCB board with the same shape as the $PV_{IN}$ thermal pad. This pad is electrically connected to the PVIN pin. |
| PD3 | PGND Thermal Pad | Used for both the PGND pin (Pin # 18) and for heat removal connecting to heat dissipation layers using Vias. Connect this pad to a copper island on the PCB board with the same shape as the PGND thermal pad. This pad is electrically connected to the PGND pin. |
| PD4 | $V_{OUT}$ Thermal Pad | Used for both the VOUT pin (Pin # 19) and for heat removal connecting to heat dissipation layers using Vias. Connect this pad to a copper island on the PCB board with the same shape as the $V_{OUT}$ thermal pad.Tthis pad is electrically connected to the VOUT pin. |

## Typical Application Circuits

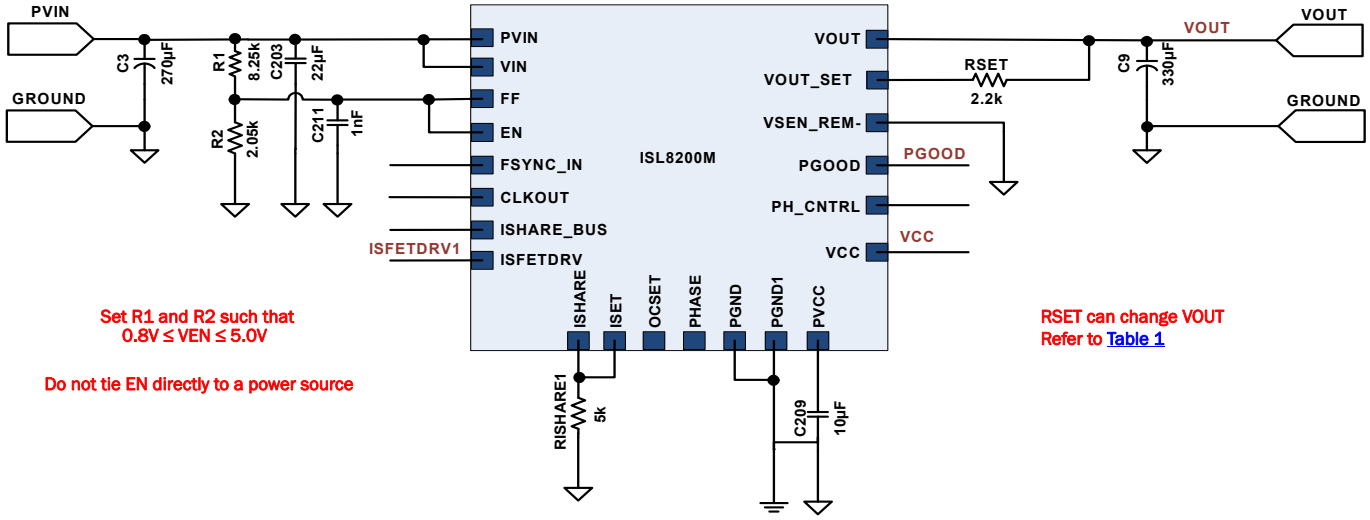
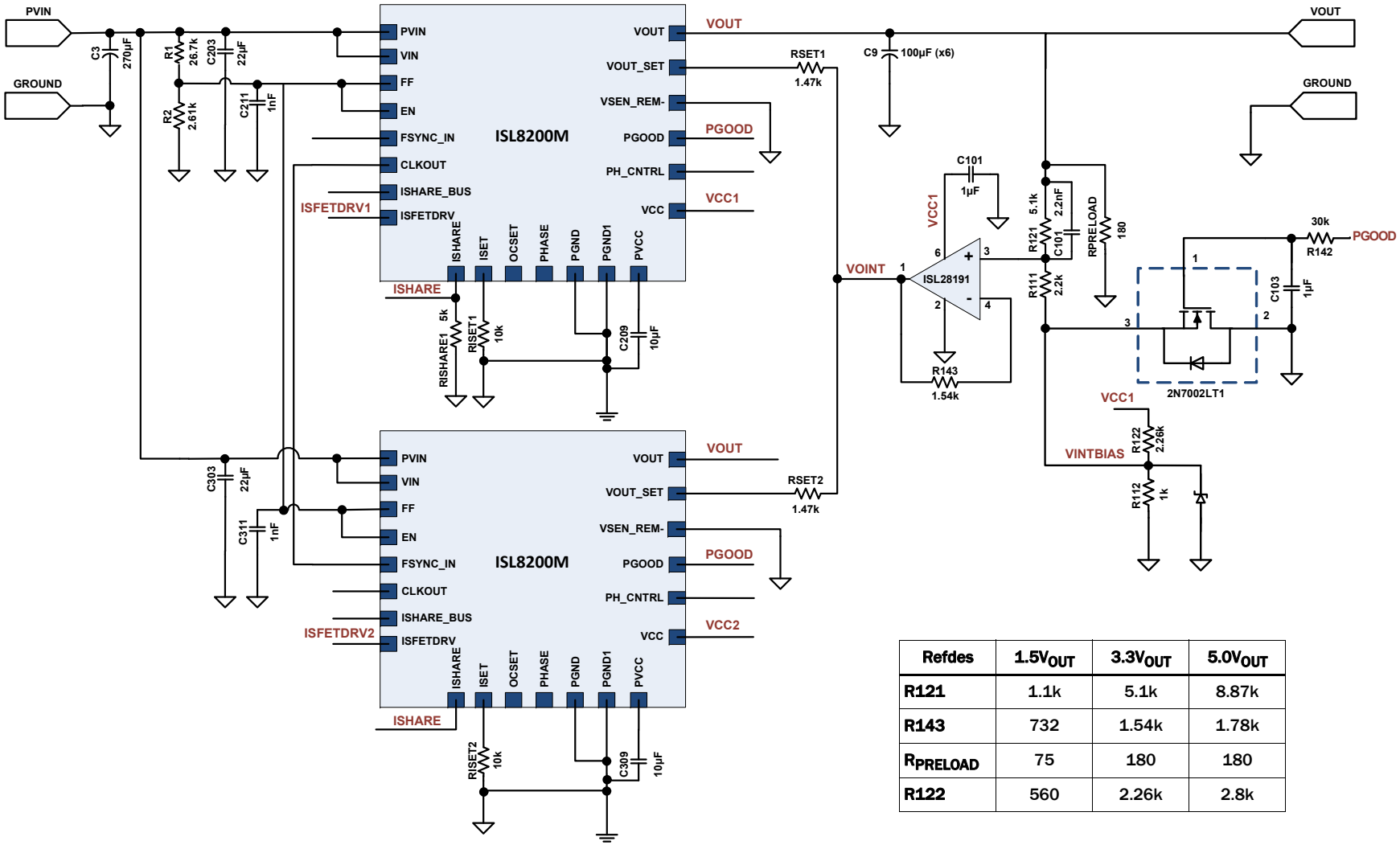



FIGURE 3. SINGLE PHASE 10A 1.2V OUTPUT CIRCUIT

# Typical Application Circuits (continued)




| Refdes | 1.5V$_{OUT}$ | 3.3V$_{OUT}$ | 5.0V$_{OUT}$ |
|---|---|---|---|
| R121 | 1.1k | 5.1k | 8.87k |
| R143 | 732 | 1.54k | 1.78k |
| R$_{PRELOAD}$ | 75 | 180 | 180 |
| R122 | 560 | 2.26k | 2.8k |

FIGURE 4. TWO PHASE 20A 3.3V OUTPUT CIRCUIT

## Absolute Maximum Ratings

Input Voltage, PVIN, $V_{IN}$ . . . . . -0.3V to +27V
Driver Bias Voltage, PVCC . . . . . -0.3V to +6.5V
Signal Bias Voltage, $V_{CC}$ . . . . . -0.3V to +6.5V
BOOT/UGATE Voltage, $V_{BOOT}$ . . . . . -0.3V to +36V
Phase Voltage, $V_{PHASE}$ . . . . . $V_{BOOT}$ - 7V to $V_{BOOT}$ + 0.3V
BOOT to PHASE Voltage,
$V_{BOOT}$ - $V_{PHASE}$ . . . . . -0.3V to $V_{CC}$ + 0.3V
Input, Output or I/O Voltage . . . . . -0.3V to $V_{CC}$ + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114E) . . . . . 2kV
Machine Model (Tested per JESD22-A115-A) . . . . . 200V
Charge Device Model (Tested per JESD22-C101C) . . . . . 1kV
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . . . 100mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| QFN Package (Notes 4, 5) | 13 | 2.0 |

Maximum Storage Temperature Range . . . . . -40°C to +150°C
Pb-Free Reflow Profile . . . . . see Figure 40

## Recommended Operating Conditions

Input Voltage, $V_{IN}$ . . . . . 4.5V to 20V
Input Voltage, PVIN . . . . . 3V to 20V
Driver Bias Voltage, PVCC . . . . . 4.5V to 5.6V
Signal Bias Voltage, $V_{CC}$ . . . . . 4.5V to 5.6V
Boot to Phase Voltage
$V_{BOOT}$ - $V_{PHASE}$ . . . . . <6V
Industrial Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +125°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board (i.e., 4-layer type without thermal vias - see tech brief TB379) per JEDEC standards except that the top and bottom layers assume solid plains.
5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

**Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP (Note 6) | MAX | UNITS |
|---|---|---|---|---|---|---|
| **VCC SUPPLY CURRENT** | | | | | | |
| Nominal Supply $V_{IN}$ Current | $I_{Q\_VIN}$ | PVIN = $V_{IN}$ = 20V; No Load; $F_{SW}$ = 700kHz | | 36 | | mA |
| Nominal Supply $V_{IN}$ Current | $I_{Q\_VIN}$ | PVIN = $V_{IN}$ = 4.5V; No Load; $F_{SW}$ = 700kHz | | 27 | | mA |
| Shutdown Supply $V_{CC}$ Current | $I_{VCC}$ | EN = 0V, $V_{CC}$ = 2.97V | | 9 | | mA |
| **INTERNAL LINEAR REGULATOR** | | | | | | |
| Maximum Current | $I_{PVCC}$ | PVCC = 4V | | 320 | | mA |
| Saturated Equivalent Impedance | $R_{LDO}$ | P-Channel MOSFET ($V_{IN}$ = 5V) | | 1 | | Ω |
| PVCC Voltage Level (Note 7) | PVCC | $I_{PVCC}$ = 0mA, $V_{IN}$ = 12V | **5.15** | 5.4 | **5.95** | V |
| **POWER-ON RESET** (Note 7) | | | | | | |
| Rising VCC Threshold | | | | 2.85 | **2.97** | V |
| Falling VCC Threshold | | | | 2.65 | **2.75** | V |
| Rising PVCC Threshold | | | | 2.85 | **3.05** | V |
| Falling PVCC Threshold | | | | 2.65 | **2.75** | V |
| System Soft-start Delay | $t_{SS\_DLY}$ | After PLL, $V_{CC}$, and PVCC PORs, and EN above their thresholds | | 384 | | Cycles |
| **ENABLE** (Note 7) | | | | | | |
| Turn-On Threshold Voltage | | | **0.75** | 0.8 | **0.86** | V |
| Hysteresis Sink Current | $I_{EN\_HYS}$ | | **23** | 30 | **35** | µA |
| Undervoltage Lockout Hysteresis | $V_{EN\_HYS}$ | $V_{EN\_RTH}$ = 10.6V; $V_{EN\_FTH}$ = 9V<br>$R_{UP}$ = 53.6kΩ, $R_{DOWN}$ = 5.23kΩ | | 1.6 | | V |
| Sink Current | $I_{EN\_SINK}$ | $V_{EN}$ = 1V | 15.4 | | | mA |
| Sink Impedance | $R_{EN\_SINK}$ | $V_{EN}$ = 1V | | | **64** | Ω |
| **OSCILLATOR** | | | | | | |
| Oscillator Frequency | FOSC | $R_{FS}$ = 59kΩ; Figure 33 | | 700 | | kHz |
| Total Variation (Note 7) | | $V_{CC}$ = 5V; -40°C < $T_A$ < +85°C | **-9** | | **+9** | % |

## Electrical Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP (Note 6) | MAX | UNITS |
|---|---|---|---|---|---|---|
| **FREQUENCY SYNCHRONIZATION AND PHASE LOCK LOOP** (Note 7) | | | | | | |
| Synchronization Frequency | | $V_{CC}$ = 5V | FOSC | | **1500** | kHz |
| PLL Locking Time | | $V_{CC}$ = 5.4V; $F_{SW}$ = 700kHz | | 210 | | µs |
| Input Signal Duty Cycle Range | | | 10 | | 90 | % |
| **PWM** (Note 7) | | | | | | |
| Minimum PWM OFF Time | $t_{MIN\_OFF}$ | | **310** | 345 | **410** | ns |
| Current Sampling Blanking Time | $t_{BLANKING}$ | | | 175 | | ns |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Continuous Current Range | $I_{OUT(DC)}$ | PVIN = $V_{IN}$ = 12V, $V_{OUT}$ = 1.2V | 0 | | 10 | A |
| Line Regulation Accuracy | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{OUT}$ = 1.2V, $I_{OUT}$ = 0A, PVIN = $V_{IN}$ = 3.5V to 20V | | 0.15 | | % |
| | | $V_{OUT}$ = 1.2V, $I_{OUT}$ = 10A, PVIN = $V_{IN}$ = 5V to 20V | | 0.15 | | % |
| Load Regulation Accuracy | $\Delta V_{OUT}/\Delta I_{OUT}$ | $I_{OUT}$ = 0A to 10A, $V_{OUT}$ = 1.2V, PVIN = $V_{IN}$ = 12V | | 0.1 | | % |
| Output Ripple Voltage | $\Delta V_{OUT}$ | $I_{OUT}$ = 10A, $V_{OUT}$ = 1.2V, PVIN = $V_{IN}$ = 12V | | 27 | | $mV_{P-P}$ |
| | | $I_{OUT}$ = 0A, $V_{OUT}$ = 1.2V, PVIN = $V_{IN}$ = 12V | | 19 | | $mV_{P-P}$ |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Voltage Change For Positive Load Step | $\Delta V_{OUT-DP}$ | $I_{OUT}$ = 0A to 5A. Current slew rate = 2.5A/µs, PVIN = $V_{IN}$ = 12V, $V_{OUT}$ = 1.2V | | 45 | | $mV_{P-P}$ |
| Voltage Change For Negative Load Step | $\Delta V_{OUT-DN}$ | $I_{OUT}$ = 5A to 0A. Current slew rate = 2.5A/µs, PVIN = $V_{IN}$ = 12V, $V_{OUT}$ = 1.2V | | 55 | | $mV_{P-P}$ |
| **REFERENCE** (Note 7) | | | | | | |
| Reference Voltage (Include Error and Differential Amplifiers' Offsets) | $V_{REF1}$ | ISL8200MIRZ, $T_A$ = -40°C to +85°C | | 0.6 | | V |
| | | | **-0.7** | | **0.7** | % |
| **DIFFERENTIAL AMPLIFIER** (Note 7) | | | | | | |
| DC Gain | UG_DA | Unity Gain Amplifier | | 0 | | dB |
| Unity Gain Bandwidth | UGBW_DA | | | 5 | | MHz |
| $V_{SEN+}$ Pins Input Current | $I_{VSEN+}$ | | 0.2 | 1 | 2.5 | µA |
| Maximum Source Current for Current Sharing | $I_{VSEN1-}$ | VSEN1- Source Current for Current Sharing when parallel multiple modules each of which has its own voltage loop | | 350 | | µA |
| Input Impedance | $R_{VSEN+\_to\_VSEN-}$ | $V_{VSEN+}/I_{VSEN+}$, $V_{VSEN+}$ = 0.6V | | -600 | | kΩ |
| Output Voltage Swing | | | 0 | | $V_{CC}$ - 1.8 | V |
| Input Common Mode Range | | | -0.2 | | $V_{CC}$ - 1.8 | V |
| Disable Threshold | $V_{VSEN-}$ | $V_{MON1}$ = Tri-State | | $V_{CC}$ - 0.4 | | V |
| **OVERCURRENT PROTECTION** (Note 7) | | | | | | |
| Channel Overcurrent Limit | $I_{SOURCE}$ | $V_{CC}$ = 2.97V to 5.6V | | 108 | | µA |
| Channel Overcurrent Limit | $I_{SOURCE}$ | $V_{CC}$ = 5V | **89** | 108 | **122** | µA |
| Share Pin OC Threshold | $V_{OC\_ISHARE}$ | Comparator offset included | **1.16** | 1.20 | **1.22** | V |
| **CURRENT SHARE** | | | | | | |
| External Current Share Accuracy | | Up to 3 phases | | ±10 | | % |
| **POWER GOOD MONITOR** (Note 7) | | | | | | |
| Undervoltage Falling Trip Point | $V_{UVF}$ | Percentage Below Reference Point | **-15** | -13 | **-11** | % |
| Undervoltage Rising Hysteresis | $V_{UVR\_HYS}$ | Percentage Above UV Trip Point | | 4 | | % |
| Overvoltage Rising Trip Point | $V_{OVR}$ | Percentage Above Reference Point | **11** | 13 | **15** | % |

## Electrical Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP (Note 6) | MAX | UNITS |
|---|---|---|---|---|---|---|
| Overvoltage Falling Hysteresis | $V_{OVF\_HYS}$ | Percentage below OV Trip Point | | 4 | | % |
| PGOOD Low Output Voltage | | $I_{PGOOD}$ = 2mA | | | **0.35** | V |
| Sinking Impedance | | $I_{PGOOD}$ = 2mA | | | **70** | Ω |
| Maximum Sinking Current | | $V_{PGOOD}$ < 0.8V | | 10 | | mA |
| **OVERVOLTAGE PROTECTION** (Note 7) | | | | | | |
| OV Latching Trip Point | | EN= UGATE = LATCH Low, LGATE = High | **118** | 120 | **122** | % |
| OV Non-Latching Trip Point | | EN = Low, UGATE = Low, LGATE = High | | 113 | | % |
| LGATE Release Trip Point | | EN = Low/High, UGATE = Low, LGATE = Low | | 87 | | % |
| **OVER-TEMPERATURE PROTECTION CONTROLLER JUNCTION TEMPERATURE** | | | | | | |
| Over-Temperature Trip | | Controller junction temperature | | 150 | | °C |
| Over-Temperature Release Threshold | | Controller junction temperature | | 125 | | °C |
| **INTERNAL COMPONENT VALUES** | | | | | | |
| Internal Resistor Between PVCC and VCC Pin | $R_{CC}$ | | | 5 | | Ω |
| Internal Resistor Between PHASE and OCSET Pins | $R_{ISEN-IN}$ | | | 2.2k | | Ω |
| Internal Resistor Between FSYNC_IN and PGND1 Pins | $R_{FS}$ | | | 59k | | Ω |
| Internal Resistor Between PGOOD and VCC Pins | $R_{PG}$ | | | 10k | | Ω |
| Internal Resistor Between CLKOUT and VCC Pins | $R_{CLK}$ | | | 10k | | Ω |
| Internal Resistor Between PH_CNTRL and VCC Pins | $R_{PHC}$ | | | 10k | | Ω |
| Internal Resistor Between VOUT_SET and VSEN_REM- Pin | $R_{OS1}$ | | | 2.2k | | Ω |

NOTES:

6. Parameters with TYP limits are not production tested, unless otherwise specified.
7. Parameters with MIN and/or MAX limits are 100% tested for internal IC prior to module assembly, unless otherwise specified. Temperature limits established by characterization and are not production tested.

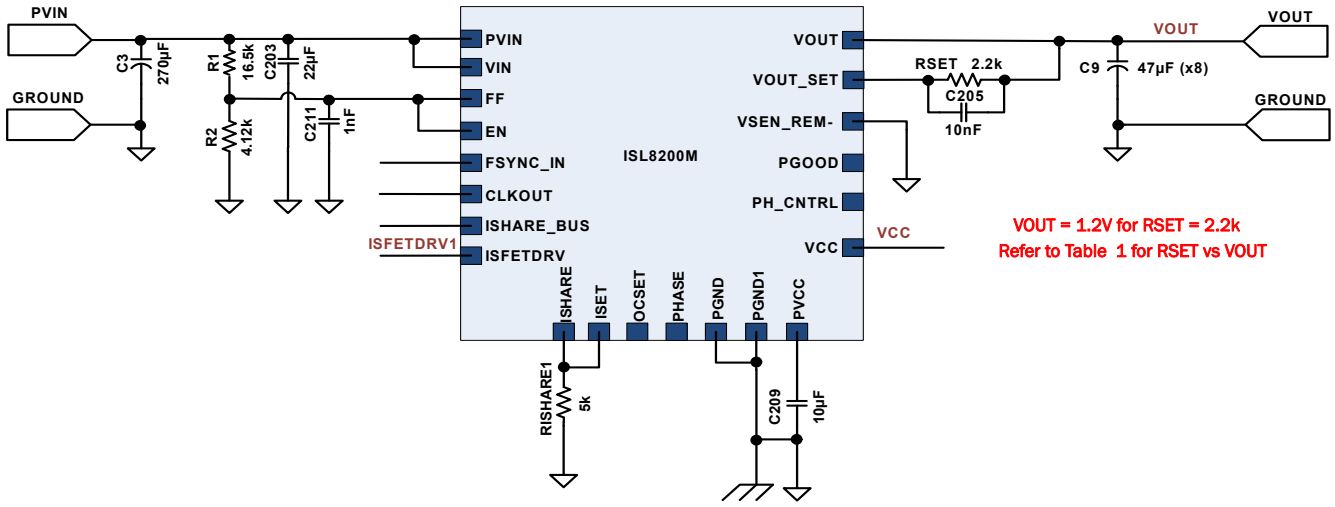



FIGURE 5. TEST CIRCUIT FOR ALL PERFORMANCE AND DERATING GRAPHS

# Typical Performance Characteristics

## Efficiency Performance

$T_A$ = +25°C, $PV_{IN}$ = $V_{IN}$, $C_{IN}$ = 220µFx1, 10µF/Ceramic x 2, $C_{OUT}$ = 47µF/Ceramic x 8.

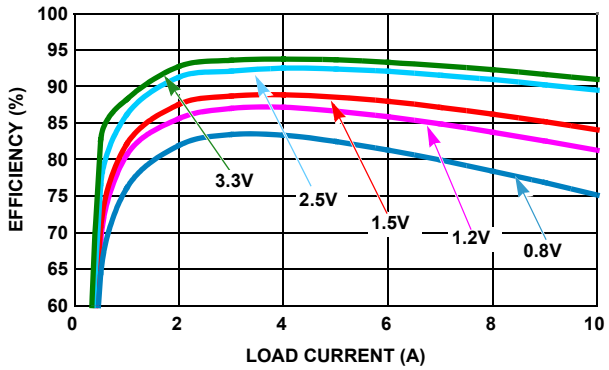



FIGURE 6. EFFICIENCY vs LOAD CURRENT ($5V_{IN}$)

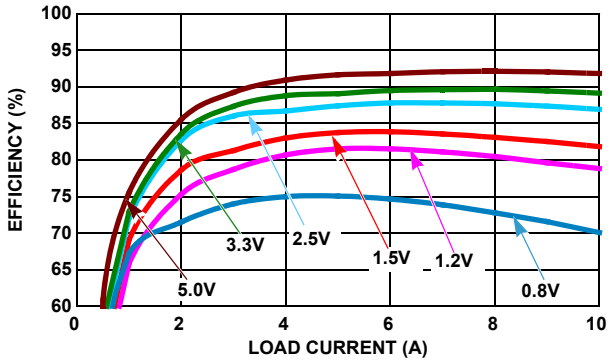



FIGURE 7. EFFICIENCY vs LOAD CURRENT ($12V_{IN}$)

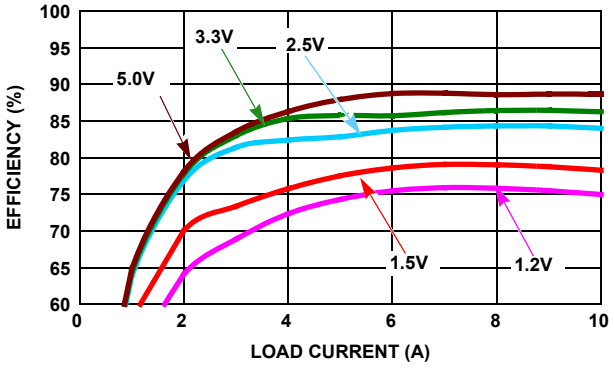



FIGURE 8. EFFICIENCY vs LOAD CURRENT ($20V_{IN}$)

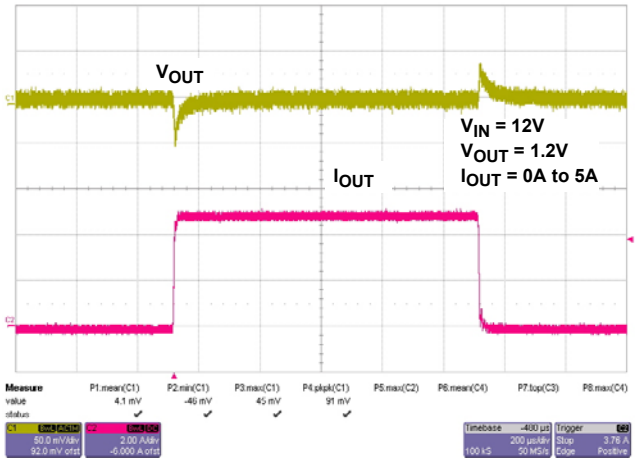



FIGURE 9. 1.2V TRANSIENT RESPONSE

# Typical Performance Characteristics (Continued)

## Transient Response Performance

$T_A$ = +25°C, $PV_{IN}$ = $V_{IN}$ = 12V, $C_{IN}$ = 220µFx1, 10µF/Ceramic x 2, $C_{OUT}$ = 47µF/Ceramic x 8
$I_{OUT}$ = 0A to 5A, Current slew rate = 2.5A/µs

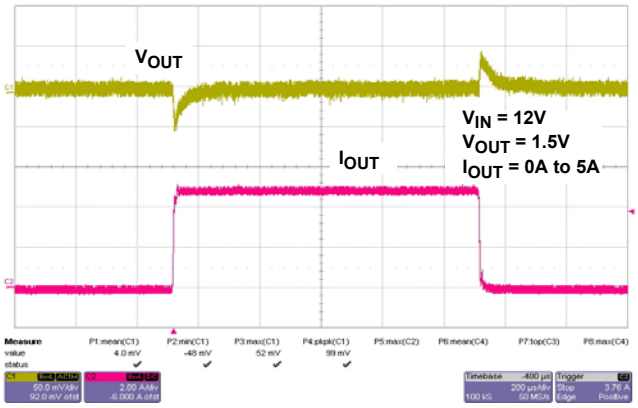



FIGURE 10. 1.5V TRANSIENT RESPONSE

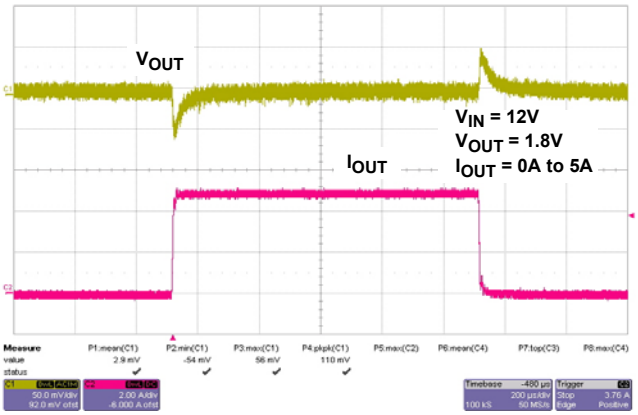



FIGURE 11. 1.8V TRANSIENT RESPONSE

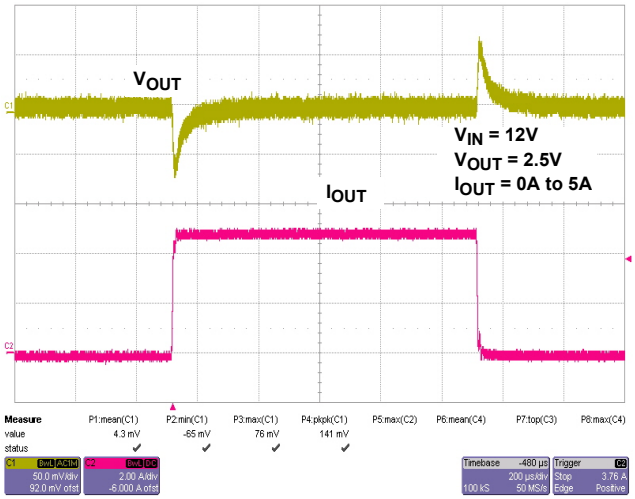



FIGURE 12. 2.5V TRANSIENT RESPONSE

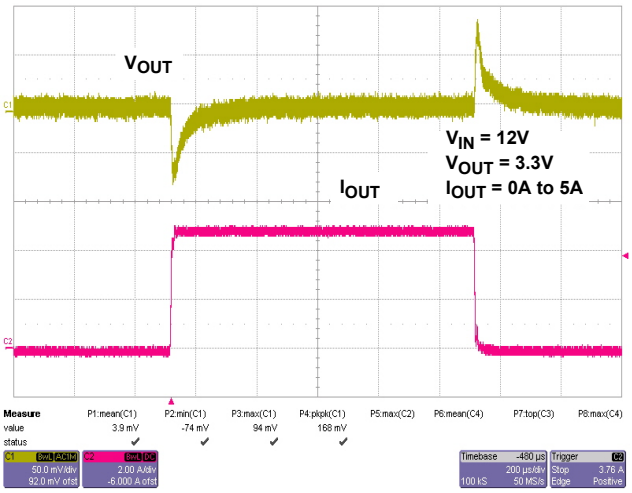



FIGURE 13. 3.3V TRANSIENT RESPONSE

# Typical Performance Characteristics (Continued)

## Output Ripple Performance

$T_A$ = +25°C, $PV_{IN}$ = $V_{IN}$ = 12V, $C_{IN}$ = 220µFx1, 10µF/Ceramic x 2, $C_{OUT}$ = 47µF/Ceramic x 8 $I_{OUT}$ = No Load, 5, 10A

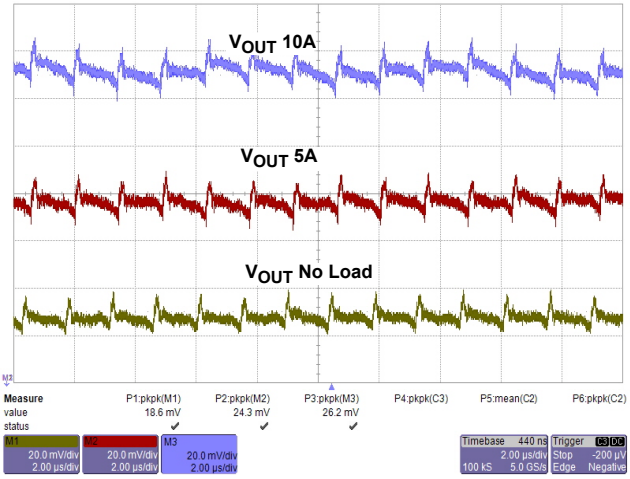



FIGURE 14. 1.2V OUTPUT RIPPLE

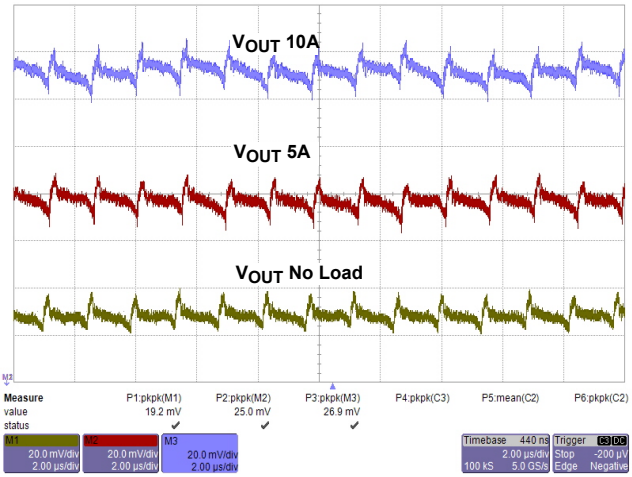



FIGURE 15. 1.5V OUTPUT RIPPLE

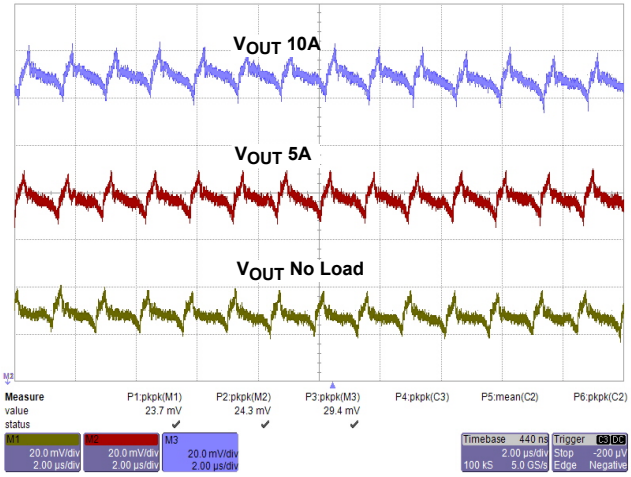



FIGURE 16. 2.5V OUTPUT RIPPLE

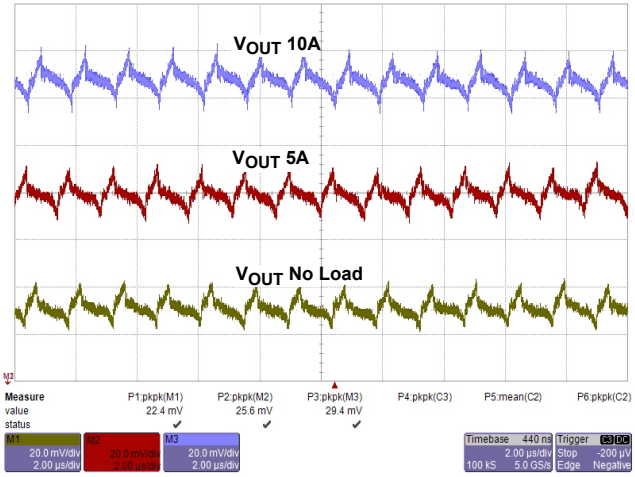



FIGURE 17. 3.3V OUTPUT RIPPLE

# Typical Performance Curves

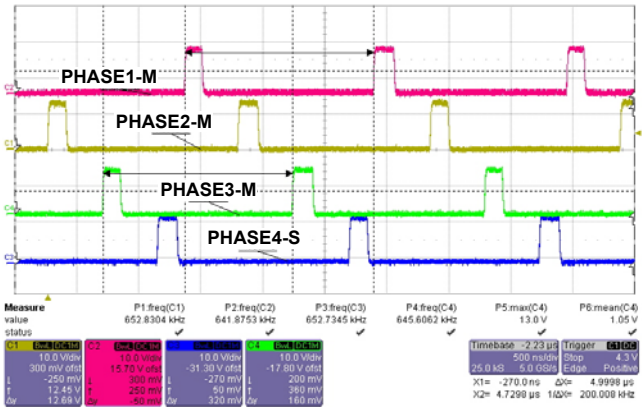



FIGURE 18. FOUR MODULE CLOCK SYNC ($V_{IN}$ = 12V)

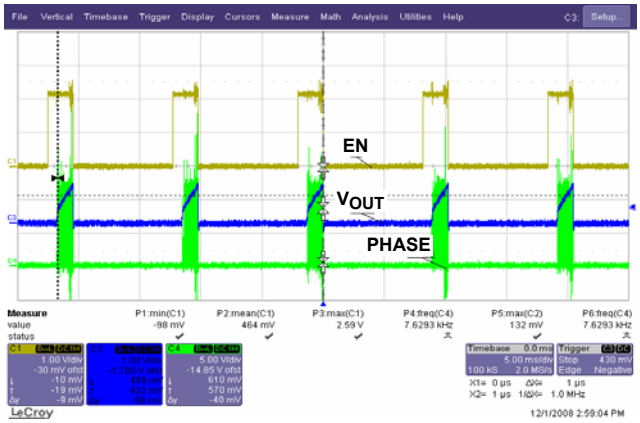



FIGURE 19. OVERCURRENT PROTECTION

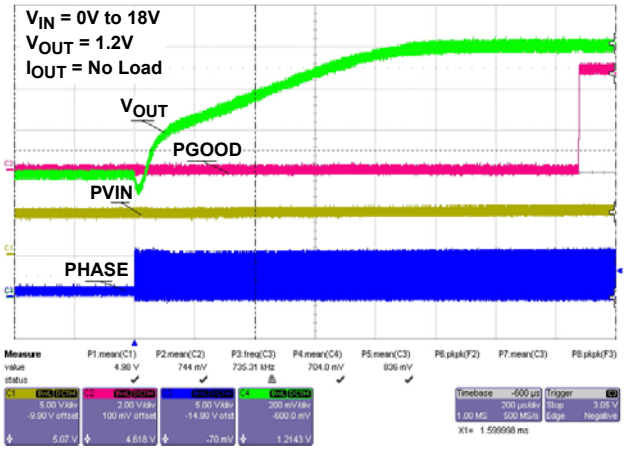



FIGURE 20. 50% PRE-BIAS START-UP

# Applications Information

## Programming the Output Voltage ($R_{SET}$)

The ISL8200M has an internal 0.6V ± 0.7% reference voltage. Programming the output voltage requires a dividing resistor ($R_{SET}$) between VOUT_SET pin and $V_{OUT}$ regulation point. The output voltage can be calculated as shown in Equation 1:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{SET}}{R_{OS}}\right) \quad \text{(EQ. 1)}$$

Note: ISL8200M has integrated 2.2kΩ resistances into the module dividing resistor for bottom side ($R_{OS}$). The resistances for different output voltages in single phase operation are listed in Table 1.

TABLE 1. $V_{OUT}$ - $R_{SET}$

| $V_{OUT}$ | 0.6V | 0.8V | 1.0V | 1.2V |
|---|---|---|---|---|
| $R_{SET}$ | 0Ω | 732Ω | 1.47kΩ | 2.2kΩ |

| $V_{OUT}$ | 1.5V | 1.8V | 2.0V | 2.5V |
|---|---|---|---|---|
| $R_{SET}$ | 3.32kΩ | 4.42kΩ | 5.11kΩ | 6.98kΩ |

| $V_{OUT}$ | 3.3V | 5.0V | 6.0V |
|---|---|---|---|
| $R_{SET}$ | 10kΩ | 16.2kΩ | 20kΩ |

The output voltage accuracy can be improved by maintaining the impedance at $V_{OUTSET}$ (internal $V_{SEN1+}$) at or below 1kΩ effective impedance. Note: the impedance between $V_{SEN1+}$ and $V_{SEN1-}$ is about 600kΩ.

The module has a minimum input voltage at a given output voltage, which needs to be a minimum of 1.43 times output voltage if operating at $F_{SW}$ = 700kHz switching frequency. This is due to the Minimum PWM OFF Time ($t_{MIN-OFF}$).

The equation to determine the minimum $PV_{IN}$ to support the required $V_{OUT}$ is given by Equations 2 and 3; it is recommended to add 0.5V to the result to account for temperature variations.

$$PV_{IN\_MIN} = \frac{V_{OUT} \times t_{SW}}{t_{SW} - t_{MIN\_OFF}} \quad \text{(EQ. 2)}$$

$t_{SW}$ = switching period = $1/F_{SW}$

for the 700kHz switching frequency = 1428ns

$$PV_{IN\_MIN} = 1.43 \times V_{OUT} \quad \text{(EQ. 3)}$$

For 3.3V input voltage operation, the VIN voltage is recommended to be 5V for sufficient gate drive voltage. This can be accomplished by using a voltage greater than or equal to 5V on VIN, or directly connecting the 5V source to both VIN and PVCC.

VIN is the input to the internal LDO that powers the control circuitry while PVCC is the output of the aforementioned LDO. PVIN is the power input to the power stage. Figure 21 shows a scenario where the power stage is running at 3.3V and the control circuitry is running at 5.0V; keep in mind that the PVCC pin is also at 5.0V to ensure that the LDO is not functioning. Figure 22 shows a setup where both the control circuitry and the power stage is at a 5.0V rail. It is imperative to not cross 5.5V in this setup as that is the voltage limit on the PVCC pin. Figure 23 is a more general setup and can accommodate VIN ranges up to 20V; PVCC is not tied to VIN and hence the control circuitry is powered by the internal LDO.

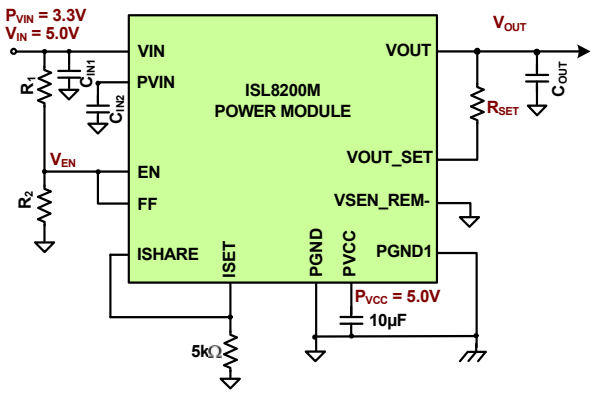



FIGURE 21. 3.3V OPERATION

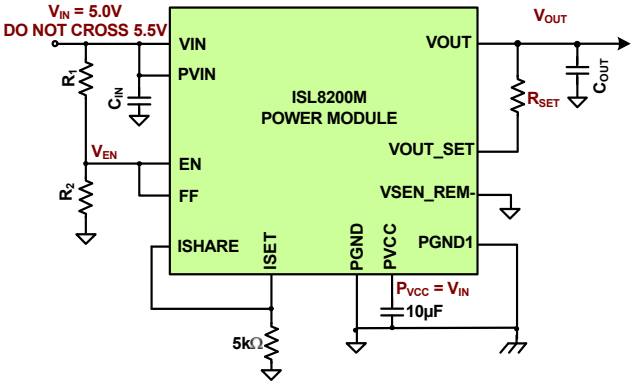



FIGURE 22. 5.0V OPERATION

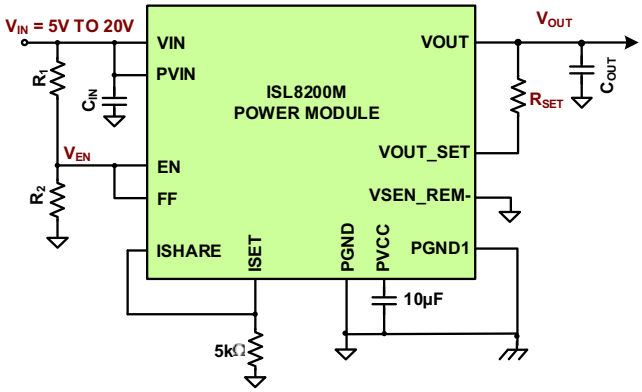



FIGURE 23. 5V TO 20V OPERATION

## Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, but consideration should be taken for the higher surge current during power-up. The ISL8200M provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by Equation 4:

$$C_{IN(MIN)} = I_O \bullet \frac{D \bullet (1 - D)}{V_{P\text{-}P(MAX)} \bullet F_S} \quad \text{(EQ. 4)}$$

Where:

$C_{IN(MIN)}$ is the minimum input capacitance (µF) required

$I_O$ is the output current (A)

D is the duty cycle ($V_O/V_{IN}$)

$V_{P\text{-}P(MAX)}$ is the maximum peak to peak voltage (V)

$F_S$ is the switching frequency (Hz)

In addition to the bulk capacitance, some low Equivalent Series Inductance (ESL) ceramic capacitance is recommended to decouple between the drain terminal of the high side MOSFET and the source terminal of the low side MOSFET. This is used to reduce the voltage ringing created by the switching current across parasitic circuit elements.

## Output Capacitors

The ISL8200M is designed for low output voltage ripple. The output voltage ripple and transient requirements can be met with bulk output capacitors ($C_{OUT}$) with low enough Equivalent Series Resistance (ESR); the recommended ESR is <10mΩ. When the total ESR is below 4mΩ, a capacitor ($C_{FF}$) between 2.2nF to 10nF is recommended; $C_{FF}$ is placed in parallel with RSET, in between the VOUT and VOUT_SET pin. $C_{OUT}$ can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical capacitance is 330µF and decoupled ceramic output capacitors are used per phase. The internally optimized loop compensation provides sufficient stability margins for all ceramic capacitor applications with a recommended total value of 300µF per phase. Additional output filtering may be needed if further reduction of output ripple or dynamic transient spike is required.

# Functional Description

## Initialization

The ISL8200M requires $V_{CC}$ and PVCC to be biased by a single supply. Power-On Reset (POR) circuits continually monitor the bias voltages (PVCC and $V_{CC}$) and the voltage at EN pin. The POR function initiates soft-start operation 384 clock cycles after the EN pin voltage is pulled to be above 0.8V, all input supplies exceed their POR thresholds and the PLL locking time expires. The enable pin can be used as a voltage monitor and to set desired hysteresis with an internal 30µA sinking current going through an external resistor divider. The sinking current is disengaged after the system is enabled. This feature is especially designed for applications that require higher input rail POR for better undervoltage protection. For example, in 12V applications, $R_{UP}$ = 53.6k and $R_{DOWN}$ = 5.23k will set the turn-on threshold ($V_{EN\_RTH}$) to 10.6V and turn-off threshold ($V_{EN\_FTH}$) to 9V, with 1.6V hysteresis ($V_{EN\_HYS}$). These numbers are explained in Figure 28 on page 16.

During shutdown or fault conditions, the soft-start is quickly reset while UGATE and LGATE immediately change state (<100ns) upon the input dropping below POR.

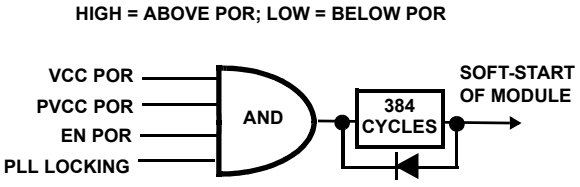



FIGURE 24. SOFT-START INITIALIZATION LOGIC

## Soft-start

The ISL8200M has an internal digital pre-charged soft-start circuitry, which has a rise time inversely proportional to the switching frequency and is determined by a digital counter that increments with every pulse of the phase clock. The full soft-start time from 0V to 0.6V can be estimated by Equation 5.

$$t_{SS} = \frac{2560}{f_{SW}} \quad \text{(EQ. 5)}$$

The ISL8200M has the ability to work under a pre-charged output. The PWM outputs will not be fed to the drivers until the first PWM pulse is seen. The low-side MOSFET is held low for the first clock cycle to provide charge for the bootstrap capacitor. If the pre-charged output voltage is greater than the final target level but less than the 113% setpoint, switching will not start until the output voltage is reduced to the target voltage and the first PWM pulse is generated. The maximum allowable pre-charged level is 113%. If the pre-charged level is above 113% but below 120%, the output will hiccup between 113% (LGATE turns on) and 87% (LGATE turns off) while EN is pulled low. If the pre-charged load voltage is above 120% of the targeted output voltage, then the controller will be latched off and not be able to power-up.

## Voltage Feed-forward

The voltage applied to the FF pin is fed to adjust the sawtooth amplitude of the channel. The amplitude the sawtooth is set to 1.25 times the corresponding FF voltage when the module is enabled. This configuration helps to maintain a constant gain ($G_M = V_{IN} \bullet D_{MAX}/\Delta V_{RAMP}$) and input voltage to achieve optimum loop response over a wide input voltage range. The sawtooth ramp offset voltage is 1V (equal to 0.8V*1.25), and the peak of the sawtooth is limited to $V_{CC}$ - 1.4V. With $V_{CC}$ = 5.4V, the ramp has a maximum peak-to-peak amplitude of $V_{CC}$ - 2.4V (equal to 3V); so the feed-forward voltage effective range is typically 3x as the ramp amplitude ranges from 1V to 3V.

A 384 cycle delay is added after the system reaches its rising POR and prior to the soft-start. The RC timing at the FF pin should be sufficiently small to ensure that the input bus reaches its static state and the internal ramp circuitry stabilizes before soft-start. A large RC could cause the internal ramp amplitude not to synchronize with the input bus voltage during output start-up or when recovering from faults. A 1nF capacitor is recommended as a starting value for typical application. The voltage on the FF pin needs to be above 0.8V prior to soft-start and during PWM switching to ensure reliable regulation. In a typical application, FF pin can be shorted to EN pin.

## Power-good

The Power-good comparators monitor the voltage on the internal VMON1 pin. The trip points are shown in Figure 29. PGOOD will not be asserted until after the completion of the soft-start cycle. The PGOOD pulls low upon both EN's disabling it or the internal VMON1 pin's voltage is out of the threshold window. PGOOD will not be asserted until after the completion of the soft-start cycle. PGOOD will not pull low until the fault is present for three consecutive clock cycles.

The UV indication is not enabled until the end of soft-start. In a UV event, if the output drops below -13% of the target level due to some reason (cases when EN is not pulled low) other than OV, OC, OT, and PLL faults, PGOOD will be pulled low.

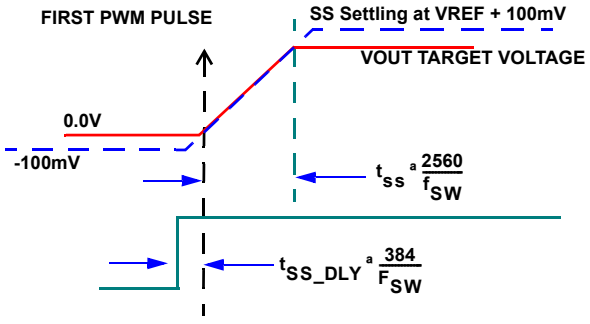



FIGURE 25. SOFT-START WITH $V_{OUT}$ = 0V

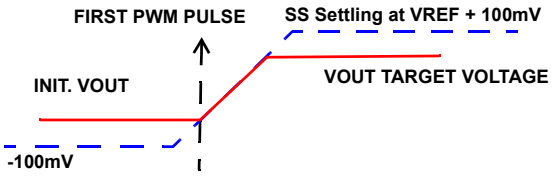



FIGURE 26. SOFT-START WITH $V_{OUT}$ < TARGET VOLTAGE

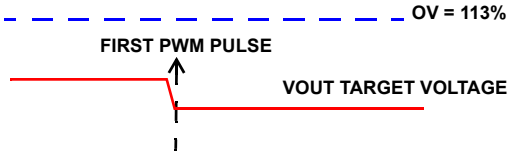



FIGURE 27. SOFT-START WITH VOUT BELOW 0V BUT ABOVE FINAL TARGET VOLTAGE

$$R_{UP} = \frac{V_{EN\_HYS}}{I_{EN\_HYS}} \qquad R_{DOWN} = \frac{R_{UP} \bullet V_{EN\_REF}}{V_{EN\_FTH} - V_{EN\_REF}}$$

where N is number of EN pins connected together

$$V_{EN\_FTH} = V_{EN\_RTH} - V_{EN\_HYS}$$

$$\Delta V_{RAMP} = \text{LIMIT}(V_{CC\_FF} \times G_{RAMP}, \text{VCC - 1.4V - } V_{RAMP\_OFFSET})$$

$$V_{CC\_FF} = \max(0.8V, V_{FF})$$

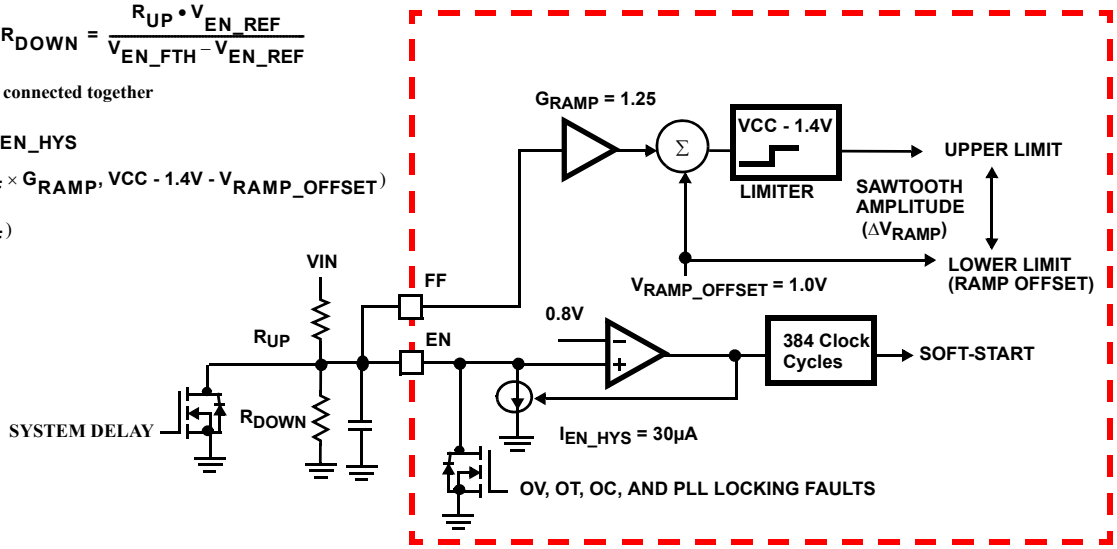



FIGURE 28. SIMPLIFIED ENABLE AND VOLTAGE FEED-FORWARD CIRCUIT

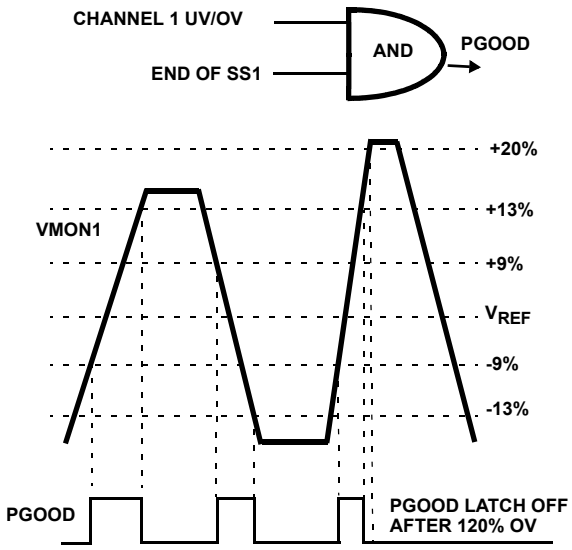



FIGURE 29. POWER-GOOD THRESHOLD WINDOW

## Current Share

The IAVG_CS is the current of the module. ISHARE and ISET pins source a copy of IAVG_CS with 15µA offset, i.e., the full scale will be 123µA.

The share bus voltage ($V_{ISHARE}$) set by an external resistor ($R_{ISHARE}$ = $R_{ISET}$/NCTRL) represents the average current of all active modules. The voltage ($V_{ISET}$) set by $R_{ISET}$ represents the average current of the corresponding module and is compared with the share bus ($V_{ISHARE}$). The current share error signal (ICSH_ER) is then fed into the current correction block to adjust each module's PWM pulse accordingly. The current share function provides at least 10% overall accuracy between ICs, up to 3 phases. The current share bus works for up to 6-phase. Figure 4 further illustrates the current sharing aspects of the ISL8200M.

When there is only one module in the system, the ISET and ISHARE pins can be shorted together and grounded via a single resistor to ensure zero share error - a resistor value of 5k (paralleling 10k on ISET and ISHARE) will allow operation up to the OCP level.

## Overvoltage Protection (OVP)

The Overvoltage (OV) protection indication circuitry monitors the voltage on the internal VMON1 pin.

OV protection is active from the beginning of soft-start. An OV condition (>120%) would latch the IC off (the high-side MOSFET to latch off permanently; the low-side MOSFET turns on immediately at the time of OV trip and then turns off permanently after the output voltage drops below 87%). The EN and PGOOD are also latched low at OV event. The latch condition can be reset only by recycling $V_{CC}$.

There is another non-latch OV protection (113% of target level). At the condition of EN low and the output over 113% OV, the lower side MOSFET will turn on until the output drops below 87%. This is to protect the overall power trains in case of a single channel of a multi-module system detecting OV. The low-side MOSFET always turns on at the conditions of EN = LOW and the output voltage above 113% (all EN pins are tied together) and turns off after the output drops below 87%. Thus, in a high phase count application (multi-module mode), all cascaded modules can latch off simultaneously via the EN pins (EN pins are tied together in multiphase mode), and each IC shares the same sink current to reduce the stress and eliminate the bouncing among phases.

## Over-temperature Protection (OTP)

When the junction temperature of the IC is greater than +150°C (typically), EN pin will be pulled low to inform other cascaded channels via their EN pins. All connected ENs stay low and release after the IC's junction temperature drops below +125°C (typically), a +25°C hysteresis (typically).

## Overcurrent Protection (OCP)

The OCP function is enabled at startup. The load current sampling $I_{CS1}$ is sensed by sampling the voltage across Q2 MOSFET $r_{DS(ON)}$ during turn on through the resistor between the OCSET and the PHASE pin. IC1 is compared with the Channel Overcurrent Limit '108µA OCP' comparator, and waits 7-cycles before the OCP condition is declared. The module's output current ($I_{CS1}$) plus a fixed internal 15µA offset forms a voltage ($V_{ISHARE}$) across the external resistor, $R_{ISHARE}$. $V_{ISHARE}$ is compared with a precision internal 1.2V threshold for a second method to detect OCP condition.

Multi-module operation can be achieved by connecting the ISHARE pin of two or more modules together. In multi-module operation the voltage on the ISHARE pin correlates to the average current of all active channels. The output current of each module in multi-module operation is compared to a precise 1.2V threshold to determine the overcurrent condition. Additionally, each module has an overcurrent trip point of 108µA with 7 cycle delay. This scheme helps protect from damaging a module(s) in multi-module mode by not having a single module carrying more than 108µA. Note that it is not necessary for the $R_{ISHARE}$ to be scaled to trip at the same level as the 108µA OCP comparator. Typically the ISHARE pin average current protection level should be higher than the phase current protection level.

With an internal $R_{ISEN-IN}$ of 2.2kΩ, the OCP level is set to the default value. To lower the OCP level, an external $R_{ISEN-EX}$ is connected between the OCSET and PHASE pin. The relationships between the external $R_{ISEN-EX}$ values and the typical output current $I_{OUT(MAX)}$ OCP levels for ISL8200M are shown in Figures 30 through 33. It is important to note that the OCP level shown in these graphs is the average output current and not the inductor ripple current.

The relationships between the external $R_{ISEN-EX}$ values and the typical output current $I_{OUT(MAX)}$ OCP levels for ISL8200M are shown in Figures 30 through 33. It is important to note that the OCP level shown in these graphs is the average output current and not the inductor ripple current.

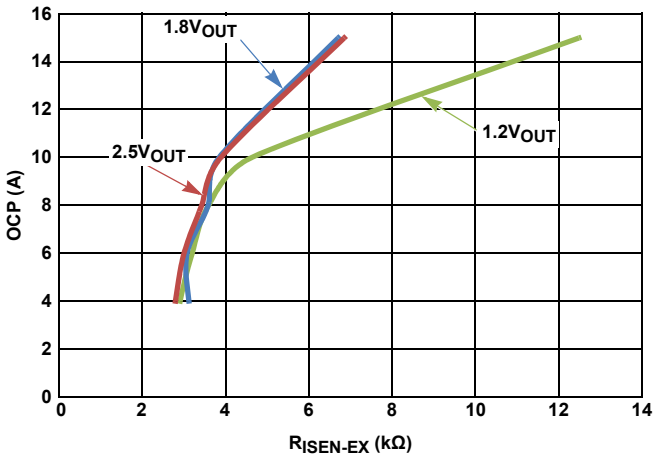



FIGURE 30. $R_{ISEN-EX}$ VALUES vs OCP LEVEL WITH $5V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES

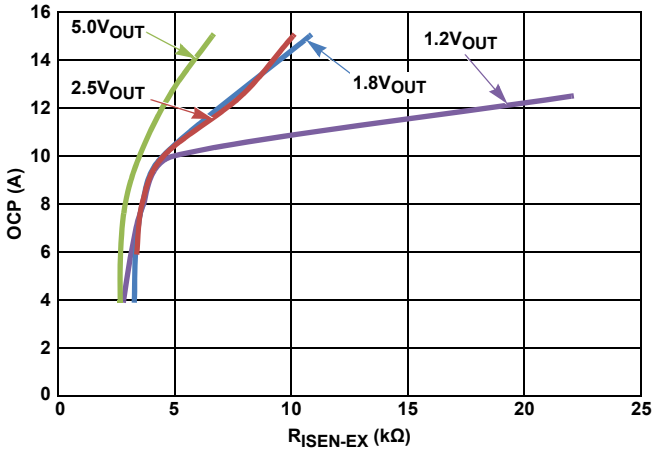



FIGURE 31. $R_{ISEN-EX}$ VALUES vs OCP LEVEL WITH $12V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES

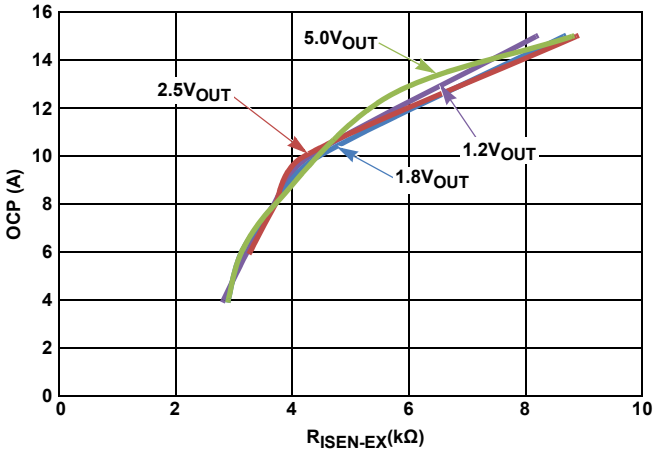



FIGURE 32. $R_{ISEN-EX}$ VALUES vs OCP LEVEL WITH $20V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES

In a high input voltage, high output voltage application, such as 20V input to 5V output, the inductor ripple becomes excessive due to the fixed internal inductor value. In such application, the output current will be limited from the rating to approximately 70% of the module's rated current.

When OCP is triggered, the controller pulls EN low immediately to turn off UGATE and LGATE.

For overload and hard short conditions, the overcurrent protection reduces the regulator RMS output current much less than full load by putting the controller into hiccup mode. A delay time, equal to 3 soft-start intervals, is entered to allow the disturbance to be cleared out. After the delay time, the controller then initiates a soft-start interval. If the output voltage comes up and returns to the regulation, PGOOD transitions high. If the OC trip is exceeded during the soft-start interval, the controller pulls EN low again. The PGOOD signal will remain low and the soft-start interval will be allowed to expire. Another soft-start interval will be initiated after the delay interval. If an overcurrent trip occurs again, this same cycle repeats until the fault is removed.

## Fault Handshake

In a multi-module system, with the EN pins wired OR'ed together, all modules can immediately turn off, at one time, when a fault condition occurs in one or more modules. A fault would pull the EN pin low, disabling all the modules and would not create current bounce. Thus, no single channel would be over stressed when a fault occurs.

Since the EN pins are pulled down under fault conditions, the pull-up resistor ($R_{UP}$) should be scaled to sink no more than 5mA current from EN pin. Essentially, the EN pins cannot be directly connected to VCC.

## Oscillator

The Oscillator is a sawtooth waveform, providing for leading edge modulation with 350ns minimum dead time. The oscillator (Sawtooth) waveform has a DC offset of 1.0V. Each channel's peak-to-peak of the ramp amplitude is set proportionally to the voltage applied to its corresponding FF pin.

## Frequency Synchronization and Phase Lock Loop

The FSYNC_IN pin has two primary capabilities: fixed frequency operation and synchronized frequency operation. By tying a resistor ($R_{FS}$) to PGND1 from the FSYNC_IN pin, the switching frequency can be set at any frequency between 700kHz and 1.5MHz. The ISL8200M has an integrated 59kΩ resistor between FSYNC_IN and PGND1, which sets the default frequency to 700kHz. The frequency setting curve shown in Figure 33 is provided to assist in selecting an externally connected resistor RFS-ext between FSYNC_IN and PGND1 to increase the switching frequency.

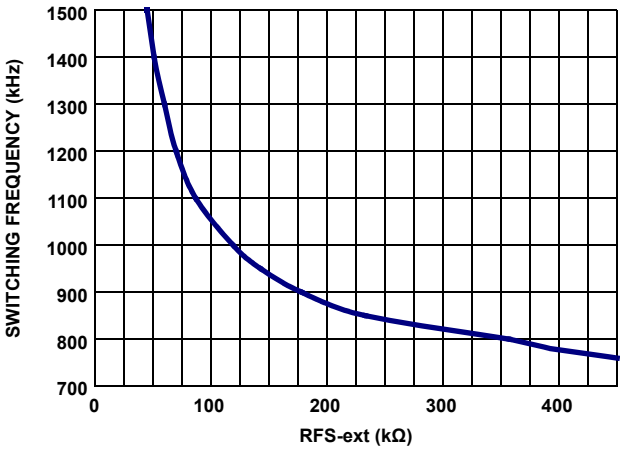



FIGURE 33. RFS-ext vs SWITCHING FREQUENCY

By connecting the FSYNC_IN pin to an external square pulse waveform (such as the CLKOUT signal, typically 50% duty cycle from another ISL8200M), the ISL8200M will synchronize its switching frequency to the fundamental frequency of the input waveform. The voltage range on the FSYNC_IN pin is $V_{CC}/2$ to $V_{CC}$. The Frequency Synchronization feature will synchronize the leading edge of the CLKOUT signal with the falling edge of Channel 1's PWM clock signal. CLKOUT is not available until the PLL locks.

The locking time is typically 210µs for $F_{SW}$ = 700kHz. EN is not released for a soft-start cycle until FSYNC_IN is stabilized and the PLL is in locking. It is recommended to connect all EN pins together in multiphase configuration.

The loss of a synchronization signal for 13 clock cycles causes the IC to be disabled until the PLL returns locking, at which point a soft-start cycle is initiated and normal operation resumes. Holding FSYNC_IN low will disable the IC.

## Setting Relative Phase-shift on CLKOUT

Depending upon the voltage level at PH_CNTRL, set by the VCC resistor divider output, the ISL8200M operates with CLKOUT phase shifted, as shown in Table 2. The phase shift is latched as $V_{CC}$ raises above POR so it cannot be changed on the fly.

TABLE 2.

| DECODING PH_CNTRL RANGE | PHASE FOR CLKOUT WRT CHANNEL 1 | REQUIRED PH_CNTRL |
|---|---|---|
| <29% of $V_{CC}$ | -60° | 15% $V_{CC}$ |
| 29% to 45% of $V_{CC}$ | 90° | 37% $V_{CC}$ |
| 45% to 62% of $V_{CC}$ | 120° | 53% $V_{CC}$ |
| 62% to $V_{CC}$ | 180° | $V_{CC}$ |

## Layout Guide

To achieve stable operation, low losses, and good thermal performance some layout considerations are necessary, which are illustrated in Figures 34 and 35.

- The ground connection between PGND1 (pin 15) and PGND (pin 18) should be a solid ground plane under the module.
- Place a high frequency ceramic capacitor between (1) PVIN and PGND (pin 18) and (2) a 10µF between PVCC and PGND1 (pin 15) as close to the module as possible to minimize high frequency noise. High frequency ceramic capacitors close to the module between VOUT and PGND will help to minimize noise at the output ripple.
- Use large copper areas for power path (PVIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Keep the trace connection to the feedback resistor short.
- Use remote sensed traces to the regulation point to achieve a tight output voltage regulation, and keep them in parallel. Route a trace from VSEN_REM- to a location near the load ground, and a trace from feedback resistor to the point-of-load where the tight output voltage is desire.
- Avoid routing any sensitive signal traces, such as the VOUT and VSEN_REM- sensing point near the PHASE pin or any other noise-prone areas.
- FSYNC_IN is a sensitive pin. If it is not used for receiving an external synchronization signal, then keep the trace connecting to the pin short. A bypass capacitor value of 100pF, connecting between FSYNC_IN pin and GND1, can help to bypass the noise sensitivity on the pin.

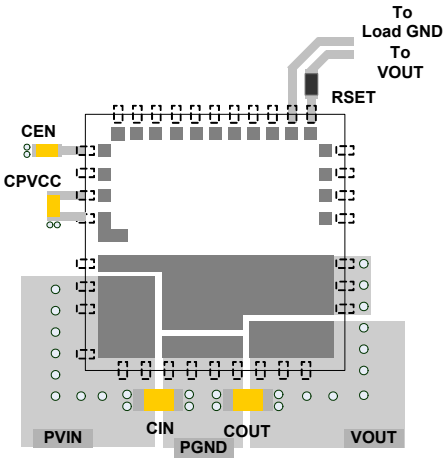



FIGURE 34. RECOMMENDED LAYOUT FOR SINGLE PHASE SETUP

The recommended layout considerations for operating multiple modules in parallel follows the single-phase guidelines as well as these additional points:

- Orient VOUT towards the load on the same layer and connect with thick direct copper etch directly to minimize the loss.
- Place modules such that pins 1-11 point away from power pads (PD1-4) so that signal busses (EN, ISHARE, CLKOUT-to-FSYNC_IN) can be routed without going under the module. Run them along the perimeter as in Figure 35.
- Keep remote sensing traces separate, and connect only at the regulation point. Four separate traces for VSEN_REM- and RSET, as in the example in Figure 35.

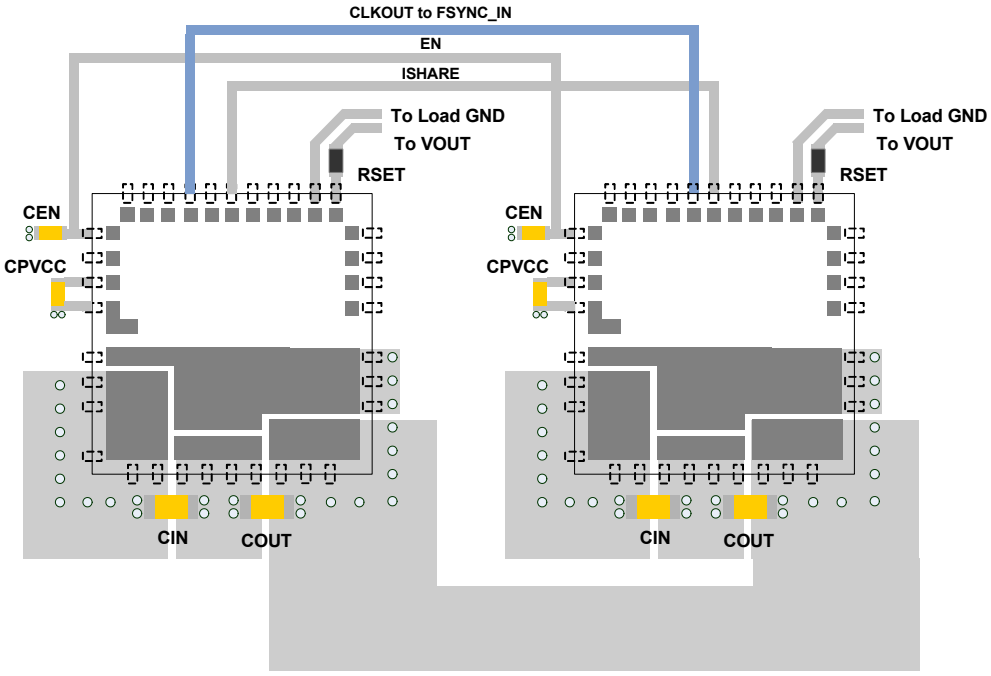



**FIGURE 35. RECOMMENDED LAYOUT FOR DUAL PHASE SETUP**

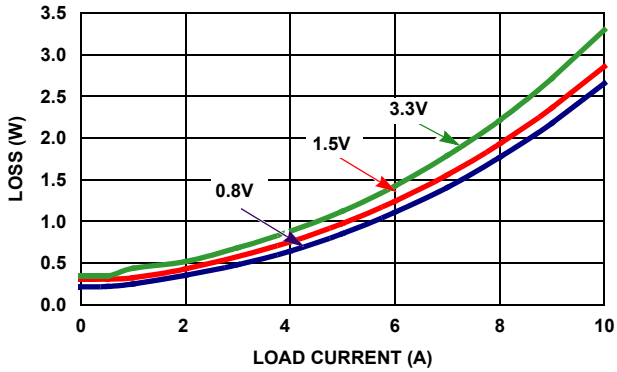



FIGURE 36. POWER LOSS vs LOAD CURRENT ($5V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

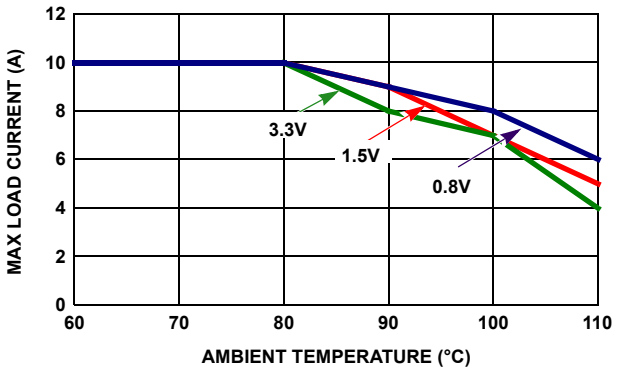



FIGURE 37. DERATING CURVE ($5V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

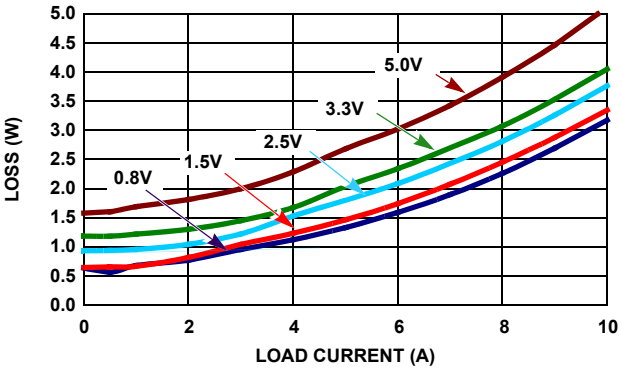



FIGURE 38. POWER LOSS vs LOAD CURRENT ($12V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

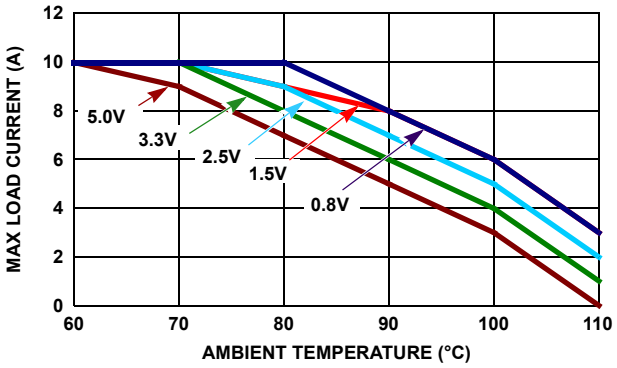



FIGURE 39. DERATING CURVE ($12V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

### Thermal Considerations

Experimental power loss curves along with $\theta_{JA}$ from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margin should be considered.

## Package Description

The structure of the ISL8200M belongs to the Quad Flat-pack No-lead package (QFN). This kind of package has advantages, such as good thermal and electrical conductivity, low weight and small size. The QFN package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8200M contains several types of devices, including resistors, capacitors, inductors and control ICs. The ISL8200M is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the package outline drawing L23.15x15 on page 25. The module has a small size of 15mm x 15mm x 2.2mm. Figure 40 shows typical reflow profile parameters. These guidelines are general design rules. Users could modify parameters according to their application.

## PCB Layout Pattern Design

The bottom of ISL8200M is a lead-frame footprint, which is attached to the PCB by surface mounting process. The PCB layout pattern is shown in the Package Outline Drawing L23.15x15 on page 24. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and I/O termination dimensions, except for the PCB lands being a slightly extended distance of 0.2mm (0.4mm max) longer than the QFN terminations, which allows for solder filleting around the periphery of the package. This ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

## Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be from 0.3mm to 0.33mm in diameter with the barrel plated with 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

## Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the Package Outline Drawing L23.15x15 on page 25. The gap width between pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) QFN.

## Reflow Parameters

Due to the low mount height of the QFN, "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profile given in Figure 40 is provided as a guideline, to be customized for varying manufacturing practices and applications.

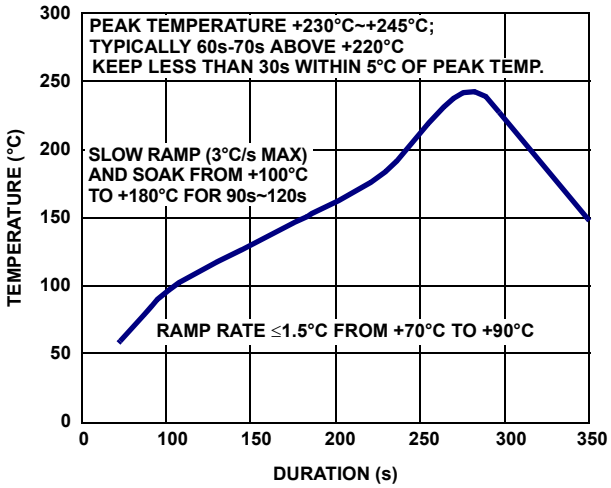



FIGURE 40. TYPICAL REFLOW PROFILE

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| June 9, 2015 | FN6727.2 | -Complete Functional Schematic on page 1 changed $V_{IN}$ Range from "3V to 20V" to "4.5V to 20V" and added Note.<br>-Stamped “Not Recommended for New Designs Recommended Replacement part ISL8200AM.<br>-Updated Related literature on page 1<br>-Updated Feature bullet, changed the Input Voltage Minimum range from “+3.0V” to “+4.5V”<br>-Removed all reference to ISL8200MEVAL2PHZ evaluation board since part is retired.<br>-Added Eval board to ordering information table.<br>-Grammatical edits throughout document.<br>-Updated sense resistor reference designators, paragraph descriptions and table headings related to $R_{ISEN}$ calculations for clarity.<br>-Edited “Pinout Internal Circuit” on page 2 for clarity by adding current sharing circuitry for dual phase designs.<br>-Pin 13 in Pin Descriptions on page 4 changed 2nd sentence from “When used with an external 5V supply, this pin should be tied directly to VCC” to “When used with an external 5V supply, this pin should be tied directly to PVCC”. Last sentence also in Pin 13 changed from “Input Voltage Range 0V to 20V” to “The input voltage range is 4.5V to 20V”<br>-“Programming the Output Voltage ($R_{SET}$)” on page 13 changed "$R_{OS1}$" to "$R_{OS}$" in Note and replaced "The resistance for different output voltages are as follows:" with "The resistance for different output voltages in single phase operation are listed in Table 1”.<br>-Updated title in Figure 34 on page 19 and added Figure 35 on page 20.<br>-**Updated Electrical Specifications table as follows:**<br>1. PVCC test condition changed from 0mA to 250mA to 0mA, $V_{IN}$ = 12V and MIN, MAX from 5.1, 5.6 to 5.15, 5.96.<br>2. Changed Hysteresis sink current MIN limit from “25” to “23”.<br>3. Frequency Sync. and Phase Lock Loop - Changed "Synchronization Frequency" test condition from: "$V_{CC}$ = 5.4V (2.97)" to: "$V_{CC}$ = 5V"<br>4. Changed "PLL Locking Time" test condition from: "$V_{CC}$ = 5.4V (2.97V); $F_{SW}$ = 700kHz" to: "$V_{CC}$ = 5.4V; $F_{SW}$ = 700kHz"<br>5. Changed Undervoltage Lockout Hysteresis TYP from “1.5” to “1.6”.<br>6. Sink current added MIN limit 15.4 and test condition $V_{EN}$ = 1V. Removed Max limit of 15mA<br>7. Sink impedance changed test condition from $I_{EN\_SINK}$ = 5mA to $V_{EN}$ = 1V. Changed max limit from 65Ω to 64Ω<br>8. Changed Paramater Name from “Negative Input Source Current” to “$V_{SEN+}$ Pins Input Current”, Symbol from from “$I_{VSEN-}$” to “$I_{VSEN+}$”. Changed TYP value from “100nA” to “1µA” and added MIN 0.2µA, MAX = 2.5µA<br>9. Input Impedance TYP changed from 1MΩ to -600kΩ and added test conditions<br>10. Share Pin OC Threshold Test Condition changed from “VCC = 2.97V to 5.6V (comparator offset included)” to “Comparator offset included”<br>11. Removed “Share Pin OC Hysteresis” Parameter.<br>12. Over-temperature Protection, added Test Conditions “Controller junction temperature” to both Over-temperature Trip and Over-Temperature Release<br>13. Overvoltage Protection, removed “Up” from OV Latching Up Trip Point and OV Non-Latching Up Trip Point Parameters.<br>14. External Current Share Accuracy TYP changed from ±5% to ±10%. Changed Test conditions from “VCC = 2.97V and 5.6V, 1% Resistor Sense, 10mV Signal” to “Up to 3 phases”. |
| February 26, 2010 | FN6727.1 | Updated page 1 title, description and features to better highlight the part’s ease-of-use. Added Related Literature section. Replaced Figures 1, 3, 4, 5. Added Theta $J_C$ and associated note. Added 1st paragraph under Table 1. Changed instances of VMON to VMON1 throughout. Removed VMON2 reference in test conditions for disable threshold. Changed ROS to ROS1 in paragraph above Table 1 on page 13. Replaced last paragraph under “Programming the Output Voltage ($R_{SET}$)” on page 13. Added Equations 2 and 3 and related text. |
| December 22, 2009 | FN6727.0 | Initial Release. |

# About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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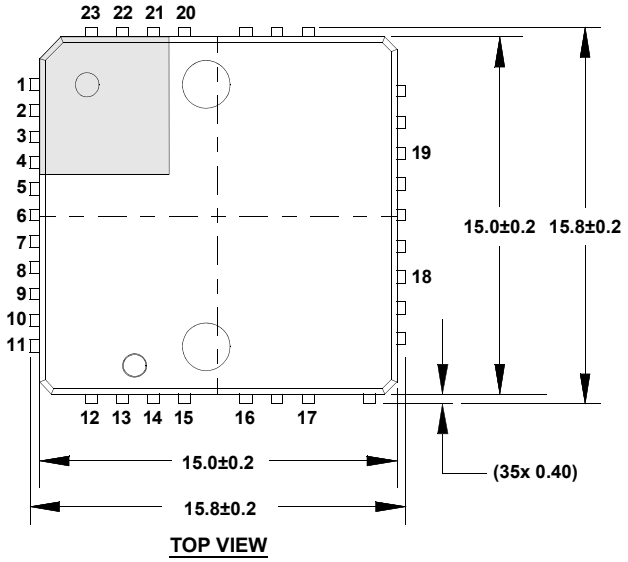
# Package Outline Drawing

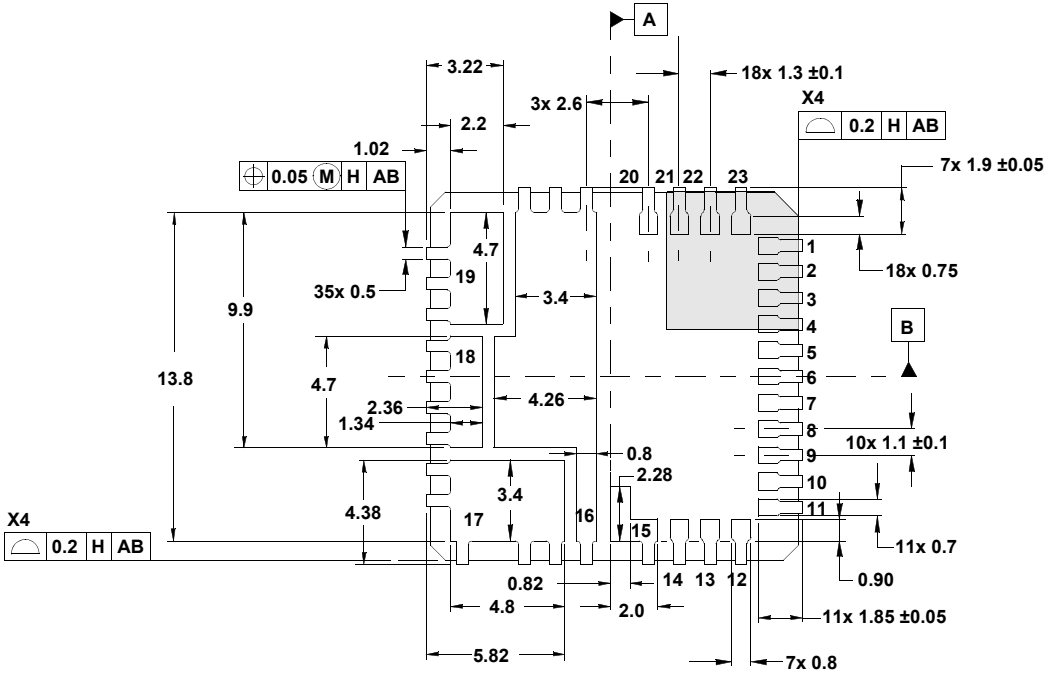
## L23.15x15

**23 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)**

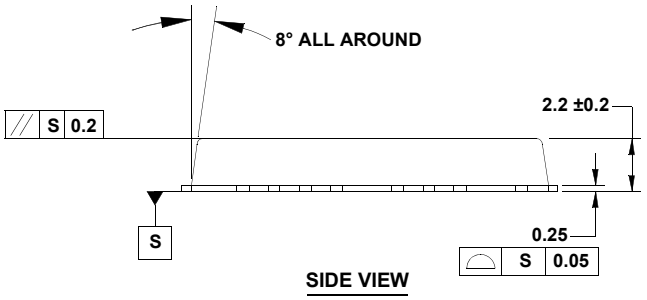
**Rev 3, 10/10**




TOP VIEW



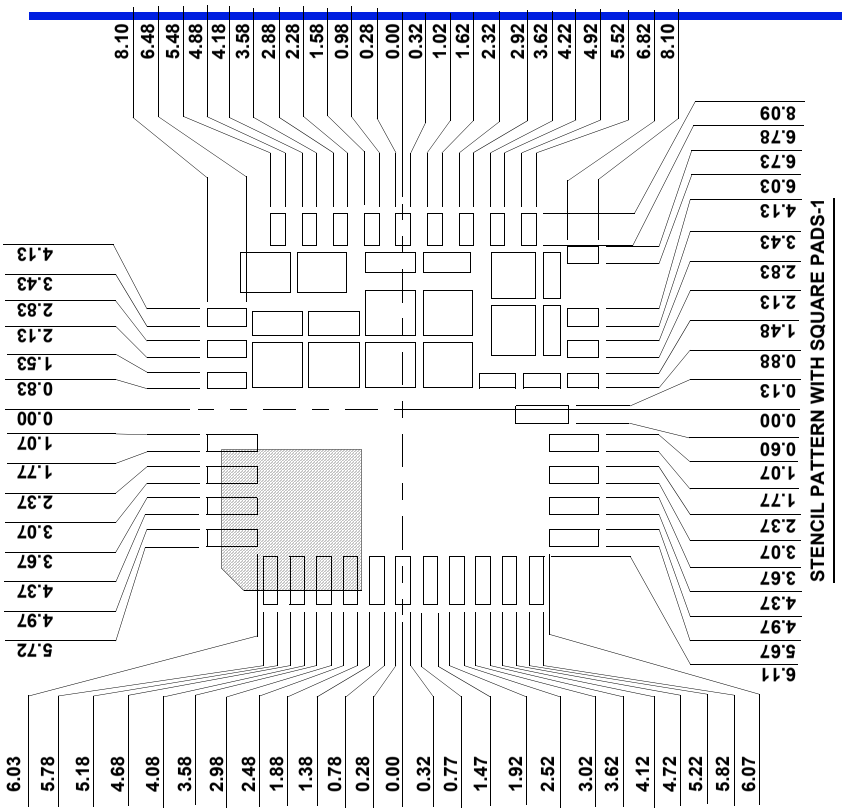

BOTTOM VIEW

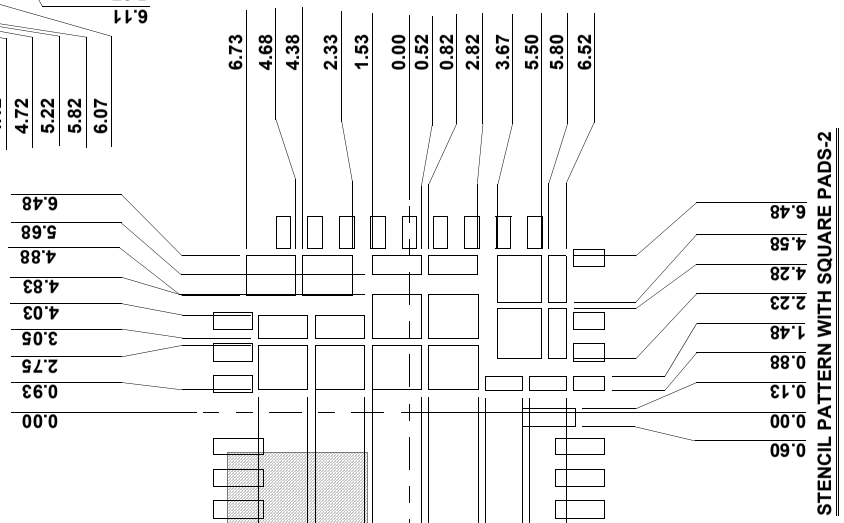


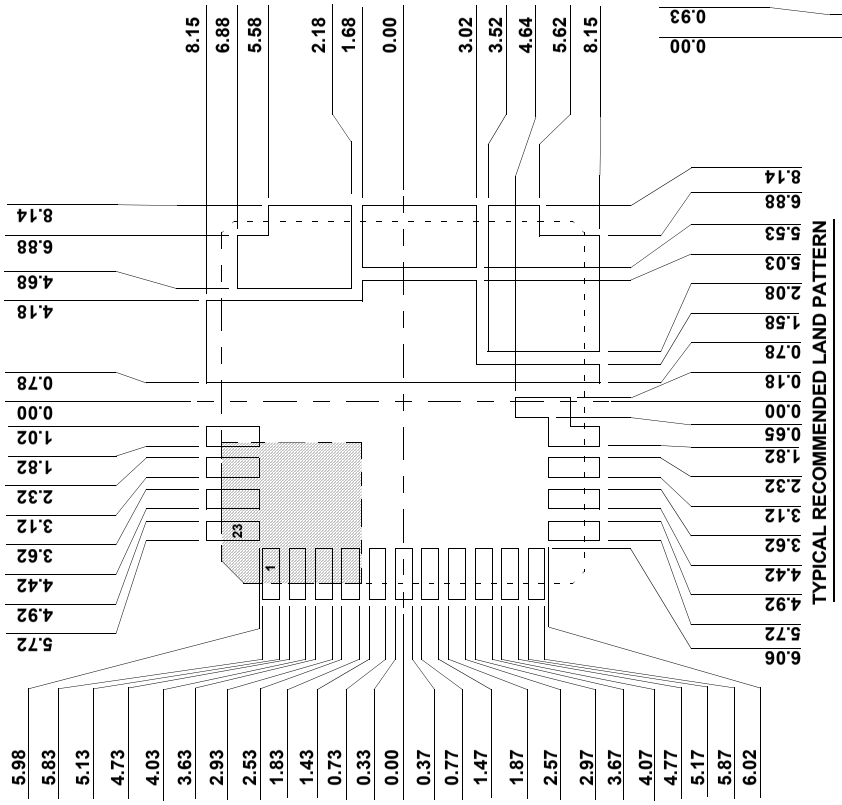

SIDE VIEW

**NOTES:**

1. Dimensions are in millimeters.
2. Unless otherwise specified, tolerance : Decimal ± 0.2; Body Tolerance ±0.2mm
3. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.


STENCIL PATTERN WITH SQUARE PADS-1


STENCIL PATTERN WITH SQUARE PADS-2


TYPICAL RECOMMENDED LAND PATTERN