ISL78263

Automotive 42V Dual Synchronous Boost and Low-Iq Buck Controllers with Integrated Drivers

The ISL78263 offers synchronous boost and buck controllers. The boost controller operates either as an independent channel or as a pre-boost function that supplies the buck controller. The low-I_Q buck controller uses only 6µA quiescent current, allowing it to support low-power, always-on operation. Both controllers support wide duty-cycles for switching frequencies from 200kHz to 2.2MHz. Both devices can be synchronized to an external clock and offer programmable spread spectrum clocking to mitigate EMI.

In pre-boost buck mode, the boost of the ISL78263 can be set to activate during falling V_{IN} transients and continues to operate with an input voltage down to 2.1V. This allows the buck output to maintain regulation, even as the V_{IN} voltage falls below its output. To support the increase in input current that occurs when V_{IN} falls, the ISL78263 integrates robust MOSFET drivers to allow the use of multiple FETs in parallel.

ISL78263 is qualified to AEC-Q100 Grade 1 and is specified to operate across an ambient temperature range of -40°C to 125°C. The device is available in a 5mmx5mm, 32 Ld WFQFN (Wettable Flank) package. The features of the ISL78263 make it ideally suited as a front-end regulator for automotive systems that must maintain always-on operation and support severe cold-cranking transients.

Features

- V_{IN} operating range: 2.1 to 42V
- Low quiescent current: 6µA typical, buck channel
- Switching frequency: 200kHz to 2.2MHz
- Boost frequency at 1x or 0.2x the buck frequency
- Dropout mode (buck) for high duty-cycle operation
- 25ns on-times for low duty-cycle operation
- External synchronization
- Programmable spread spectrum clocking
- 2A Sourcing / 3A sinking MOSFET drivers
- Boot UV and programmable boot refresh time
- Extensive protection mechanisms for OV/UV/OC/OT

Applications

- Automotive battery supplied application
- In cabin systems
- ADAS: Advanced Driver Assist Systems
- Start-stop protected systems (such as head unit, cluster, e-Mirror)

Table 1. Output Configurations

Controller 1 Output	Controller 2 Output
Buck 3.3V Fixed Buck 5.0V Fixed	Boost Adjustable 5V to 40V
Buck Adjustable 0.8V to 5V	

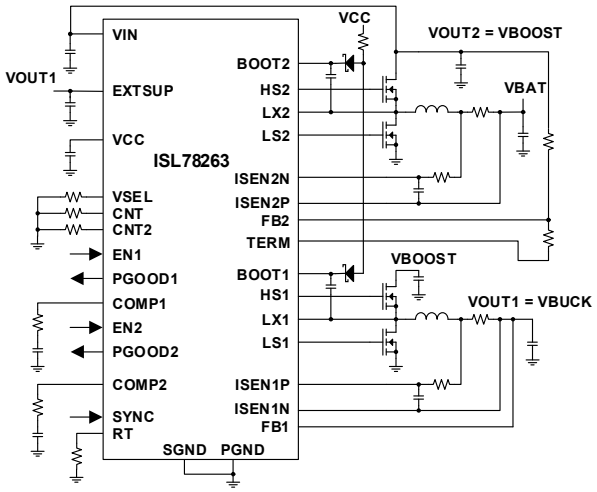


Figure 1. Typical Applications Schematic

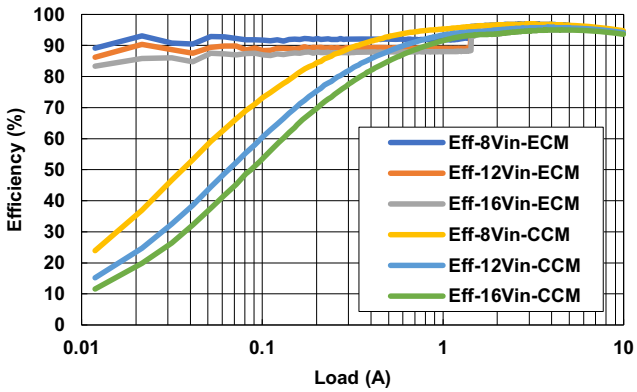


Figure 2. Buck Efficiency (VOUT1 = 5V, f_{SW} = 400 kHz)

© 2020 Renesas Electronics

Contents

1. Overview . . . 3
1.1 Typical Application Schematic . . . 3
1.2 Block Diagram . . . 4
1.3 Ordering Information . . . 5
1.4 Pin Configuration . . . 5
1.5 Pin Descriptions . . . 5

2. Specifications . . . 8
2.1 Absolute Maximum Ratings . . . 8
2.2 Thermal Information . . . 8
2.3 Recommended Operation Conditions . . . 8
2.4 Electrical Specifications . . . 9

3. Typical Perfomance Curves . . . 14

4. Functional Description . . . 18
4.1 Synchronous Buck and Boost . . . 18
4.2 Configuration Tables for VSEL, CNT, and CNT2 . . . 18
4.3 Start-Up Operation in Cold Crank Configuration . . . 19
4.4 Start-Up Operation with Individual Buck and Boost . . . 20
4.5 Enable 1 and Enable 2 Operational Levels . . . 20
4.6 Internal LDO and EXTSUP . . . 20
4.7 Oscillator . . . 20
4.8 Phase Shift . . . 21
4.9 PGOOD Signals . . . 21
4.10 Buck Stage (Converter 1) . . . 21
4.11 Boost Stage (Converter 2) . . . 22
4.12 Energy Conservation Mode (ECM) . . . 23

5. Application Information . . . 26
5.1 Buck Converter . . . 26
5.2 Boost Converter . . . 30
5.3 Recommended PCB Layout . . . 33

6. Revision History . . . 35

7. Package Outline Drawing . . . 36

1. Overview

1.1 Typical Application Schematic

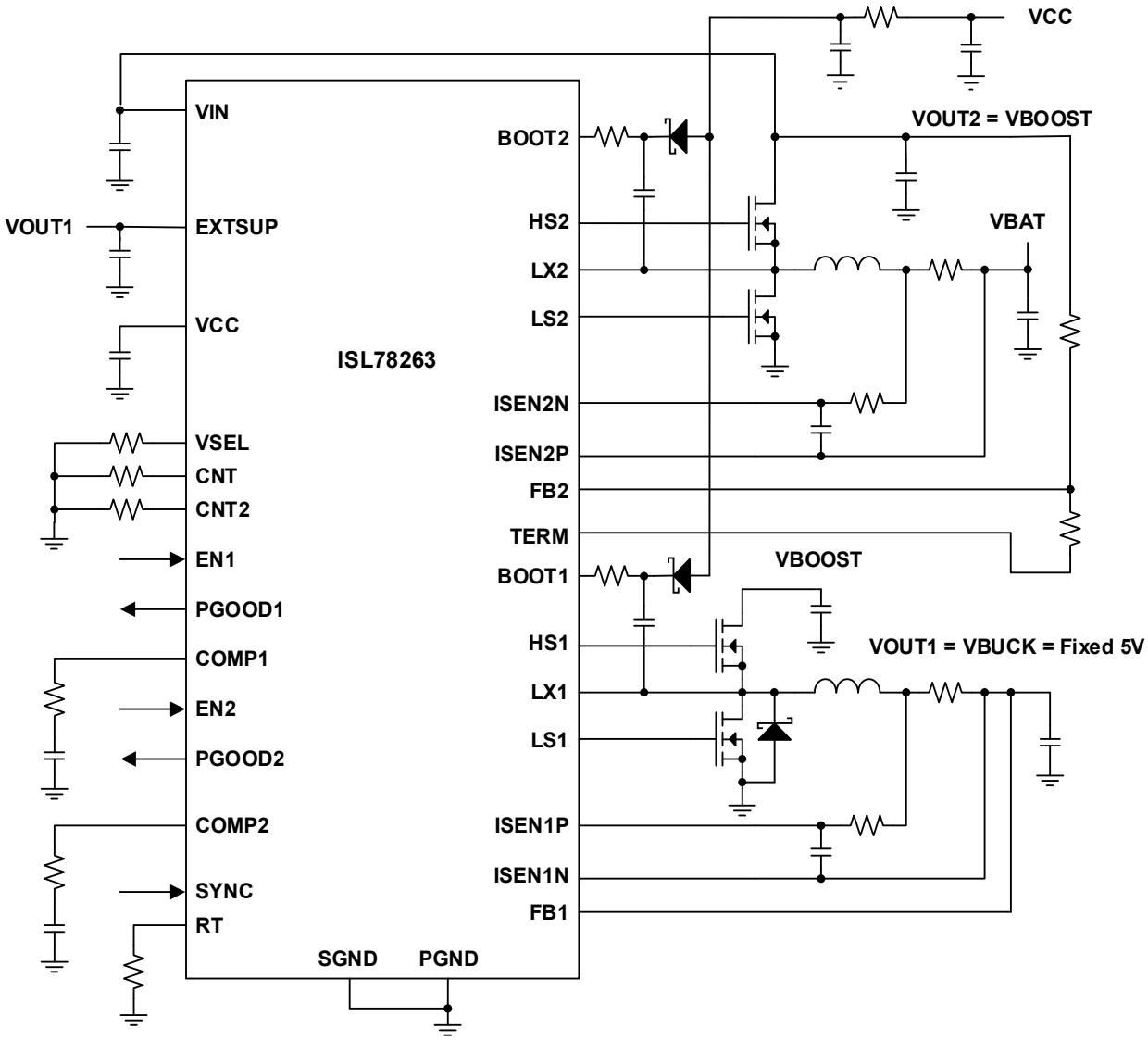


Figure 3. Typical Cold Crank Applications Schematic (Channel 1 Fixed at 5V)

1.2 Block Diagram

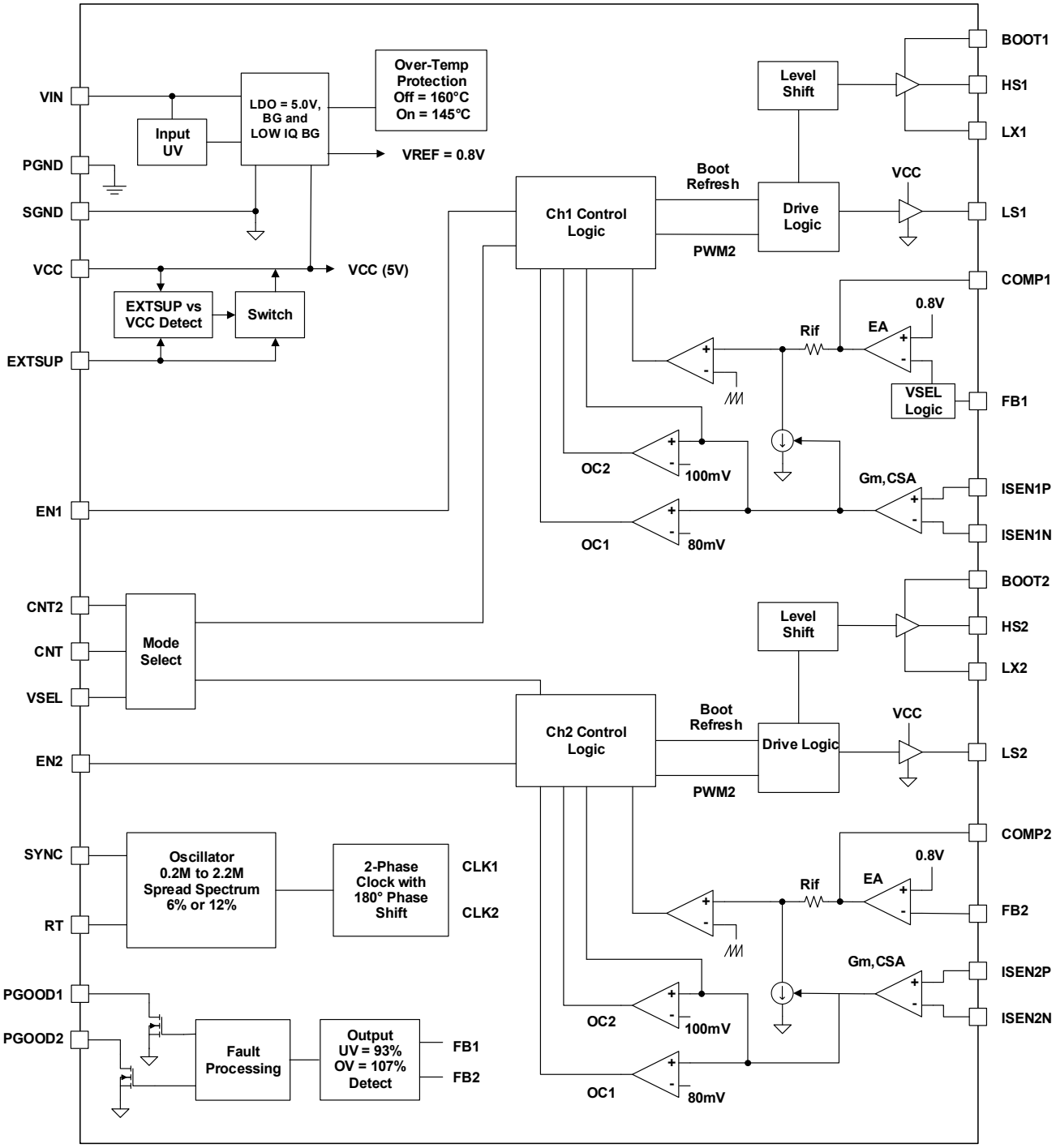


Figure 4. Block Diagram

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Package (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp Range
ISL78263ARZ	78263ARZ	32 Ld 5x5 QFN	L32.5x5H	Tube	-40 to +125°C
ISL78263ARZ-T				Reel, 6k	
ISL78263ARZ-T7A				Reel, 250	
ISL78263EVAL1Z	Evaluation Board for ISL78263				

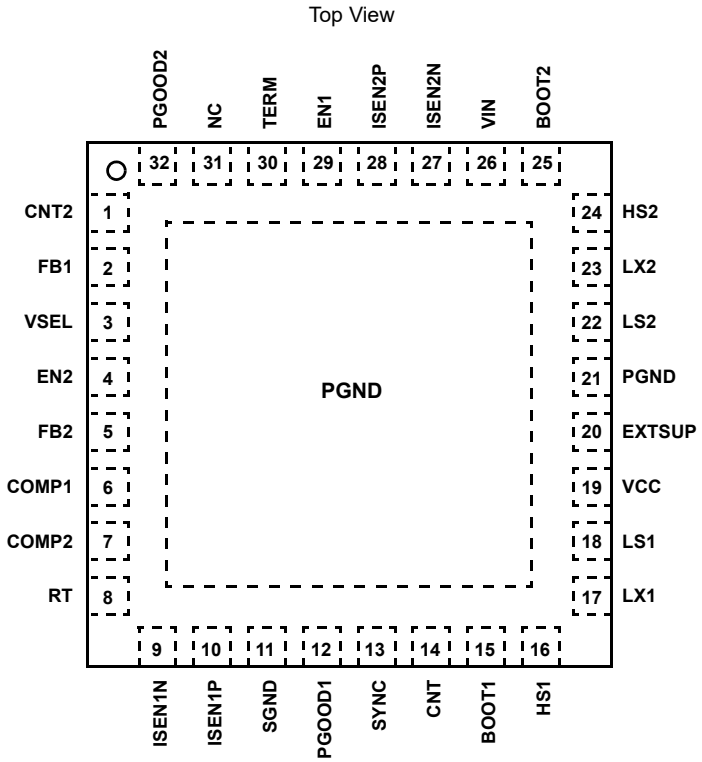
Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL78263 device page. For more information about MSL see TB363.

Table 2. Key Differences Between Family of Parts

Part #	Channel 1 Output Range	Channel 2 Output Range
ISL78263	Buck, 3.3V, 5V, 0.8V to 5V Adjustable	Boost, 5V to 40V Adjustable
ISL78264	Buck, 3.3V, 5V, 0.8V to 5V Adjustable	Buck, 0.8V to 32V Adjustable

1.4 Pin Configuration



1.5 Pin Descriptions

Pin Number	Pin Names	Description
1	CNT2	This pin sources a current at startup and reads the voltage across a resistor to ground to program internal boot refresh on-time of the low-side switch for 180ns or 360ns, and also allows selection of Channel 2 boost frequency as either $1xf_{SW}$ or $1/5xf_{SW}$ of channel 1 buck (See Table 5).

Pin Number	Pin Names	Description
2	FB1	Feedback pin for Channel 1 buck. For fixed output voltages of 5.0V or 3.3V, this pin is connected directly to the output of Channel 1 buck. For adjustable output, this pin connects to a resistive divider from Channel 1 output to ground, and the FB1 voltage is regulated to 0.8V.
3	VSEL	This pin sources a current at startup and reads the voltage across a resistor to ground to program the Channel 1 buck output to a fixed voltage of 5.0V or 3.3 V, or as an adjustable voltage in the range of 0.8V to 5.0V. For each of these selections, the boost converter can be configured as Cold Crank or Individual Boost operation. (See Table 3).
4	EN2	Enable control pin of Channel 2 with a logic high voltage enabling operation of Channel 2.
5	FB2	Feedback pin for Channel 2 boost regulator with adjustable output. This pin connects to a resistive divider from Channel 2 output to ground, and the FB2 voltage is regulated to 0.8V.
6	COMP1	Loop compensation pin for Channel 1 with a resistor/capacitor network connected to ground to provide control loop compensation for Channel 1 buck regulator.
7	COMP2	Loop compensation pin for Channel 2 with a resistor/capacitor network connected to ground to provide control loop compensation for Channel 2 boost regulator.
8	RT	A resistor from RT to GND programs the switching frequency for Channel 1 and Channel 2, with Channel 2 shifted 180° in phase from Channel 1 to minimize input ripple current. This pin is pulled to ground while in ECM and is otherwise 0.5V.
9	ISEN1N	The output current sense pin connected to the negative terminal of the current sense resistor, also connected to the output voltage of Channel 1.
10	ISEN1P	The output current sense pin connected to the junction of the positive terminal of the current sense resistor and the power inductor of Channel 1.
11	SGND	Analog GND for the IC, connected to the PGND pin in the top copper trace under the IC.
12	PGOOD1	Power-good pin for Channel 1 with an open-drain output, producing a low output if the Channel 1 output is not within ±7% (typical) of the programmed output voltage, and a logic high output if the output is within regulation.
13	SYNC	Connect SYNC to an external clock in the range of 200kHz to 2.4MHz to synchronize the internal clock with operation in FCCM. Connect to VCC to force the part into Fixed frequency Continuous Conduction Mode (FCCM) operation using the internal oscillator. Connect to GND to allow the controller to automatically switch between Continuous Conduction Mode, and Diode Emulation Mode (DEM), or ECM mode depending on load current level. In DEM and CCM the device will use the internal oscillator programmed by RT pin. The pin can be switched during operation (VCC to GND, or GND to VCC) to change the mode of operation.
14	CNT	This pin sources a current at startup and reads the voltage across a resistor to ground to program the spread spectrum (ON/OFF, and frequency variation) and dead time (See Table 4 on page 19).
15	BOOT1	Provides connection point for a ceramic boot capacitor providing high-side gate voltage supply for Channel 1. The capacitor is charged through an external diode connected to VCC through an R-C filter.
16	HS1	The output of Channel 1 high-side MOSFET gate driver.
17	LX1	Connected to the Channel 1 switch node, providing the return path for the high-side MOSFET gate driver back to BOOT1.
18	LS1	The output of Channel 1 low-side MOSFET gate driver swinging between VCC and GND.
19	VCC	Bias supply (5V typical) for the IC and MOSFET gate drivers, and should be decoupled with a ceramic capacitor of 10µF. This pin is supplied by internal LDO during start-up and can be powered from EXTSUP after initial start-up, using the automatic switchover function.
20	EXTSUP	EXTSUP accepts external bias input of 5V typical that can be supplied from Channel 1 output of 5.0V, or an independent supply derived from other sources. The external bias should not be applied until VIN has exceeded initial start-up voltage; however, a voltage such that EXTSUP - VIN ≤ 0.5V would be allowed.

Pin Number	Pin Names	Description
21	PGND	Connection point for power ground of the switching circuits for Channel 1 and Channel 2, and serves as the return path for the low-side MOSFET gate drive.
22	LS2	The output of Channel 2 low-side MOSFET gate driver swinging between VCC and GND.
23	LX2	Connected to the Channel 2 switch node, providing the return path for the high-side MOSFET gate driver back to BOOT2.
24	HS2	The output of Channel 2 high-side MOSFET gate driver.
25	BOOT2	Provides connection point for a ceramic boot capacitor providing high-side gate voltage supply for Channel 2. The capacitor is charged through an external diode connected to VCC.
26	VIN	Connected to the high voltage input supply for the buck regulators, and is normally supplied from a battery. This pin is decoupled using a 0.1µF or larger ceramic capacitor.
27	ISEN2N	Input current sense pin of Channel 2 boost, connected to the negative terminal of the current sense resistor and the inductor.
28	ISEN2P	Input current sense pin connected to the positive terminal of the current sense resistor at the input of the Channel 2 boost.
29	EN1	Enable control pin of Channel 1 with a logic high voltage enabling operation of Channel 1. For initial start-up, this pin may be connected to the VIN supply through a 100kΩ resistor.
30	TERM	This is the GND disconnect terminal for the bottom of the buck feedback resistor. The external resistive divider connected to the TERM pin should have sufficient resistance to limit the current into the TERM pin to < 25mA at maximum VBOOST.
31	NC	Not internally connected; leave unconnected or tie to GND.
32	PGOOD2	Power-good pin for Channel 2 with an open-drain output, producing a low output if the Channel 2 output is not within ±7% (typical) of the programmed output voltage, and a logic high output if the output is within regulation.
33	EPAD	The bottom pad of the IC, to be connected to PGND and SGND under the IC. Connect to internal PCB GND layers using multiple vias.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VIN, EN1, FB1, FB2, TERM, ISEN2N, and ISEN2P	-0.3	45	V
HS1, HS2, LX1, LX2, BOOT1, BOOT2	-0.3	65	V
EN2, COMP1, COMP2, PGOOD1, PGOOD2, CNT, RT, SYNC	-0.3	6.5	V
ISEN1N and ISEN1P, LS1, LS2, VCC, EXTSUP, VSEL, CNT2	-0.3	6.5	V
All Other Pins	-0.3	6.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per AEC-Q100-002E)	3		kV
Charged Device Model (Tested per AEC-Q100-011C1)	2		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld 5x5 QFN Package (Notes 4, 5)	30	1.2

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+125	°C
Startup Voltage Range V_{IN}	6.0	42	V
Battery Voltage Range V_{BAT} (Cold Crank)	2.1	42	V
Buck Channel 1 V_{OUT} Fixed options	3.3	5.0	V
Buck Channel 1 V_{OUT} Adjustable Range	0.8	5.0	V
Boost Channel 2 V_{OUT} Adjustable Range	5.0	40	V

2.4 Electrical Specifications

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
Power Supply						
V_{IN} Undervoltage Lockout Threshold	$V_{IN,UVLO}$	Rising voltage sensed at VIN pin	**5.455**	5.650	**5.845**	V
Boost ON/OFF Lower (V_{IN} Monitor Pin)	V_{INL}	Turn-on threshold rising, measured at ISEN2P (Buck continues to operate)	**4.3**	4.5	**4.7**	V
		Turn-off threshold falling, measured at ISEN2P (Buck continues to operate)	**2.0**	2.1	**2.2**	V
Boost OFF/ON Upper (V_{IN} Monitor Pin)	V_{VINU}	Turn-off threshold rising (Buck continues to operate)	**8.0**	8.25	**8.4**	V
		Turn-on threshold falling (Buck continues to operate)	**7.76**	8	**8.24**	V
V_{IN} Supply Current in ECM	I_{QECM}	ECM mode, no external load on V_{OUT} (Note 8)		6		µA
V_{IN} Supply Current during normal switching	I_Q	PWM mode, no external load on V_{OUT}, EN1 = EN2 = HIGH, f_{SW} = 2.2MHz, Gate drive No Load		11	**25**	mA
V_{IN} Supply Current, Shutdown	I_{SD}	EN1 = EN2 = SGND		0.3	**6**	µA
LDO and EXTSUP						
Output Voltage of internal LDO	V_{VCC}	V_{IN} = 6.0V to 42V, I_{OUT} = 130mA	**4.75**	5.0	**5.25**	V
Output Current of internal LDO	I_{VCC}	V_{IN} = 6.0 to 42V			**0.13**	A
Dropout Voltage of internal LDO	D_{VCC}	V_{IN} = 4.5V, I_{LDO}=130mA			**1.0**	V
LDO Current Limit	I_{LMTLDO}	V_{CC} = 4.5V	**130**		**250**	mA
LDO Current Limit	I_{LMTLDO}	V_{CC} = 0V	**130**		**250**	mA
VCC Undervoltage Lockout Threshold	$V_{VCCUVLO}$	Rising	**4.0**	4.2	**4.3**	V
		Falling	**3.8**	4.0	**4.1**	V
		Hysteresis	**0.15**	0.2	**0.25**	V
External Bias Voltage	V_{EXTSUP}		**4.75**	5	**5.25**	V
External Bias Voltage Switchover Threshold	VTH_{EXTSUP}	Rising	**4.462**	4.6	**4.738**	V
		Falling	**4.268**	4.4	**4.532**	V
		Hysteresis	**0.15**	0.2	**0.25**	V
Oscillator, Spread Spectrum						
CH1 Internal Switching Frequency	f_{SWCH1}	RT to GND resistor = 86.6kΩ	**0.18**	0.2	**0.22**	MHz
		RT to GND resistor = 6.81kΩ	**2.0**	2.2	**2.4**	MHz
CH1 External Switching Frequency	f_{SWCH1}	Applied to SYNC pin	**0.2**		**2.4**	MHz
CH2 Internal Switching Frequency	f_{SWCH2}	1/5 x f_{SW}; See CNT2 configuration (Table 5)	**396**	440	**484**	kHz
	f_{SWCH2}	1 x f_{SW}; See CNT2 configuration (Table 5)	**2.0**	2.2	**2.4**	MHz
RT Pin Voltage	V_{RT}			0.5		V
Spread Spectrum Narrow Mode	F_{SSNAR}	Spread Spectrum ON narrow mode, See CNT configuration (Table 4)		+6		%
Spread Spectrum Wide Mode	F_{SSWID}	Spread Spectrum ON wide mode, See CNT configuration (Table 4)		+12		%

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
Controller 1 Specification (Buck)						
Output Voltage	V_{OUTCH1}	VSEL to GND resistor = 6.04kΩ, See V_{SEL} configuration (Table 3)	**3.2505**	3.3	**3.3495**	V
		VSEL to GND resistor = 75kΩ, See V_{SEL} configuration (Table 3)	**4.925**	5.0	**5.075**	V
FB1 Pin Voltage Regulation (Adj)	$V_{FBCH1ADJ}$	VSEL to GND resistor = 37.4kΩ, See V_{SEL} configuration (Table 3)	**0.788**	0.8	**0.812**	V
V_{OUT} Comparator Threshold at ECM	V_{FBCH1}	V_{OUT} = 3.3V	**3.234**	3.3	**3.366**	V
		V_{OUT} = 5.0V	**4.9**	5.0	**5.1**	V
		V_{FB} = 0.8V, in adjustable V_{OUT} mode	**0.784**	0.80	**0.816**	V
FB Pin Leakage Current	I_{FBCH1}				**0.25**	µA
Forward CH1 Cycle-by-Cycle Current Limit	$I_{LMT1CH1+}$	ISEN1P-ISEN1N	**64**	80	**100**	mV
Forward CH1 Hiccup Current Limit	$I_{LMT2CH1+}$	ISEN1P-ISEN1N	**80**	100	**124**	mV
Reverse CH1 Current Limit	$I_{LMTCH1-}$	ISEN1P-ISEN1N	**-50**	-40	**-33**	mV
CH1 Zero Cross	I_{ZCDCH1}		**-4**	2	**9**	mV
CH1 Short Dead Time	T_{DTLH1S}	Low-side low to high-side high, See CNT configuration (Table 4)	**15**	25	**40**	ns
	T_{DTHL1S}	High-side low to low-side high, See CNT configuration (Table 4)	**30**	43	**70**	ns
CH1 Long Dead Time	T_{DTLH1L}	Low-side low to high-side high, See CNT configuration (Table 4)	**70**	100	**120**	ns
	T_{DTHL1L}	High-side low to low-side high, See CNT configuration (Table 4)	**70**	100	**120**	ns
CH1 Maximum Duty	$T_{DTMAXCH1}$		**97**	98.75		%
CH1 Minimum On-Time	$T_{ONMINCH1}$		**15**	25	**35**	ns
CH1 Minimum Off-Time	$T_{OFFMINCH1}$		**30**	40	**55**	ns
CH1 Soft-Start Time	T_{SSCH1}			4.5		ms
CH1 Buck Error Amp (OTA) GM	$CH1_{EAOTA}$			1.7		mS
BOOT1 Refresh	$V_{B1RFRESH}$	Rising	**3.3**	3.5	**3.7**	V
		Falling	**3.2**	3.4	**3.6**	V
		Hysteresis	**0.04**	0.08	**0.16**	V
CH1 Overvoltage Protection	$CH1_{OVP}$	Rising	**105**	107	**109**	%
		Falling	**103**	105	**107**	%
		Hysteresis	**1.5**	2.2	**3.0**	%
CH1 Undervoltage Protection	$CH1_{UVP}$	Rising	**93**	95	**97**	%
		Falling	**91**	93	**95**	%
		Hysteresis	**1.5**	2.2	**3**	%
V_{IN} Pulse Skip Threshold	VTH_{PSKIP}	Rising	**18**	18.6	**19.5**	V
		Falling	**17.6**	18.2	**18.7**	V
		Hysteresis	**0.4**	0.55	**0.7**	V

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
ECM Entry Threshold	VTH_{ECMENT}	Rising	**5.6**	5.7	**5.85**	V
		Falling	**5.3**	5.4	**5.55**	V
		Hysteresis	**0.2**	0.27	**0.35**	V
Controller 2 Specification (Boost)						
FB2 Pin Voltage Regulation	V_{FBCH2}	V_{OUT} adjustable	**0.788**	0.8	**0.812**	V
FB2 Pin Leakage Current	I_{FBCH2}				**0.25**	µA
Forward CH2 Cycle-by-Cycle current limit	$I_{LMT1CH2+}$	ISEN2P-ISEN2N	**64**	80	**100**	mV
Forward CH2 Hiccup Current Limit	$I_{LMT2CH2+}$	ISEN2P-ISEN2N	**80**	100	**124**	mV
Reverse CH2 Current Limit	$I_{LMTCH2-}$	ISEN2P-ISEN2N	**-50**	-40	**-33**	mV
CH2 zero cross	I_{ZCDCH2}		**-4**	2	**9**	mV
CH2 Short Dead Time	T_{DTLH2S}	Low-side low to high-side high, See configuration Table 4.	**30**	43	**70**	ns
		High-side low to low-side high, See configuration Table 4.	**15**	27	**40**	ns
CH2 Long Dead Time	T_{DTLH2L}	Low-side low to high-side high, See configuration Table 4.	**70**	100	**120**	ns
		High-side low to low-side high, See configuration Table 4.	**70**	100	**120**	ns
CH2 Maximum Duty	$T_{DTMAXCH2}$			90		%
CH2 Minimum On-time	$T_{ONMINCH2}$		**15**	25	**35**	ns
CH2 Minimum Off-Time	$T_{OFFMINCH2}$		**30**	40	**55**	ns
CH2 Soft-Start Time	T_{SSCH2}			4.5		ms
Boost Error Amp (OTA) GM	$CH2EA_{OTA}$			1.7		mS
BOOT2 Refresh	$V_{B2RFRESH}$	Rising	**3.3**	3.5	**3.7**	V
		Falling	**3.2**	3.4	**3.6**	V
		Hysteresis	**0.04**	0.08	**0.16**	V
CH2 Overvoltage Protection	$CH2_{OVP}$	Rising	**105**	107	**109**	%
		Falling	**103**	105	**107**	%
		Hysteresis	**1.5**	2.2	**3**	%
CH2 Undervoltage Protection	$CH2_{UVP}$	Rising	**93**	95	**97**	%
		Falling	**91**	93	**95**	%
		Hysteresis	**1.5**	2.2	**3**	%
Output Drivers						
High-Side Drive Source Current	$I_{HS,SRC}$	V_{HS} - V_{LX} = 2.5V, V_{BOOT} - V_{LX} = 4.4V		2		A
High-Side Drive Source Resistance	$R_{HS,SRC}$	100mA source current, V_{BOOT} - V_{LX} = 4.4V		1.2		Ω
High-Side Drive Sink Current	$I_{HS,SNK}$	V_{HS} - V_{LX} = 2.5V, V_{BOOT} - V_{LX} = 4.4V		2		A
Hide-Side Drive Sink Resistance	$R_{HS,SNK}$	100mA sink current, V_{BOOT} - V_{LX} = 4.4V		0.6		Ω
Low-Side Drive Source Current	$I_{LS,SRC}$	V_{LS} - V_{PGND} = 2.5V, VCC = 5V		2		A
Low-Side Drive Source Resistance	$R_{LS,SRC}$	100mA source current, VCC = 5V		1.2		Ω

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
Low-Side Drive Sink Current	$I_{LS,SNK}$	V_{LS} - V_{PGND} = 2.5V, V_{CC} = 5V		3		A
Low-Side Drive Sink Resistance	$R_{LS,SNK}$	100mA sink current, V_{CC} = 5V		0.55		Ω
Input Pins						
EN1 Input Low Voltage threshold	VIL_{EN1}	EN1 = CH1 = buck turned OFF; CH2 can be ON/OFF	**0.4**	1.0		V
EN1 Input High Voltage threshold	VIH_{EN1}	EN1 = CH1 = buck turned ON; CH2 can be ON/OFF		1.2	**1.4**	V
EN1 Leakage Current	ILK_{EN1}		**-0.5**		**0.5**	µA
EN2 Input Low Voltage threshold	VIL_{EN2}	EN2 = CH2 = Boost turned OFF; CH1 is always ON	**0.4**	1.0		V
EN2 Input High Voltage threshold	VIH_{EN2}	EN2 = CH2 = Boost turned ON; CH1 is always ON		1.2	**1.4**	V
EN2 Leakage Current	ILK_{EN2}		**-0.5**		**0.5**	µA
SYNC Input Low Voltage	VIL_{SYNC}				**0.3 x VCC**	V
SYNC Input High Voltage	VIH_{SYNC}		**0.7 x VCC**			V
SYNC Pulse Width High	$T_{SYNCMINH}$		**50**			ns
SYNC Pulse Width Low	$T_{SYNCMINL}$		**50**			ns
Switching Frequency SYNC Range	f_{SYNC}		**0.2**		**2.2**	MHz
CNT/CNT2/VSEL Level 0 Voltage	V_0				**35**	mV
CNT/CNT2/VSEL Level 1 Voltage	V_1		**75**		**180**	mV
CNT/CNT2/VSEL Level 2 Voltage	V_2		**225**		**360**	mV
CNT/CNT2/VSEL Level 3 Voltage	V_3		**415**		**560**	mV
CNT/CNT2/VSEL Level 4 Voltage	V_4		**615**		**870**	mV
CNT/CNT2/VSEL Level 5 Voltage	V_5		**940**		**1240**	mV
CNT/CNT2/VSEL Level 6 Voltage	V_6		**1.33**		**1680**	V
CNT/CNT2/VSEL Level 7 Voltage	V_7		**1.78**		**VCC**	V
Output Pins						
PGOOD1 Pin Voltage	VOL_{PGOOD1}	V_{OUTCH1} = OFF; Sink Current = 3mA		0.3	**0.6**	V
PGOOD2 Pin Voltage	VOL_{PGOOD2}	V_{OUTCH2} = OFF; Sink Current = 3mA		0.3	**0.6**	V
PGOOD1 Pin Leakage Current	ILK_{PGOOD1}	V_{PULLUP} = 5V		0.01	**1**	µA
PGOOD2 Pin Leakage Current	ILK_{PGOOD2}	V_{PULLUP} = 5V		0.01	**1**	µA
PGOOD1 Pin Filter Delay	T_{PGOOD1}		**10**	15	**20**	µs
PGOOD2 Pin Filter Delay	T_{PGOOD2}		**10**	15	**20**	µs
Thermal Shutdown	T_{OTP}	Rising	**151**	160	**175**	°C
		Falling		145		°C
		Hysteresis		15		°C

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
TERM Pin Resistance	R_{TERM}		**55**	85	**170**	**Ω**
TERM Leakage Current	ILK_{TERM}			0.01	**1**	µA

Notes:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for T_A = +25°C and V_{IN} = 12V.
8. Quiescent current measurements are taken when the output is not switching. (Condition VIN = 12V, VOUT1 = 5V, EXTSUP = VOUT1)

3. Typical Perfomance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 6V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation.

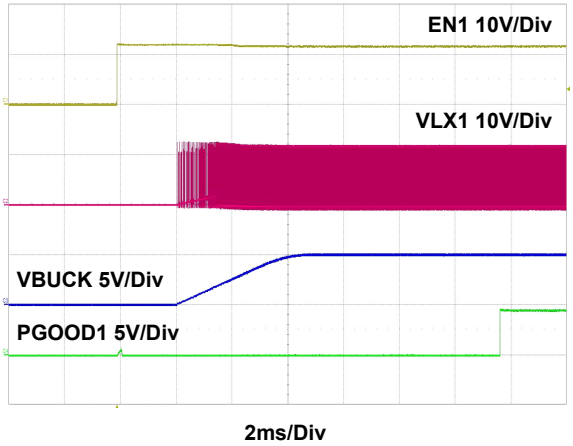


Figure 5. Buck 1 Start-Up with 10 A Load

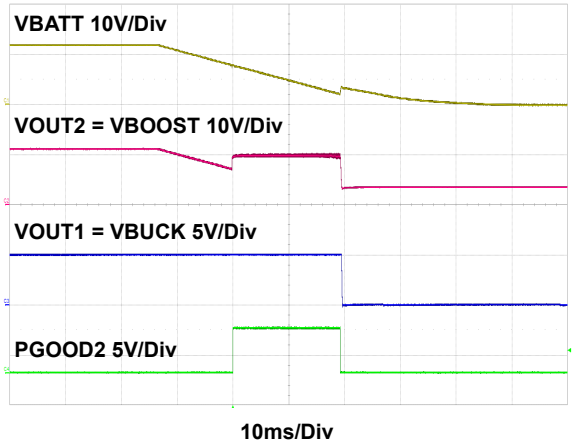


Figure 6. V_{IN} Fall with BOOST Turn ON/OFF

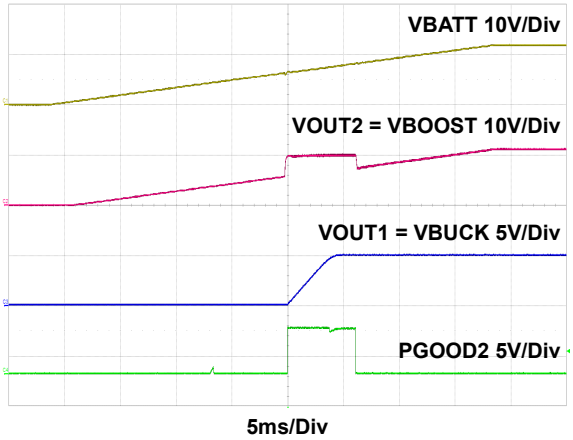


Figure 7. V_{IN} Rise with BOOST Turn ON/OFF

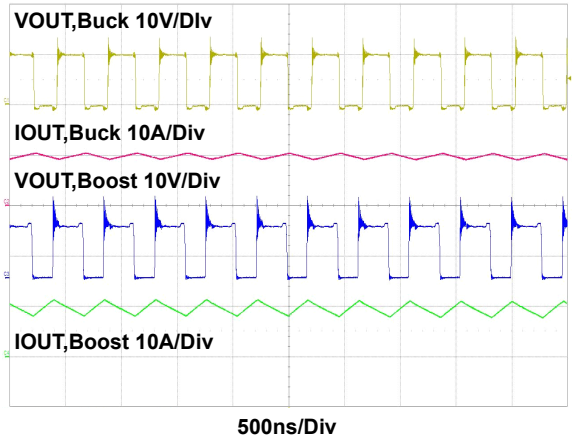


Figure 8. Phase Shift with f_{SW}, Buck = f_{SW}, Boost = 2.2MHz

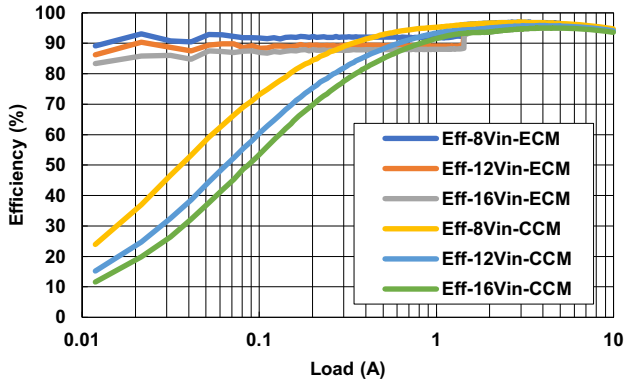


Figure 9. Buck Efficiency (VOUT1 = 5V, f_{SW} = 400kHz)

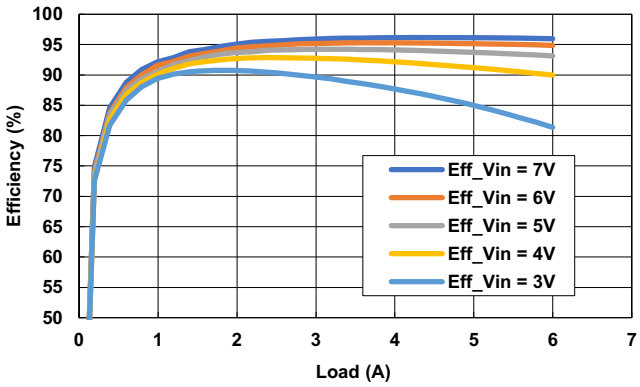


Figure 10. Boost Efficiency (VOUT2 = 10V, f_{SW} = 400kHz)

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 6V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation. **(Continued)**

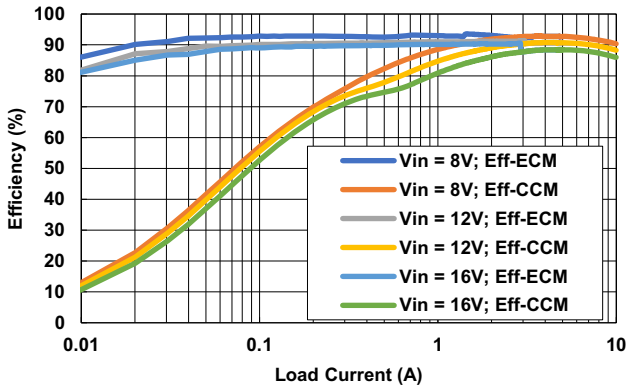


Figure 11. Buck Efficiency (VOUT1 = 5V, f_{SW} = 2.2MHz)

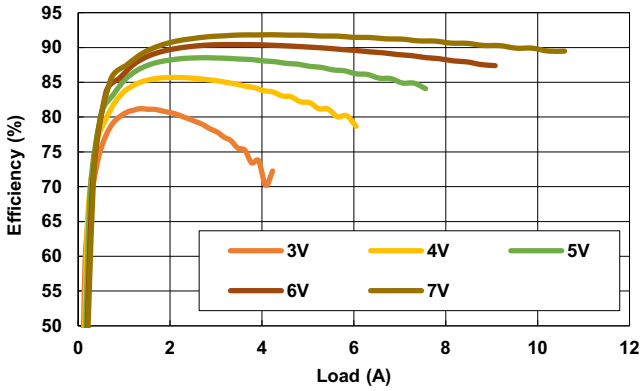


Figure 12. Boost Efficiency (VOUT2 = 10V, f_{SW} = 2.2MHz)

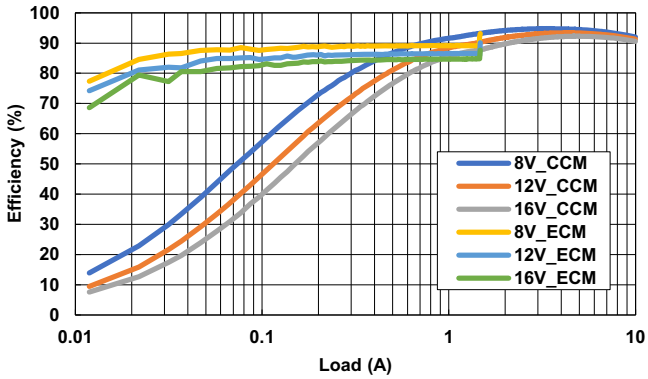


Figure 13. Buck Efficiency (VOUT1 = 3.3V, f_{SW} = 400kHz)

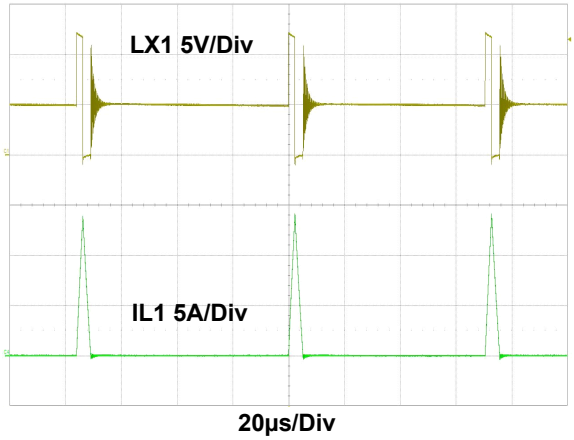


Figure 14. Steady-State ECM Operation with IOUT1 = 0.5A

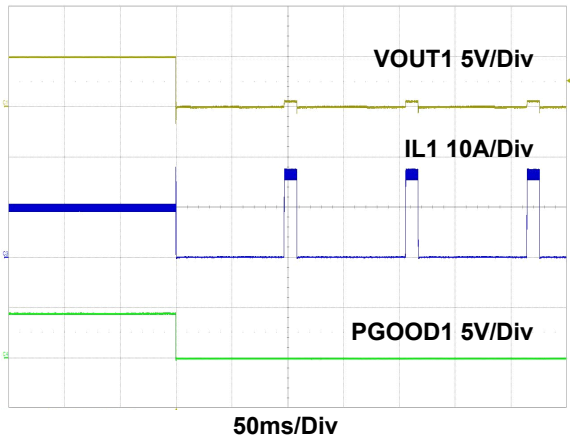


Figure 15. Buck with 10 A Load, then Short Output

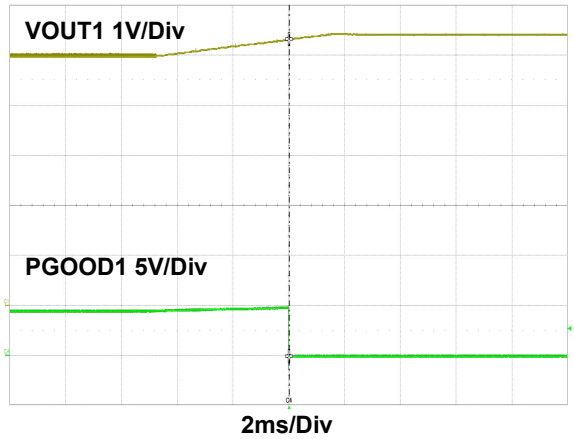


Figure 16. Buck1 Overvoltage Detection

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 6V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation. **(Continued)**

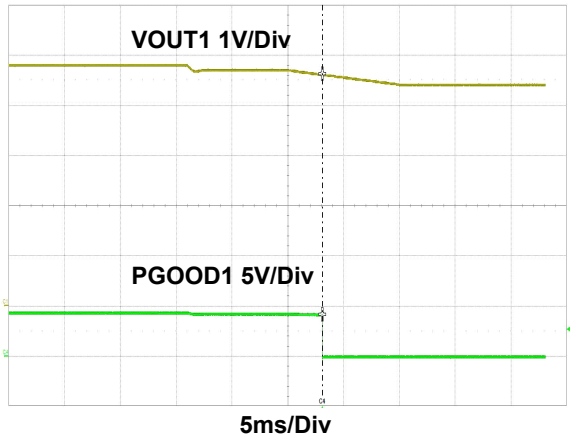


Figure 17. Buck1 Undervoltage Detection

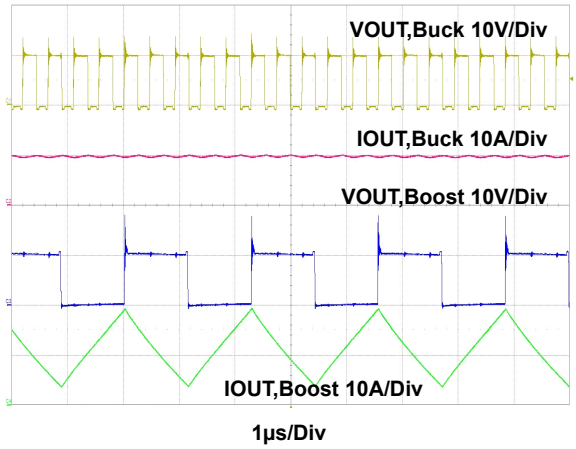


Figure 18. Phase Shift with f_{SW}, Buck = 2.2 MHz and f_{SW}, Boost = 440kHz

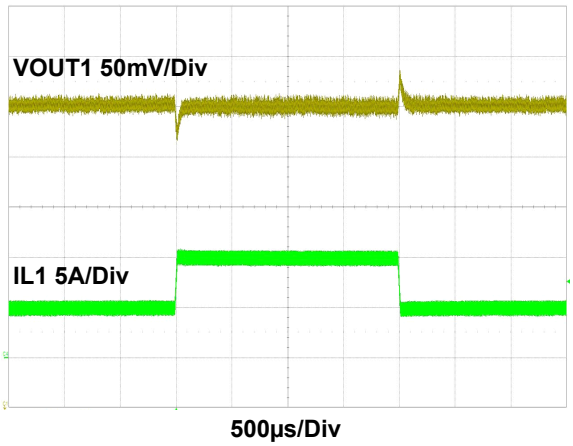


Figure 19. Buck1 Load Transient from 5A to 10A in FCCM

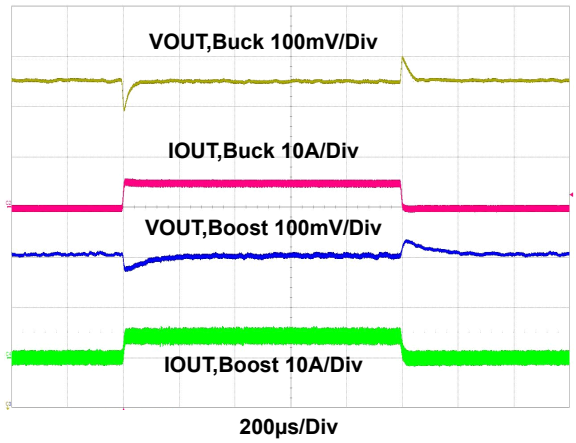


Figure 20. Buck/Boost Transient 0A to 5A

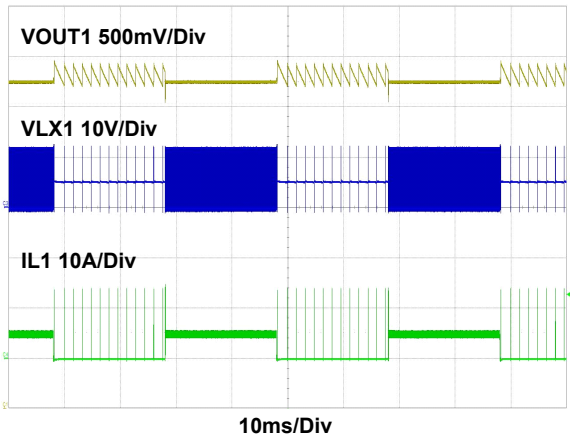


Figure 21. Buck1 Load Transient from 0A to 5A with ECM Enabled

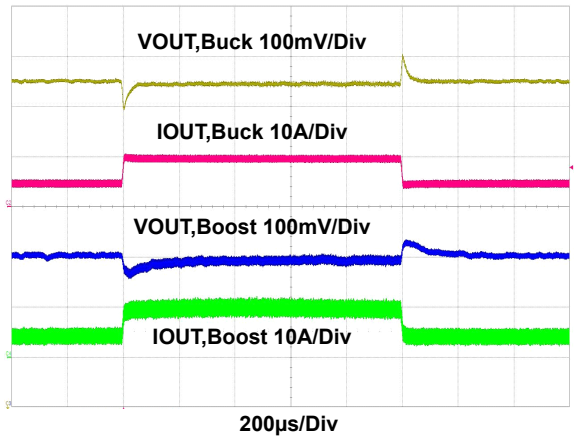


Figure 22. Buck/Boost Transient 5A to 10A

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 6V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation. **(Continued)**

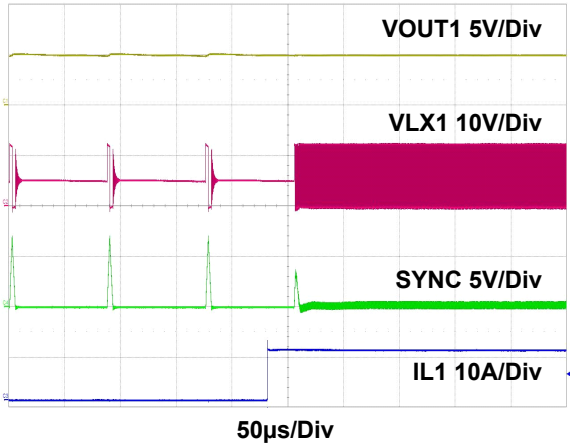


Figure 23. Buck1 SYNC High ECM Exit

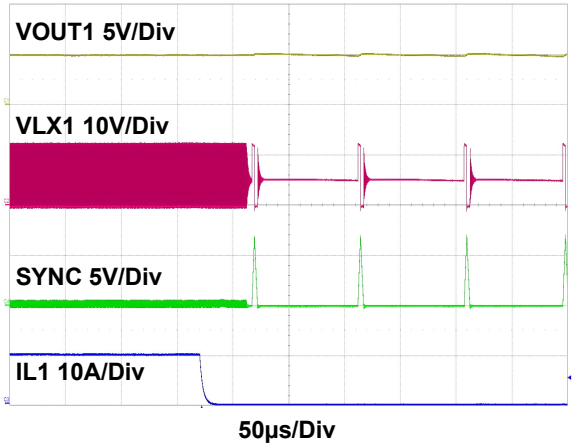


Figure 24. Buck 1 SYNC Low ECM Entry

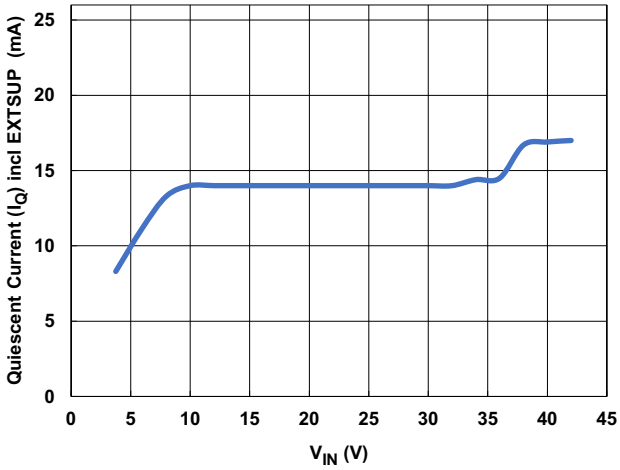


Figure 25. I_Q vs V_{IN}

4. Functional Description

The ISL78263 has controllers that support two DC/DC channels Buck 1 and Boost 2 that can be configurable in various modes and operate across a V_{IN} range of 2.1V to 40V after the V_{IN} UVLO threshold (5.65V typical) has been exceeded. Channel 1 operates as a buck converter and can be configured as a fixed 3.3V, fixed 5.0V, or as an adjustable output voltage from 0.8V to 5.0V. Channel 2 is a boost circuit that can be configured to operate in different modes as defined in configuration Table 3. The combination of a cold crank boost feeding a buck is required to support applications requiring a buck output that remains in regulation during battery dropouts during cold crank periods. Alternatively, the boost can be configured to operate independently of the buck to boost the input voltage from 5V to 40V. The ISL78263 can support significantly more than 10A of load current with both the buck and boost converter if the proper external components are selected.

4.1 Synchronous Buck and Boost

To improve efficiency, the ISL78263 employs both a synchronous buck and synchronous boost architecture. In a synchronous buck, the LS1 output drives the synchronous low-side MOSFET, which replaces the freewheeling diode and improves the power losses by lessening the voltage drop of the freewheeling diode while the high-side MOSFET is off. The HS1 signal provides buck controller PWM information and is complementary to the LS1 signal. HS1 is powered from a charge pump that generates a voltage between BOOT1 and LX1 by using an external diode from VCC to BOOT1 to charge an external capacitor between BOOT1 and LX1 when LS1 is high and LX1 is low.

In a synchronous boost, the circuit function of the high-side MOSFET(s) and low-side MOSFET(s) are interchanged. The HS2 output drives the synchronous high-side MOSFET, which replaces the blocking/freewheeling diode and improves the power losses by lessening the voltage drop of the freewheeling diode while the low-side MOSFET is off. The LS2 signal is complementary to the HS2 signal and provides boost controller PWM information to the low-side MOSFET. The HS2 signal is powered from a charge pump that generates a voltage between BOOT2 and LX2 using an external diode from VCC to BOOT2 to charge an external capacitor between BOOT2 and LX2 when LS2 is high and LX2 is low.

4.2 Configuration Tables for VSEL, CNT, and CNT2

VSEL, CNT, and CNT2 are the three configuration pins that are available to select operational settings in the ISL78263.

4.2.1 VSEL

The VSEL pin allows the selection of Channel 1 voltage as fixed at 5V or 3.3V, or adjustable with an external voltage divider. The operating mode of Channel 2 can be programmed as a cold crank with the boost converter only operational with 2.1V < V_{BAT} < 8V. Conversely, the Channel 2 Boost can be operated individually, continuing to boost the input until the input exceeds the programmed boost output voltage. Select values for the VSEL configuration resistor to ground are listed in Table 3.

Table 3. VSEL Configuration Values

Resistor (Ω)	Ch1 V_{OUT} (V)	Ch2 Operating Mode
75k	5	Individual Boost
54.9k	5	Cold Crank Boost
37.4k	Adjustable	Individual Boost
24.9	3.3	Individual Boost
14.7k	Adjustable	Cold Crank Boost
6.04k	3.3	Cold Crank Boost

4.2.2 CNT

The CNT pin allows the selection of spread spectrum ON with +6% or +12% modulation depth, or it allows selection of spread spectrum OFF. Also, the dead time is selectable as 30ns for high-frequency operation for smallest component size using MOSFETS with small gate charge, or 100ns for larger gate charge MOSFETs with lower Rds, on values, common with lower switching frequencies for maximum efficiency. Select values for CNT configuration are listed in Table 4.

Table 4. CNT Configuration Values

Resistor (kΩ)	Spread Spectrum	Dead Time (ns)
75	+12%	Short (30)
54.9	+12%	Long (100)
37.4	+6%	Short (30)
24.9	+6%	Long(100)
14.7	Off	Short (30)
6.04	Off	Long (100)

4.2.3 CNT2

The CNT2 pin allows selection of minimum boot refresh time of 360ns or 180ns, with the longer time preferred for typical applications. CNT2 also allows programming the Channel 2 boost frequency to be equal to Channel 1 buck frequency or as 1/5 of the Channel 1 buck frequency. Select values for CNT2 configuration are listed in Table 5.

Table 5. CNT2 Configuration Values

Resistor (kΩ)	Boot Refresh Time (ns)	Boost Frequency
75	360	1 x f_{SW} buck
54.9	360	1/5 x f_{SW} buck
24.9	180	1 x f_{SW} buck
6.04	180	1/5 x f_{SW} buck

4.3 Start-Up Operation in Cold Crank Configuration

When V_{BAT} is applied to the circuit, the battery voltage is applied to the V_{BOOST} circuit node through the body diode of Channel 2 boost high-side MOSFET. The initial ISL78263 start-up procedure requires that V_{IN} is greater than the undervoltage lockout rising threshold, which has a maximum value of 5.845V. In cold crank applications, Channel 1 Buck is normally enabled first using EN1, which is biased to VIN, or can be simultaneously enabled with the boost converter EN2 biased to VCC or a separate 5V level. This configuration allows the internal LDO regulator to supply V_{CC} voltage and begin switching operation and the buck output goes through a soft-start sequence. In the cold crank application, when EN2 is logic high, Converter 2 boost ON/OFF operation is controlled by the actual battery voltage level that is sensed through the ISEN2P pin. After the output reaches a steady-state level, the power-good pin signal (open-drain) can implement additional sequencing requirements. The IC continues operation until the V_{CC} voltage level reduces below the V_{CC} UVLO falling threshold or when VIN falls below 2.1V (typical).

To support a typical cold crank application, both EN1 and EN2 should be logic high within respective voltage levels discussed in “Enable 1 and Enable 2 Operational Levels” on page 20. In a cold crank scenario, the Converter 2 boost is enabled but not operating in Boost mode when V_{BAT} is at the typical level of 12V. However, as V_{BAT} drops below 8V, the boost circuit quickly engages to raise and maintain the boost output voltage feeding Converter 1 buck output to a required level, typically 10V. The boost circuit continues to operate as V_{BAT} drops to the boost turn OFF falling threshold of 2.1V typical value. The Converter 2 signal PGOOD2 is an open drain when both the boost converter is ON and the boost output voltage is within the programmed range.

4.4 Start-Up Operation with Individual Buck and Boost

The ISL78263 start-up procedure requires that V_{IN} is greater than the undervoltage lockout rising threshold, which has a maximum value of 5.845V. After this condition is met, the startup can be initiated by driving either EN1 or EN2 to its respective logic high level, which activates the internal regulator to supply VCC to provide bias for control circuitry and gate drive for the external MOSFETs.

The Channel 1 Buck operation is controlled by EN1 pin status. After EN1 transitions to logic high, the buck output voltage goes through a soft-start interval to increase the output voltage to the programmed level. After reaching a steady-state level, the PGOOD1 pin signal goes to an open drain and can be used in implementing additional sequencing requirements.

For use in individual boost configuration, the Converter 2 Boost operation is controlled by the EN2 pin status. Before the boost is enabled, the output V_{BOOST} is charged to a voltage one diode drop below V_{IN} through the body diode of the high-side MOSFET. After being enabled, the boost converter goes through a soft-start interval to increase the output voltage to the programmed level. After reaching a steady-state level, the PGOOD2 pin signal goes to an open drain and can be used in implementing additional sequencing requirements.

4.5 Enable 1 and Enable 2 Operational Levels

The EN1 pin can withstand high voltage and can connect to VIN through a resistor for initial start-up. The EN2 pin can only accept voltage from 0V to 5.5V and can be enabled uisng a pull-up resistor to VCC after EN1 is high or through an external source with proper voltage level. For simultaneous start-up of Buck 1 and Boost 2, the enable pins (EN1 and EN2) can be resistively pulled to respective logic levels when V_{IN} is applied. The IC continues operation until the V_{CC} voltage level reduces below the V_{CC} UVLO falling threshold or when VIN falls below 2.1V threshold (typical).

4.6 Internal LDO and EXTSUP

The internal LDO derives power from VIN and provides an output on VCC of 5.0V (typical) during the start-up of the device and can also be used in continuous operation. Because VCC provides bias power for both IC supply and gate drive current, this can produce high power dissipation in the internal regulator. To minimize IC dissipation and increase system efficiency the EXTSUP pin provides an input that can supply 5V from a voltage source other than the internal LDO regulator. An internal circuit senses the EXTSUP voltage and switches it to supply VCC if within the acceptable range. If EXTSUP is not used, Pin 20 is grounded, and the internal LDO supplies VCC.

In a typical application, the Channel 1 output voltage of 5V is connected to the EXTSUP pin so that after start-up VOUT1 can supply bias power to eliminate LDO dissipation in normal operation. During restarts, the internal EXTSUP switch is turned OFF, and this power handover between LDO and EXTSUP pin takes place during each power-up. If Channel 1 and Channel 2 are not 5V outputs, such as 3.3V, the EXTSUP can accept 5V from an independent source, such as a small 3.3V to 5V boost converter. If the external bias is applied before VIN is applied, the start-up enable circuit should be powered from the external bias source (and not VIN).

4.7 Oscillator

The buck switching frequency is programmable in the range from 0.2MHz to 2.2MHz by connecting a resistor from the RT pin to GND. External synchronization is possible in the range 0.2MHz to 2.2MHz by connecting an external clock to the SYNC pin. The device syncs on the rising edge. The RT and SYNC pins set the mode of operation per Table 6.

Table 6. Oscillator and SYNC Configuration

Pin	Connect to	Buck Frequency
RT	Resistor to GND	Programmable range 0.2MHz to 2.2MHz
SYNC	VCC	Forced CCM mode
	GND	Forced CCM, DEM, ECM, Automatic
	0.2MHz < External Clock < 2.2MHz	Overrides internal frequency

Figure 26 shows the relationship between RT and the switching frequency.

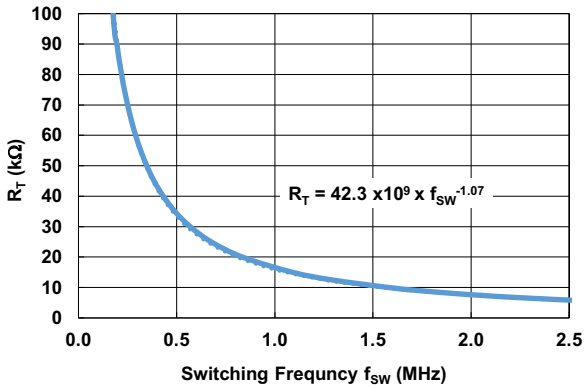


Figure 26. R_T vs f_{SW}

4.8 Phase Shift

The Channel 1 Buck and Channel 2 Boost are 180° out of phase, which helps in lowering the noise by reducing the peak current during switching. The 180° phase shift is between the buck high-side MOSFET conduction time and the boost low-side MOSFET conduction time. The Spread Spectrum is derived from an internal triangular wave oscillator with a frequency of 3kHz and a modulation depth of 6% or 12% in a pseudo-random manner. Spread spectrum is configured using the CNT pin, which selects spread spectrum ON/OFF and modulation depth using a 5-bit resolution that amounts to 32 discrete steps.

4.9 PGOOD Signals

The power-good indicators on Pin 12 (PGOOD1) and Pin 32 (PGOOD2) are provided for fault monitoring on the respective buck and boost converters. The PGOOD pins provide an open-drain logic output to indicate that the start interval is completed and the output voltage is within the specified range. An external pull-up resistor (10kΩ to 100kΩ) is required between the PGOOD pin and VCC or an external power supply (5.5V maximum). This pin is pulled low during soft-start.

4.10 Buck Stage (Converter 1)

4.10.1 Operation

The synchronous buck stage operates across an input voltage range of 3.75V to 42V and is offered in fixed output voltage options of 5.0V and 3.3V, or adjustable. In adjustable mode, Channel 1 output can be set in a range V_{OUT1} = 0.8V to 5V using an external resistive voltage divider from VOUT1 to FB1, and Ground. The adjustable range for VOUT1 is limited by the voltage rating of the current sense circuitry.

Equation 1 can derive the R_{UPPER1} and R_{LOWER1} resistor values:

(EQ. 1) $$V_{OUT1} = 0.8V \bullet (1 + (R_{UPPER1})/(R_{LOWER1}))$$

where R_{UPPER1} is the resistor between VOUT1 and FB1, and R_{LOWER1} is the resistor between FB1 and GND.

The minimum input voltage selection for a given V_{OUT} should consider the headroom required for regulation. For example, a V_{OUT} of 5V would need a minimum V_{IN} of 5.7V for normal operation. The V_{OUT} accuracy is ±1% in normal mode and is ±3% in the Energy Conservation Mode (ECM), which is a low power mode. The error amplifier compensation is achieved by using a series resistor and capacitor combination from the COMP1 pin to GND.

4.10.2 Bootstrap for High-side NMOS Drive

To turn on the high-side MOSFET properly, the ISL78263 employs a bootstrap circuit using an external boot capacitor (C_{BOOT}) in conjunction with an external diode. To maintain the current on the inductor at the time the high-side MOSFET turns off, the LX node goes down to GND level at low-side MOSFET turn-on. While in this low-side MOSFET on period, the diode connected from VCC to boot capacitor is forward-biased and charges up the boot capacitor. When the low-side MOSFET is turned off and the high-side MOSFET is turned on after dead time, the LX node goes up to V_{IN} level and the BOOT pin bias is V_{IN} + V_{CC} - VF to drive the high-side driver circuitry.

4.10.3 Boot Refresh

The BOOT to LX voltage is constantly monitored and if it is lower than 3.4V ±0.2V, the device inserts a 180ns/360ns pulse on to the low gate on-time. If in the Pulse Skip mode, the ISL78263 inserts a 180ns/360ns low gate on-time before the high gate starts switching. When in the Low Power mode, the device inserts a 360ns low gate on-time before the high gate starts switching. It is assumed that logic level FETs are being used.

4.10.4 Current Limit and Overcurrent Protection

The ISL78263 requires that the buck Converter 1 inductor current is sensed by a current sense amplifier to provide both control and overcurrent protection. This is accomplished by inserting a current sense resistor in series with the power inductor with a resistance value that produces a 50mV signal between ISENxP and ISENxN when the full load current is applied to the output in FCCM. Inductor DCR current sensing can also be used. If the load is increased such that the voltage across the current sense resistor is 80mV, the circuit begins limiting current on a cycle-by-cycle basis (OC1). If the load continues to increase so that the current sense resistor signal reaches 100mV, the hiccup current limit (OC2) forces the IC to shut down and a restart is attempted.

4.10.5 Undervoltage and Overvoltage

The ISL78263 Converter 1 buck circuit has an overvoltage limit of +7% typical with a hysteresis of 2% and an undervoltage limit of -7% typical with a hysteresis of 2%. The ISL78263 Converter 2 boost does not have an overvoltage detection function but has undervoltage limit of -7% typical with a hysteresis of 2%. At startup, PGOOD1 and PGOOD2 are pulled low using an internal MOSFET in an open-drain configuration, and when the respective output exceeds the undervoltage threshold, the corresponding PGOOD signal rises using an external pull-up resistor connected to VCC. If an overvoltage condition is detected on Buck Converter 1 during operation, PGOOD1 is pulled low and the circuit enters a hiccup mode of operation with successive shutdowns and restarts to detect if the overvoltage fault is cleared. If an undervoltage condition is detected on either converter during operation, the controller continues to operate and the corresponding PGOOD indicator is pulled low.

4.11 Boost Stage (Converter 2)

4.11.1 Operation

The synchronous boost stage operates across an input voltage range of 3.5V to 42V and has an adjustable output voltage option. The V_{OUT} can be set using two resistors (see Boost Output Voltage Programming). The main purpose of this boost converter is to supply energy during a battery voltage drop to less than 3V during cold crank periods. To achieve this, the boost converter is made active in a range of 2.1V < V_{BAT} < 9V. The high-side and low-side FET drivers of the ISL78263 can source a current of = 2A and sink = 3A.

4.11.2 Boost Output Voltage Programming

Connecting a resistor from VOUT2 to the FB2 pin and another from FB2 to GND programs the output voltage of the ISL78263. The required resistor values for a given V_{OUT2} can be calculated by using Equation 2.

Equation 2 can derive the R_1 and R_2 resistor values:

(EQ. 2)

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right)$$

where R_1 is the resistor between VOUT2 and FB2, and R_2 is the resistor between FB2 and GND.

When designing a PCB, include a GND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Place resistors R_1 and R_2 close to the FB pin.

4.11.3 Current Limit and Overcurrent Protection

The ISL78263 requires that the boost Converter 2 inductor current is sensed by a current sense amplifier to provide both control and overcurrent protection. This is accomplished by inserting a current sense resistor in series from V_{IN} to the power inductor with a resistance value that produces a 50mV signal between ISEN2P and ISEN2N when the full load current is applied to the input and output in FCCM. Inductor DCR current sensing can also be used. If the load is increased such that the voltage across the current sense resistor is 80mV, the circuit begins limiting current by reducing the on-time of the low-side MOSFET on a cycle-by-cycle basis (OC1). However, if the low-side FET is not turned ON, the current continues to flow from VIN though the inductor and body diode of the high-side MOSFET to the output, a characteristic of the boost converter. The ISL78263 Boost reverse current limiting is at -40mV typical.

4.11.4 Undervoltage and Overvoltage

The ISL78263 boost circuit has an overvoltage limit of +7% typical with a hysteresis of 3%. The device has an undervoltage limit of -7% typical with a hysteresis of 3%.

4.11.5 Over-Temperature Shutdown

The ISL78263 has an over-temperature shutdown threshold of 160°C with a hysteresis of 15°C. When crossing the threshold, the device shuts down for 100ms and then tries to restart in 100ms intervals. The device turns on again when the over-temperature fault is cleared.

4.12 Energy Conservation Mode (ECM)

The ISL78263 can be configured to allow Controller 1 (Buck) to enter Energy Conservation Mode (ECM) to reduce quiescent power consumption as the load current is reduced. ECM allows a buck converter to supply from a car battery to provide a 5V output (with no load) while drawing less than 6µA average current from the battery. During ECM operation, the ISL78263 buck converter delivers power pulses to the output filter and load at a frequency that is much lower than the normal switching frequency range of 200kHz to 2.2MHz. Each power pulse supplies sufficient energy to supply small load currents with no requirement for a high-frequency multi-pulse burst operation as described in the following sections. In the time interval between consecutive ECM power pulses, the ISL78263 is able to drastically reduce its operating current requirement to minimize average standby current drawn from the input supply, which is normally a car battery. With proper component selection, the circuit can automatically enter or exit ECM with minimal disturbance on the output within a wide range of operating conditions.

4.12.1 Overview of ECM Setup and Operation

Many factors determine whether ECM can be entered, maintained, or exited. If a converter is configured to allow ECM at light loads, it automatically exits ECM under certain conditions. Therefore, ECM can be allowed at light loads, but the circuit functions in Fixed Frequency Continuous Conduction Mode (FCCM) if load currents exceed one-third of the full load level as defined in the following.

The factors that impact ECM operation are discussed in the sections that follow:

- SYNC voltage level
- VIN level
- EN1 and EN2 status
- R_{SEN} value
- Full load current determined by 50 mV across R_{SEN}
- Output voltage ripple
- Load current changes

To permit ECM operation, the voltage on VIN (Pin 26) must be in a range from 6V to 18.5V and the SYNC pin must be logic low. If SYNC is connected to VCC directly the circuit always operates in FCCM. To command ECM enter/exit on-the-fly a simple switch circuit can be used to drive the SYNC pin from logic high (VCC) to GND to inhibit or permit ECM. SYNC can also be held low to keep the converter in ECM when the load is small, then SYNC can be driven to provide an external clock for synchronized operation which forces ECM exit and FCCM operation.

In the ISL78263, only the Channel 1 buck converter is able to enter ECM and the boost converter must be disabled (EN2 = 0V). The RT pin is a good indicator to monitor which determines the mode of operation for the converter. In normal FCCM mode, RT has a 0.5V level and while in ECM, RT is pulled to 0V by an internal circuit.

If ECM is enabled (SYNC = GND, EN1 = pull-up to VIN, EN2 = 0V) during initial start-up, the buck output ramps up operating in FCCM/DEM throughout the soft-start interval and the power-good output transitions high. When the buck meets ECM entry criteria, ECM operation begins 20ms to 30ms after start-up.

Steady-state buck ECM power pulse operation uses a voltage comparator in conjunction with an accurate current sense resistor and amplifier to detect loading and current thresholds. Between ECM power pulses, the ISL78263 operates with extremely low current, which uses a voltage comparator to sense the output voltage level as it slowly decays with a rate proportional to the output load current. During this interval, the output capacitors supply the load on the output. When the comparator detects the lower voltage threshold, the IC turns fully on to generate a power pulse that stores energy in the output inductor to replenish output capacitors and supply loading if present. The ECM power pulse can be terminated by two methods:

- Reaching peak inductor current threshold
- Reaching output voltage OVP level

Individual ECM power pulses are generated by the following procedure. First, the high-side MOSFET is turned ON to apply VIN-VOUT across the output inductor to ramp the inductor current up at a controlled rate. The current sense amplifier monitors the voltage level across the current sense resistor until the voltage reaches 60mV, which equates to a peak inductor current I_{PK}, ECM, which is 120% of the full load current. When the 60mV threshold is attained, the high-side MOSFET is turned off, the low-side MOSFET is turned on, applying V_{OUT} across the output inductor. This forces the inductor current to ramp down to approximately 0A at which time an internal zero current comparator turns the low-side MOSFET off. After the power pulse, the IC returns to ultra-low quiescent current consumption. Alternatively, if the output rises to approximately 3% of V_{OUT} before the peak current is detected, the high-side pulse is truncated.

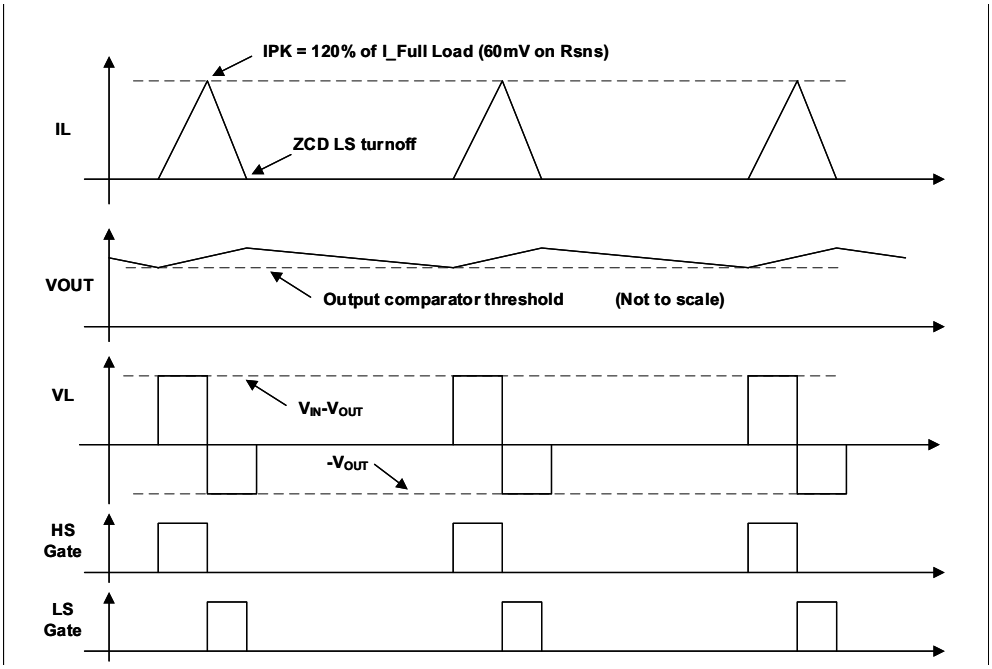


Figure 27. Energy Conservation Mode (ECM) Operational Waveforms

4.12.2 ECM Load Based Entry and Exit

The current sense resistor and amplifier set thresholds to monitor and control ECM entry, exit, and power pulse generation. To understand ECM power pulse operation, first, note that the current sense resistor (in series with the power inductor) is initially selected to produce a 50mV signal between ISENxP and ISENxN when the full load current is applied to the output in FCCM. The ISL78263 can operate and transition in multiple modes, and this section focuses on ECM entry and exit as the load on the buck is changed relatively slowly. If ECM is allowed (SYNC = GND) and the load reduces to approximately 1/6 of the full load setting, the signal across the current sense resistor is 8mV and the circuit enters ECM. The circuit remains in ECM as the load is further reduced to minimal or no load. If the load increases, the circuit exits ECM when the current sense amplifier surpasses 18mV, which indicates the load has surpassed approximately 1/3 of the full load current.

The datasheet has presented operation as the load current has changed slowly for ECM entry/exit. However, ECM entry/exit is designed to support transient load step requirements as needed. For example, if the current is large and steps to a small value (less than 1/6h of $I_{OUT,nom}$), the current-sense circuitry detects low current and enters ECM within a few milliseconds. Conversely, if the converter is operating in ECM with a small load and a large load step is applied, the circuit responds with more power pulses to support the full load rating as necessary. During the large load step, the V_{OUT} comparator continues to monitor the output voltage following the initial power pulse from 0A to I_{PK} and back to 0A. If the output voltage is below the required level, the converter immediately produces a second power pulse. If V_{OUT} is still below the required level after the second power pulse peak, the subsequent pulses have a higher valley, greater than 0, and no tri-state period. The peak-valley sequence continues until V_{OUT} reaches the required level, or eight pulses are counted, and the circuit transitions to FCCM. **Note:** The average of the peak valley operation from 60mV to 45mV is capable of supplying the full load, which equates to a 50mV level.

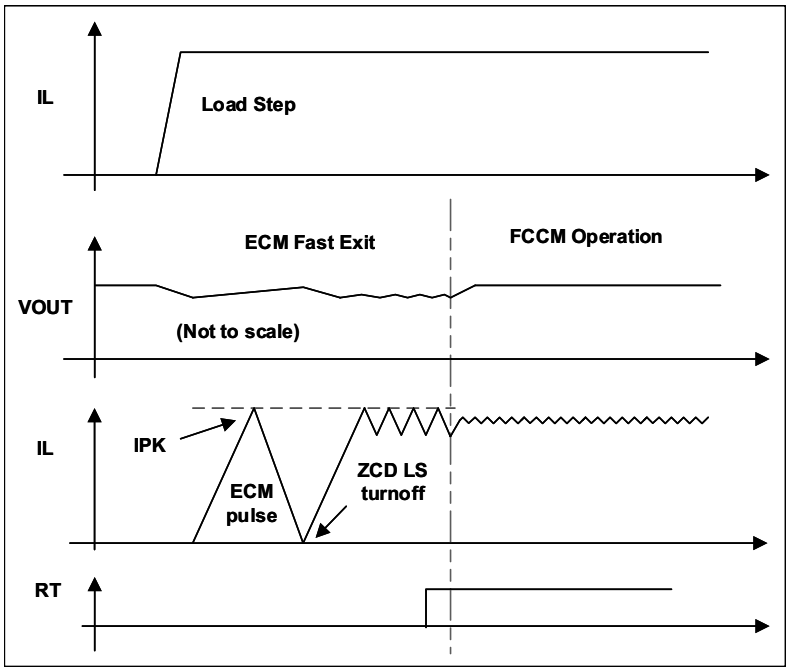


Figure 28. ECM Fast Exit with Large Load Step

5. Application Information

Several factors need to be considered in the selection of the external components for buck regulators. This section discusses some examples of how to decide the parameters of the external components based on the typical application schematic shown in Figure 3. In the actual application, the parameters may need to be adjusted and also a few more additional components may need to be added for the application-specific noise, physical sizes, thermal, testing, and other requirements.

5.1 Buck Converter

5.1.1 Buck Inductor Selection

While the buck converter is operating in a stable Continuous Conduction Mode (CCM), the output voltage and on-time of the high-side transistor is determined by Equation 3:

(EQ. 3) $$V_{OUT} = V_{IN} \bullet \frac{t_{ON}}{T} = V_{IN}D$$

where T is the switching cycle ($1/f_{SW}$) and $D = t_{ON}/T$ is the on-duty of the high-side transistor.

Under this CCM condition, the inductor ripple current can be defined as Equation 4:

(EQ. 4) $$I_{L,p\text{-}p} = t_{ON} \bullet \frac{V_{IN} - V_{OUT}}{L} = t_{OFF} \bullet \frac{V_{OUT}}{L}$$

From the previous equations, the inductor value is determined as Equation 5:

(EQ. 5) $$L = \frac{V_{IN} - V_{OUT}}{f_{SW}} \bullet \frac{V_{OUT}}{V_{IN}}$$

In general, when the inductor value is determined, the ripple current varies by the input voltage. At the maximum input voltage, the on-duty becomes the minimum and the ripple current becomes the maximum. So, the minimum inductor value can be estimated from Equation 6.

(EQ. 6) $$L_{min} = \frac{V_{IN} - V_{OUT}}{f_{SW} \bullet \Delta I_{L,\,max}} \bullet \frac{V_{OUT}}{V_{IN,\,max}}$$

In a DC/DC converter design, this ripple current is normally selected to be 20% to 50% of maximum DC output current. A reasonable starting point to adjust the inductor value is around 30% of the maximum DC output current. Increasing the inductor value reduces the ripple current and ripple voltage. However, the large inductance value can increase the response time of the converter to a load transient. Also, this reduces the ramp signal and can cause a noise sensitivity issue.

Under stable operation, the peak current flow in the inductor is the sum of output current and 1/2 of ripple current.

(EQ. 7) $$I_{L,pk} = \frac{I_{L,p\text{-}p}}{2} + I_{OUT}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current can be observed at the start-up or heavy load transient. Therefore, the size of the inductor needs to be determined with the consideration of these conditions. Also, to avoid exceeding the saturation rating of the inductor, Renesas recommends setting the OCP trip point between the maximum peak current and the saturation current rating of the inductor.

Note: The OC1 signal is fixed at 80mV (160% of full load) and the OC2 hiccup threshold is fixed at 100mV; therefore, the inductor should have a saturation value exceeding 2x full load current. The ECM operation is based on a fixed 60mV signal (120% of full load), which is less than the OC1 level, so there are no special considerations for inductor selection for ECM.

5.1.2 Buck Output Capacitor

To filter the inductor current ripples and to have sufficient transient response, output capacitors are required. The current mode control loop allows the usage of low ESR ceramic capacitors for smallest size, and/or electrolytic and polymer capacitors that offer larger capacitance values but with higher ESR and increased physical size. While the ceramic capacitor offers excellent overall performance and reliability, the actual capacitance may be considerably lower than the advertised value when operated with significant DC bias voltage in relation to rated voltage, so the manufacturer information should be carefully reviewed.

The following are equations for the required capacitance value to meet the desired ripple voltage level. Additional capacitance can be used to lower the ripple voltage and to improve transient response.

For the ceramic capacitor (low ESR):

(EQ. 8) $$V_{OUT,rip} = \frac{\Delta I_L}{8 \bullet f_{SW} \bullet C_{OUT}}$$

where ΔI_L is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

Required minimum output capacitance based on ripple current is:

(EQ. 9) $$C_{OUT,min} = \frac{\Delta I_L}{8 \bullet f_{SW} \bullet V_{OUT,rip}}$$

If using electrolytic capacitors, the ESR is the dominant portion of the ripple voltage.

(EQ. 10) $$V_{OUT,rip,ESR} = \Delta I_L \bullet ESR$$

Therefore, to reduce the ripple voltage, select the electrolytic capacitor based on maximum ESR, use multiple capacitors in parallel to reduce the ESR, or increase inductor value to reduce the ripple current.

The output capacitor value selected for FCCM may require adjustment for ECM operation depending on the magnitude of ripple voltage allowed on VOUT. In standard ECM operation when there is no external loading, the output capacitor must absorb the complete pulse of energy from the output inductor peak current of 120% of full load current. Both the capacitance value and ESR should be considered for ECM operation. The capacitance should be large enough to absorb the energy with acceptable voltage rise and the ESR must be small enough to control the potentially large step in voltage equal to Ipk, ECM x ESR.

In addition to output voltage ripple requirements, select the buck output capacitor value in conjunction with the inductor to meet output deviation requirements during normal FCCM operation, ECM (Energy Conservation Mode), and load transients.

Equation 11 calculates the value of C_{OUT} required during load reduction and the output voltage overshoots the nominal level.

(EQ. 11) $$C_{OUT_MIN_STEP_DOWN} = \frac{L\left(I_{STEP} + \frac{I_{RIPPLE}}{2}\right)^2}{2V_{OUT}\Delta V}$$

When the load is increased, the output undershoots the nominal value and the value of C_{OUT} required is calculated using Equation 12.

(EQ. 12)
$$C_{OUT_MIN_STEP_UP} = \frac{L\left(I_{STEP} + \frac{I_{RIPPLE}}{2}\right)^2}{2(V_{IN} - V_{OUT})\Delta V}$$

5.1.3 Buck Input Capacitor

The system input power rail may incorporate a combination of electrolytic and ceramic capacitors to provide a stable input voltage while supplying pulse currents at the buck switching frequency. The voltage rating of the capacitors should exceed the maximum voltage, which can be connected to the input of the regulator; it is common to provide a rating margin over 20% of the maximum input voltage.

The minimum value of the input capacitors can be estimated by limiting the drop in VIN (ΔVIN below) to approximately 1% when delivering the full load current during the on-time of the high-side MOSFET:

(EQ. 13)
$$C_{IN,MIN} = \frac{I_{LOAD,MAX} \bullet D \bullet (1 - D)}{f_{SW} \bullet \Delta VIN}$$

The specific capacitor(s) used should be selected with an RMS current capability exceeding the value estimated by the relation below.

(EQ. 14)
$$I_{CIN,RMS} \cong I_{LOAD,MAX} \bullet \sqrt{D \bullet (1 - D)}$$

5.1.4 Buck MOSFET Selection

The external MOSFETs that are driven by the ISL78263 controller need to be carefully selected to optimize the design of the synchronous buck regulator. The input voltage is typically the automotive range for battery supply, so the MOSFETs are normally rated at 40V BVdss. As the high-side and low-side gate drivers are a 5V output, the MOSFET VGS needs to be specified in this range. The MOSFET should have a low total gate charge (Qgd), low ON-resistance ($r_{DS(ON)}$) at VGS = 4.5V (10mΩ to 20mΩ), and small gate resistance (Rg <1.5Ω is recommended). Renesas recommends that the minimum VGS threshold should be higher than 1.2V, but not exceeding 2.5V to make sure the MOSFETs can be switched off reliably throughout the complete V_{CC} range.

5.1.5 Control Loop Compensation Components for the Buck Converter

Several components selected for the power, filtering, and current sense circuits play a role in the determination of the compensating components.

- R_{SENSE} = 50mV/I_{OUT} = 5mΩ (with I_{OUT} = 10A)
- Ramp slope = 38.1mV per volt of V_{IN}
- Ramp valley = 1V
- Current sense amplifier transconductance = $G_{m,CSA}$ = 91.25µS
- Current feedback resistor value = R_{IFB} = 60kΩ
- Reference voltage V_{REF} = 0.8V
- G_{mea} = 1.7mS

Calculate the current loop pole frequency

(EQ. 15) $$f_{cp} = \frac{R_{sns}}{2\pi \bullet L_{OUT}}$$

Determine PWM_{gain}

(EQ. 16) $$PWM_{gain} = \frac{1}{\text{ramp slope}} = \frac{1}{38.1\text{mV}} = 26.2$$

Calculate current loop unity gain frequency

(EQ. 17) $$f_{tc} = PWM_{gain} \bullet g_{csa} \bullet R_{ifb} \bullet f_{cp}$$

This allows you to calculate the command voltage (+1V for ramp valley voltage) for the specific conditions.

(EQ. 18) $$V_{cmd} = R_{sns} \bullet I_{max} \bullet g_{csa} \bullet R_{ifb}$$

Determine the equivalent transconductance of the modulator (I_{OUT}/V_{cmd}).

(EQ. 19) $$GM = \frac{1}{R_{sns} \bullet g_{csa} \bullet R_{ifb}}$$

Calculate the unity gain frequency of the modulator.

(EQ. 20) $$f_{tm} = \frac{GM}{2\pi \bullet C_{OUT}}$$

Constrain the voltage loop f_t to be less than current loop f_{tc}.

(EQ. 21) $$\frac{f_t}{f_{tc}} = 0.5$$

This allows you to calculate compensation resistor R_{COMP}.

(EQ. 22) $$R_{COMP} = \frac{f_{tc} \bullet V_{OUT} \bullet 0.5}{f_{tm} \bullet g_{m,\,ea} \bullet V_{REF}}$$

Now calculate compensation capacitor C_{COMP}.

(EQ. 23) $$C_{COMP} = \frac{15}{2\pi \bullet R_{COMP} \bullet f_{tc}}$$

5.2 Boost Converter

5.2.1 Bootstrap Resistor Circuit

In an application board, it is common to have ringing noise when the LX and BOOT nodes swing with high dv/dt. This is a result of parasitic inductance and capacitance in the LX node and Boot capacitor routing on the printed circuit board and in the MOSFET structure. The generated noise can disrupt portions of the control circuit analog sense lines and may need some suppression. A simple method to reduce the noise involves placing a resistor of small value (from 4.7Ω to 10Ω) between the BOOT pin and the junction of the boot diode and boot capacitor. This slows down the high-side MOSFET turn-on to reduce the dv/dt as the LX node rises from near ground towards V_{IN}.

5.2.2 Boost Inductor Selection

While the boost converter is operating in stable Continuous Conduction Mode (CCM), the output voltage and the low-side transistor on-time is determined by Equation 24:

(EQ. 24) $$V_{OUT} = \frac{V_{IN}}{1 - \frac{t_{ON}}{T}} = \frac{V_{IN}}{1 - D}$$

where T is the switching cycle ($1/f_{SW}$) and $D = t_{ON}/T$ is the high-side on-duty of the transistor.

Under this CCM condition, the inductor ripple current can be defined as Equation 25:

(EQ. 25) $$I_{L,p\text{-}p} = D \bullet T \bullet \frac{V_{IN}}{L}$$

The previous equations can be rearranged to determine the inductor value as Equation 26:

(EQ. 26) $$L = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \bullet \left(\frac{V_{IN}}{I_{L,p\text{-}p} \bullet f_{SW}}\right)$$

In a DC/DC converter design, this ripple current is set around 20% to 50% of maximum DC output current. A reasonable starting point to adjust the inductor value is around 30% of the maximum DC output current. Increasing the inductor value reduces the ripple current and ripple voltage. However, the large inductance value can increase the converter size/volume while increasing the converter's response time to a load transient. Also, this reduces the ramp signal and may cause a noise sensitivity issue.

Under stable operation, the peak current flow in the inductor is the sum of maximum input current (full load and minimum V_{IN}) and 1/2 of ripple current.

(EQ. 27) $$I_{L,pk} = \frac{I_{L,p\text{-}p}}{2} + I_{IN}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current may be observed at the start-up, heavy load transient, and minimum input voltage. Therefore, the inductor's size needs to be determined with the consideration of these conditions. Also, to avoid exceeding the saturation rating of the inductor, Renesas recommends setting the OCP trip point between the maximum peak current and the inductor's saturation current rating.

Note: The OC1 signal is fixed at 80mV (160% of full load) and the OC2 hiccup threshold is fixed at 100mV; therefore, the inductor should have a saturation value exceeding 2x full load current.

5.2.3 Boost Output Capacitor

Output capacitors are required to filter the inductor current ripple and to provide energy storage to support transient load conditions, and a combination of electrolytic and ceramic capacitors is normally used. The ceramic capacitors filter the high-frequency spikes of the main switching devices and absorb the highest frequency components of the trapezoidal output current flowing through the output rectifier of a boost converter. In layout, place these output ceramic capacitors as close as possible to the main switching devices to maintain the smallest switching loop. To maintain capacitance over the biased voltage and temperature range, high-quality capacitors such as X7R or X5R are recommended. The electrolytic capacitors handle the load transient and output ripples.

The minimum output capacitor can be estimated by Equation 28:

(EQ. 28) $$C_{OUT,min} = \frac{100 \bullet I_{OUT} \bullet T_{ON}}{V_{OUT}}$$

The boost output ripple at the switching frequency is mainly determined by the trapezoidal rectifier current and output capacitance value. For the boost converter, the maximum output voltage ripple can be estimated using Equation 29, where $I_{OUT,max}$ is the load current at output, C is the total capacitance at output, and D_{MIN} is the minimum duty cycle at $V_{IN,max}$ and $V_{OUT,min}$.

(EQ. 29) $$V_{OUT,rip} = \frac{I_{OUT,max} \bullet (1 - D_{MIN})}{8C \bullet 2 \bullet f_{SW}}$$

5.2.4 Control Loop Compensation Components for the Boost Converter

- R_{SENSE} = 3mΩ
- Ramp amplitude = V_{ramp} = 0.8V
- Current sense amplifier transconductance = $G_{m,CSA}$ = 91.25µS
- Current feedback resistor value = R_{IFB} = 144kΩ
- Selected C_{OUT} = result calculated in Equation 28
- Reference voltage V_{REF} = 0.8V
- G_{mea} = 1.7 mS

Calculate the current loop pole frequency.

(EQ. 30) $$f_p = \frac{R_s}{2\pi L}$$

Calculate modulator gain.

(EQ. 31) $$A_m = \frac{V_{OUT}}{V_{RAMP}}$$

Determine the unity gain frequency of the current loop.

(EQ. 32) $$f_{tc} = A_m \bullet g_{m_csa} \bullet R_{ifb} \bullet f_p$$

Calculate the command signal that provides I_{OUT}.

(EQ. 33) $$V_{cmd} = I_{IN} \bullet R_s \bullet g_{m_csa} \bullet R_{ifb}$$

Determine the transconductance of the closed-loop current gain block.

(EQ. 34) $$GM = \frac{I_{OUT}}{V_{cmd}}$$

Incorporating selected output capacitance, calculate the unity gain frequency of the closed current loop.

(EQ. 35) $$f_{cc} = \frac{GM}{2\pi C_{OUT}}$$

Calculate the right half-plane zero frequency.

(EQ. 36) $$f_{rhpz} = \frac{V_{IN}^{2}}{2\pi LP_{OUT}}$$

Select a unity gain frequency less half of the right half-plane zero frequency.

(EQ. 37) $$f_t \leq 0.5 f_{rhpz}$$

Now calculate the compensation resistor.

(EQ. 38) $$R_{COMP} = \frac{f_{tc} V_{OUT}}{V_{REF} \bullet g_{m_csa} \bullet f_{cc}}$$

Calculate the unity gain frequency of the voltage loop.

(EQ. 39) $$f_t = \frac{V_{REF} \bullet g_{m_ea} \bullet R_{COMP} \bullet f_{cc}}{V_{OUT}}$$

The compensation capacitor can be calculated using Equation 40.

(EQ. 40) $$C_{COMP} = \frac{5}{2\pi R_{COMP} f_t}$$

5.3 Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL78263. Each channel of the switching buck converters requires specific attention to minimize the power loop area for highly efficient, stable operation. It is also important to consider routing the shared common areas between the two converters. Route the primary paths in a single layer copper if possible to reduce parasitic inductance in the power current paths.

The following layout instructions see Figures 29 and 30 as noted.

1. In Figure 29, connect the common connection between input capacitors, output capacitors, and the low-side FET for each buck converter through the central ground (gray) area.
2. When the high-side MOSFET is switched ON and OFF the power current alternates flowing through the input capacitor and high-side MOSFET, or the low-side MOSFET. Minimize the loop area between CIN, high-side MOSFET, and low-side MOSFET to reduce interference from the high di/dt intervals as the current alternates between the MOSFETs.
3. The first inner layer below the top copper layer with power components should be a ground layer that is as complete as possible, as indicated in Figure 30 using the light green fill. This provides a tightly coupled ground return path for the power circuitry. This layer is also used in conjunction with many vias to create a low-impedance connection from the common power GND region to the ISL78264 controller, and the thermal pad is connected to this plane using multiple vias.
4. Connect the signal ground (Pin 11) to the thermal pad ground directly under the IC. For best noise immunity, signal pins such as COMP, RT, and configuration resistors can be connected in a small SGND pour that connects to Pin 11, which connects to PGND in a single point connection under the IC.
5. Each converter has ISNS connections that should be routed as shown in Figure 30. The ISNS traces are routed on the second inner layer, which is shielded from power switching currents by the ground area on the inner layer 1. Begin the ISNS traces as a kelvin connection through a via in the center of the sense resistor in each converter.
6. Minimize the trace lengths on the feedback loop and route around switching power circuits to minimize noise pick-up.
7. Place the capacitors on VIN (Pin 26) and VCC (Pin 19) close to respective pins and ground connection.

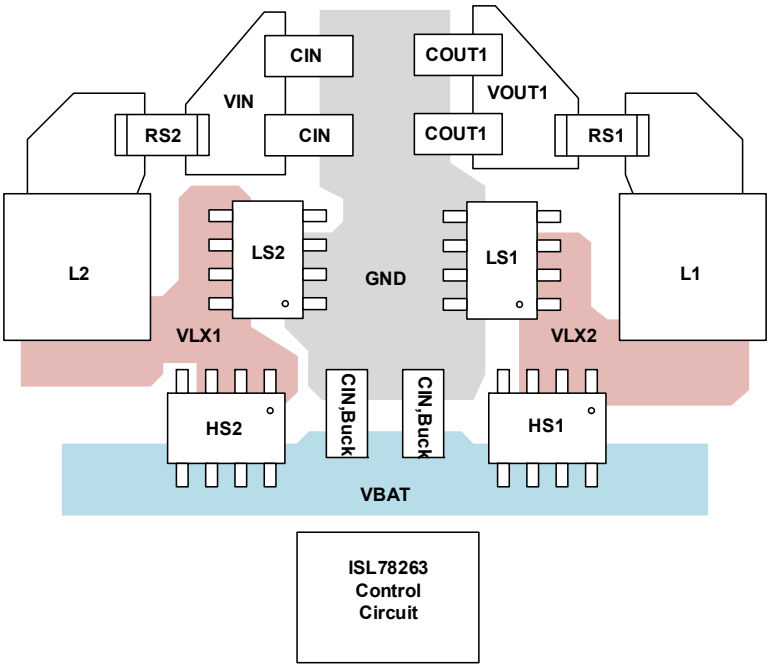


Figure 29. PCB Layout Illustrating Power Component Placement

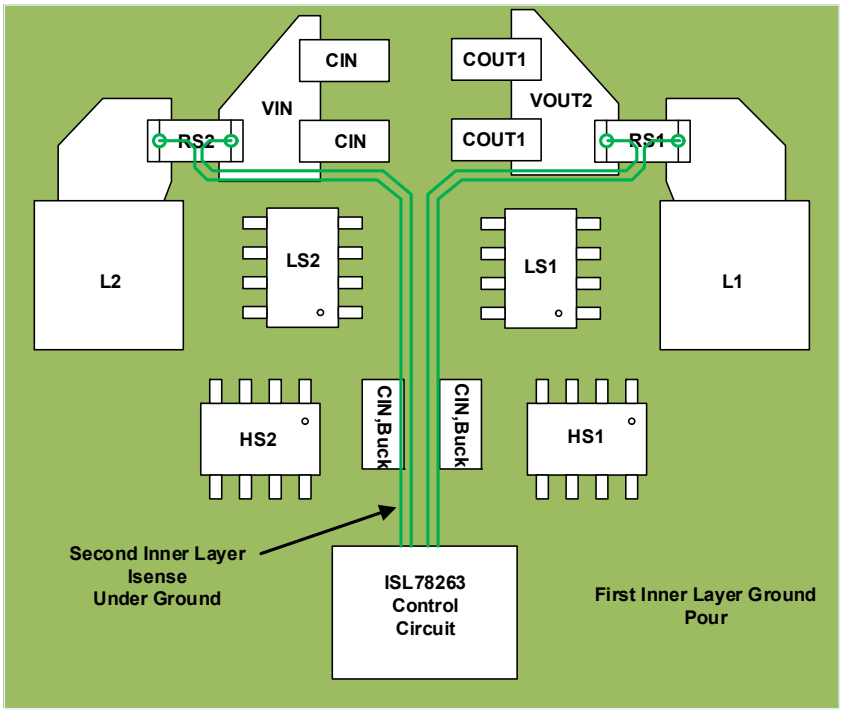


Figure 30. PCB Layout Illustrating Current Sense Routing

6. Revision History

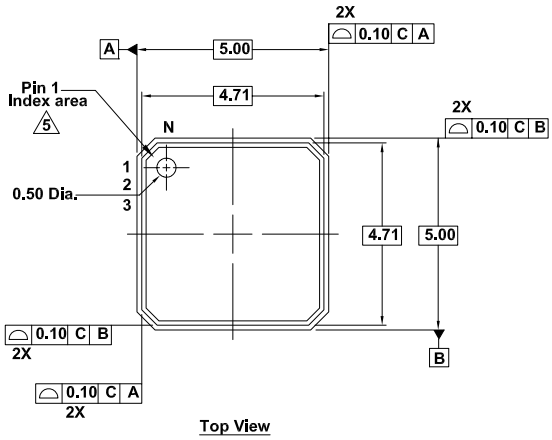
Rev.	Date	Description
2.00	Oct 22, 2021	Removed Related Literature section. Updated Ordering Information table format. Updated termination finish and tape and reel qty to reflect the correct information. Updated POD L32.5X5H to the latest revision, changes are as follows: -Added Note 7 for Edge Protection Technology -Updated D1 and E1 dimensions in Top View changing them from 4.75 to 4.71. -Updated side view by adding Edge protection information.
1.02	Mar 26, 2021	Updated Figure 1 and Figure 3.
1.01	Jan 12, 2021	Added part ISL78263ARZ-T7A.
1.00	Jul 24, 2020	Initial release

7. Package Outline Drawing

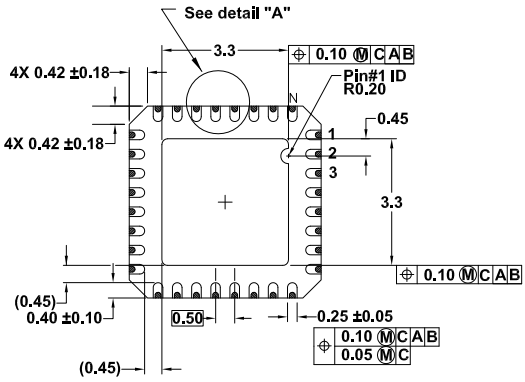
For the most recent package outline drawing, see L32.5x5H.

L32.5x5H

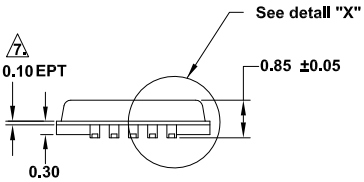
32 Lead Quad Flat No-Lead Plastic Package (Punch QFN with Wetable Flank)
Rev 3, 8/2021



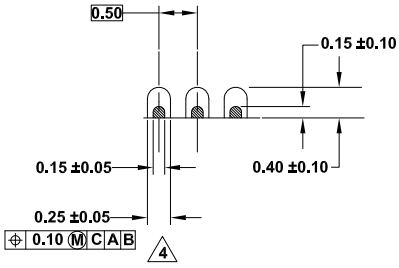
Top View



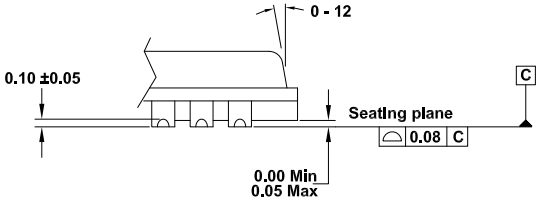
Bottom View



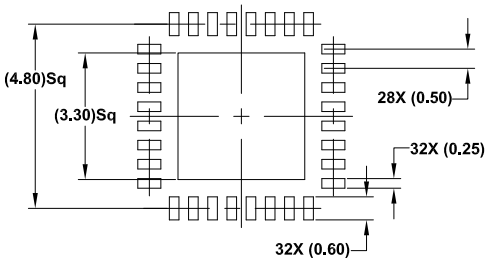
Side View



Detail "A"



Detail "X"



Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME 14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05
4. Dimension applies to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Reference document: JEDEC MO220
7. Edge Protection Technology

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   “Standard”:Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   “High Quality”:Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

    (Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

    (Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev. 4.0-2 April 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.