The ISL78233 and ISL78234 are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver 3A (ISL78233), or 4A (ISL78234) of continuous output current from a 2.7V to 5.5V input supply. The devices use current mode control architecture to deliver a very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL78233 and ISL78234 integrate a very low ON-resistance P-channel (35mΩ) high-side FET and N-channel (11mΩ) low-side FET to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 200mV dropout voltage at 4A output current. The operation frequency of the Pulse-Width Modulator (PWM) is adjustable from 500kHz to 4MHz. The default switching frequency of 2MHz is set by connecting the FS pin high.

The ISL78233 and ISL78234 can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference, while discontinuous mode provides higher efficiency by reducing switching losses at light loads.

Fault protection is provided by internal Hiccup mode current limiting during short-circuit and overcurrent conditions. Other protection, such as overvoltage and over-temperature are also integrated into the device. A power-good output voltage monitor indicates when the output is in regulation.

The ISL78233 and ISL78234 offer a 1ms Power-Good (PG) timer at power-up. When in shutdown, the ISL78233 and ISL78234 discharge the output capacitor through an internal soft-stop switch. Other features include internal fixed or adjustable soft-start and internal/external compensation.

The ISL78233 and ISL78234 are available in a 3mmx3mm 16 Ld Thin Quad Flat (TQFN) Pb-free package and in a 5mmx5mm 16 Ld Wettable Flank Quad Flat No-Lead (WFQFN) package with an exposed pad for improved thermal performance. The ISL78233 and ISL78234 are rated to operate across the temperature range of -40 °C to +125 °C.

**Features**

- 2.7V to 5.5V input voltage range
- Very low ON-resistance FETs - P-channel 35mΩ and N-channel 11mΩ typical values
- High efficiency synchronous buck regulator with up to 95% efficiency
- ±1.2%/±1% reference accuracy over temperature/load/line
- Complete BOM with as few as 3 external parts
- Internal soft-start - 1ms or adjustable
- Soft-stop output discharge during disable
- Adjustable frequency from 500kHz to 4MHz - default at 2MHz
- External synchronization up to 4MHz
- Over-temperature, overcurrent, overvoltage, and negative overcurrent protection
- Shared common device pinout allows simplified output power upgrades over time
- Tiny 3mmx3mm TQFN package
- **AEC-Q100** qualified

**Applications**

- DC/DC POL modules
- μC/μP, FPGA, and DSP power
- Video processor/SOC power
- Li-ion battery powered devices
- Automotive infotainment power

**FIGURE 1. EFFICIENCY vs LOAD (2MHz 5V<sub>IN</sub> PFM, T<sub>A</sub> = +25 °C)**
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Typical Application Diagrams

**Figure 2. Typical Application Diagrams**

**Typical Application Circuit**

**Typical Application Circuit: EN connects to Vin**

*\( C_3 \) is optional. Renesas recommends having a placeholder for it and check loop analysis before use.

Using external compensation is always recommended for loop design flexibility.

Connect COMP pin to VIN to use internal compensation (without using \( R_4/\text{CA/C5} \)) is optional, as the dot line shows.

If internal compensation is used, EN should be held below the EN\(_{\text{VIL}}\) until VIN exceeds its \( \text{VUVLO} \) rising during every time startup.

*When EN is connected to VIN directly, it needs to use external compensation.*

**Table 1. Typical Application Diagrams**

<table>
<thead>
<tr>
<th>( V_{\text{OUT}} )</th>
<th>1.2V</th>
<th>1.5V</th>
<th>1.8V</th>
<th>2.5V</th>
<th>3.3V</th>
<th>3.6V</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_1 )</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
<td>2 x 22μF</td>
</tr>
<tr>
<td>( C_3 )</td>
<td>22pF</td>
<td>22pF</td>
<td>22pF</td>
<td>22pF</td>
<td>22pF</td>
<td>22pF</td>
</tr>
<tr>
<td>( L_1 )</td>
<td>0.33-0.68μH</td>
<td>0.33-0.68μH</td>
<td>0.47-0.78μH</td>
<td>0.47-0.78μH</td>
<td>0.47-0.78μH</td>
<td>0.47-0.78μH</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>100kΩ</td>
<td>150kΩ</td>
<td>200kΩ</td>
<td>316kΩ</td>
<td>450kΩ</td>
<td>500kΩ</td>
</tr>
<tr>
<td>( R_3 )</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
</tr>
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</table>
FIGURE 3. FUNCTIONAL BLOCK DIAGRAM
## Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER (Note 4)</th>
<th>PART MARKING</th>
<th>OUTPUT VOLTAGE (V)</th>
<th>PACKAGE DESCRIPTION (RoHS Compliant)</th>
<th>PKG. DWG. #</th>
<th>CARRIER TYPE (Note 1)</th>
<th>TEMP. RANGE</th>
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</thead>
<tbody>
<tr>
<td>ISL78233ARZ (Note 2)</td>
<td>8233</td>
<td>Adjustable</td>
<td>16 Ld 3x3 TQFN</td>
<td>L16.3x3D</td>
<td>Tube</td>
<td>-40 to +125°C</td>
</tr>
<tr>
<td>ISL78233ARZ-T (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reel, 6k</td>
<td></td>
</tr>
<tr>
<td>ISL78233ARZ-T7A (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reel, 250</td>
<td></td>
</tr>
<tr>
<td>ISL78233AARZ (Note 3)</td>
<td>78233ARZ</td>
<td></td>
<td>16 Ld 5x5mm WFQFN</td>
<td>L16.5x5D</td>
<td>Tube</td>
<td></td>
</tr>
<tr>
<td>ISL78233AARZ-T (Note 3)</td>
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<td></td>
<td></td>
<td></td>
<td>Reel, 6k</td>
<td></td>
</tr>
<tr>
<td>ISL78233AARZ-T7A (Note 3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reel, 250</td>
<td></td>
</tr>
<tr>
<td>ISL78233BARZ (Note 2)</td>
<td>8233</td>
<td></td>
<td>16 Ld 3x3 TQFN</td>
<td>L16.3x3D</td>
<td>Tube</td>
<td></td>
</tr>
<tr>
<td>ISL78233BARZ-T (Note 2)</td>
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<td></td>
<td></td>
<td></td>
<td>Reel, 6k</td>
<td></td>
</tr>
<tr>
<td>ISL78233BARZ-T7A (Note 2)</td>
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<td></td>
<td></td>
<td>Reel, 250</td>
<td></td>
</tr>
<tr>
<td>ISL78234ARZ (Note 2)</td>
<td>8234</td>
<td></td>
<td>16 Ld 3x3 TQFN</td>
<td>L16.3x3D</td>
<td>Tube</td>
<td></td>
</tr>
<tr>
<td>ISL78234ARZ-T (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reel, 6k</td>
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</tr>
<tr>
<td>ISL78234ARZ-T7A (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reel, 250</td>
<td></td>
</tr>
<tr>
<td>ISL78234AARZ (Note 3)</td>
<td>78234AARZ</td>
<td></td>
<td>16 Ld 5x5mm WFQFN</td>
<td>L16.5x5D</td>
<td>Tube</td>
<td></td>
</tr>
<tr>
<td>ISL78234AARZ-T (Note 3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reel, 6k</td>
<td></td>
</tr>
<tr>
<td>ISL78234AARZ-T7A (Note 3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reel, 250</td>
<td></td>
</tr>
<tr>
<td>ISL78233EVAL1Z</td>
<td>3x3mm TQFN</td>
<td></td>
<td>Evaluation Board</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL78234EVAL1Z</td>
<td>3x3mm TQFN</td>
<td></td>
<td>Evaluation Board</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>ISL78233EVAL2Z</td>
<td>5x5mm WFQFN</td>
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<td>Evaluation Board</td>
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<tr>
<td>ISL78234EVAL2Z</td>
<td>5x5mm WFQFN</td>
<td></td>
<td>Evaluation Board</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL78233, ISL78234 device information pages. For more information about MSL, see TB363.

### TABLE 2. KEY DIFFERENCE BETWEEN FAMILY OF PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>I&lt;sub&gt;OUT MAX (A)&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISL78233</td>
<td>3</td>
</tr>
<tr>
<td>ISL78234</td>
<td>4</td>
</tr>
<tr>
<td>ISL78235</td>
<td>5</td>
</tr>
</tbody>
</table>
**Pin Configuration**

**Pin Descriptions**

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 16</td>
<td>VIN</td>
<td>Input supply voltage. Place a minimum of two 22µF ceramic capacitors from VIN to PGND as close as possible to the IC for decoupling.</td>
</tr>
<tr>
<td>2</td>
<td>VDD</td>
<td>Input supply voltage for logic. Connect to the VIN pin.</td>
</tr>
<tr>
<td>3</td>
<td>PG</td>
<td>Power-good is an open-drain output. Use a 10kΩ to 100kΩ pull-up resistor connected between VIN and PG. At power-up or EN HI, PG rising edge is delayed by 1ms upon output reached within regulation.</td>
</tr>
<tr>
<td>4</td>
<td>SYNC</td>
<td>Mode Selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with the positive edge trigger. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case of SYNC pin float.</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge output capacitor when driven to low.</td>
</tr>
<tr>
<td>6</td>
<td>FS</td>
<td>This pin sets the oscillator switching frequency, using a resistor, RFS, from the FS pin to GND. The frequency of operation may be programmed between 500kHz to 4MHz. The default frequency is 2MHz if FS is connected to VIN.</td>
</tr>
<tr>
<td>7</td>
<td>SS</td>
<td>SS is used to adjust the soft-start time. Set to SGND for internal 1ms rise time. Connect a capacitor from SS to SGND to adjust the soft-start time. Do not use more than 33nF per IC.</td>
</tr>
<tr>
<td>8</td>
<td>COMP</td>
<td>The feedback network of the regulator, FB, is the negative input to the transconductance error amplifier. COMP is the output of the amplifier if COMP is not tied to VDD. Otherwise, COMP is disconnected through a MOSFET for internal compensation. Must connect COMP to VDD in internal compensation mode. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. There is an internal compensation to meet a typical application. Additional external networks across COMP and SGND might be required to improve the loop compensation of the amplifier operation. In addition, the regulator power-good and undervoltage protection circuitry use FB to monitor the regulator output voltage.</td>
</tr>
<tr>
<td>9</td>
<td>FB</td>
<td>The exposed pad must be connected to the SGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the SGND plane for optimal thermal performance.</td>
</tr>
<tr>
<td>10</td>
<td>SGND</td>
<td>Signal ground</td>
</tr>
<tr>
<td>11, 12</td>
<td>PGND</td>
<td>Power ground</td>
</tr>
<tr>
<td>13, 14, 15</td>
<td>PHASE</td>
<td>Switching node connections. Connect to one terminal of the inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See &quot;Functional Block Diagram&quot; on page 4 for more detail.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings (Reference to GND)

VIN .......................... -0.3V to 5.8V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB .......................... -0.3V to VIN + 0.3V
PHASE
DC .......................... -0.3V to 6.5V
Pulsed (Note 8) .......................... -2V (< 0.6µJ) to 7V (20ms)
COMP, SS (Note 7) .......................... -0.3V to 2.7V

ESD Rating
Human Body Model (Tested per AEC-Q100-002) .... 5kV
Machine Model (Tested per AEC-Q100-003) .... 300V
Charge Device Model (Tested per AEC-Q100-011) .... 2kV
Latch-Up (Tested per AEC-Q100-004, Class II, Level A) .... 100mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:
5. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
6. $\theta_{JC}$, case temperature location is at the center of the exposed metal pad on the package underside.
7. COMP is an input and output pin. When the ISL7823x is used with an internal compensation, the COMP pin has a rating similar to VIN. When using the ISL7823x in an external compensation, the ratings are -0.3V to 2.7V.
8. The PHASE pin negative voltage can be less than -2V as long as the energy of the pulse does not exceed 0.6µJ.

Thermal Information

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 9)</th>
<th>TYP</th>
<th>MAX (Note 9)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance</td>
<td>$\theta_{JA}$ ($^\circ$C/W)</td>
<td>16 Ld TQFN Package (Notes 5, 6)</td>
<td>43</td>
<td>3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\theta_{JC}$ ($^\circ$C/W)</td>
<td>16 Ld WQFN Package (Notes 5, 6)</td>
<td>33</td>
<td>3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Pb-Free Reflow Profile</td>
<td>see TB493</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

V_IN Supply Voltage Range .......................... 2.7V to 5.5V
Load Current Range
(ISL78233) ............................................. 0A to 3A
(ISL78234) ............................................. 0A to 4A
Ambient Temperature Range .......................... -40°C to +125°C

Electrical Specifications

Unless otherwise noted, all parameter limits are established across the recommended operating conditions and the specification limits are measured at the following conditions: $T_A = -40°C$ to $+125°C$, $V_IN = 3.6V$, $EN = V_IN$, unless otherwise noted. Typical values are at $T_A = +25°C$. Boldface limits apply across the operating temperature range, -40°C to +125°C.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 9)</th>
<th>TYP</th>
<th>MAX (Note 9)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN Undervoltage Lockout Threshold</td>
<td>$V_{UVLO}$</td>
<td>Rising, no load</td>
<td>2.5</td>
<td>2.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling, no load</td>
<td>2.2</td>
<td>2.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Quiescent Supply Current</td>
<td>$I_{VIN}$</td>
<td>SYNC = GND, no load at the output</td>
<td>45</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC = GND, no load at the output and no switches switching</td>
<td>45</td>
<td>60</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC = $V_{IN}$, FS = 2MHz, no load at the output</td>
<td>19</td>
<td>25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>$I_{SD}$</td>
<td>SYNC = GND, $V_{IN}$ = 5.5V, EN = low</td>
<td>3.8</td>
<td>10</td>
<td>µA</td>
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OUTPUT REGULATION

<table>
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<th>SYMBOL</th>
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<th>TYP</th>
<th>MAX (Note 9)</th>
<th>UNIT</th>
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</thead>
<tbody>
<tr>
<td>Reference Voltage</td>
<td>$V_{REF}$</td>
<td></td>
<td>0.593</td>
<td>0.600</td>
<td>0.606</td>
<td>V</td>
</tr>
<tr>
<td>VFB Bias Current</td>
<td>$I_{VFB}$</td>
<td>VFB = 0.75V</td>
<td>0.1</td>
<td>µA</td>
<td></td>
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<tr>
<td>Line Regulation</td>
<td>$V_{IN} = V_O + 0.5V$ to 5.5V (minimal 2.7V)</td>
<td>0.2</td>
<td>%/V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft-Start Ramp Time Cycle</td>
<td>$I_{SS}$</td>
<td>$V_{SS} = 0.1V$</td>
<td>1.7</td>
<td>2.1</td>
<td>2.5</td>
<td>µA</td>
</tr>
<tr>
<td>Soft-Start Charging Current</td>
<td>$I_{SS}$</td>
<td>$V_{SS} = 0.1V$</td>
<td>1</td>
<td>ms</td>
<td></td>
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</table>

OVERCURRENT PROTECTION

<table>
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<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 9)</th>
<th>TYP</th>
<th>MAX (Note 9)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Limit Blanking Time</td>
<td>$I_{OCON}$</td>
<td></td>
<td>17</td>
<td></td>
<td>Clock pulses</td>
<td></td>
</tr>
<tr>
<td>Overcurrent and Auto Restart Period</td>
<td>$I_{OCOFF}$</td>
<td></td>
<td>8</td>
<td>SS cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Peak Current Limit</td>
<td>$I_{PLIMIT}$</td>
<td>ISL78234, $T_A = +25°C$</td>
<td>5.4</td>
<td>6.7</td>
<td>8.1</td>
<td>A</td>
</tr>
<tr>
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<td>3.7</td>
<td>6.6</td>
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### Electrical Specifications

Unless otherwise noted, all parameter limits are established across the recommended operating conditions and the specification limits are measured at the following conditions: $T_A = -40^\circ C$ to $+125^\circ C$, $V_{IN} = 3.6V$, $EN = V_{IN}$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** (Continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 9)</th>
<th>TYP</th>
<th>MAX (Note 9)</th>
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<td>1.2</td>
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<td>Negative Current Limit</td>
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<td>-1.3</td>
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<td></td>
<td>-6.0</td>
<td>-0.6</td>
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</table>

### COMPENSATION

| Error Amplifier Transconductance | COMP = $V_{DD}$, internal compensation | 125 | µA/V |
| Transresistance | External compensation | 130 | µA/V |

### PHASE

**P-Channel MOSFET ON-Resistance**
- $V_{IN} = 5V$, $I_O = 200mA$: $26$ mΩ
- $V_{IN} = 2.7V$, $I_O = 200mA$: $38$ mΩ
**N-Channel MOSFET ON-Resistance**
- $V_{IN} = 5V$, $I_O = 200mA$: $5$ mΩ
- $V_{IN} = 2.7V$, $I_O = 200mA$: $8$ mΩ

**PHASE Maximum Duty Cycle**: 100 %

**PHASE Minimum On-Time**: SYNC = High, 100 ns

### OSCILLATOR

**Nominal Switching Frequency**
- $f_{SW} = V_{IN}$
- $f_{SW}$ with $RS = 402k\Omega$: $420$ kHz
- $f_{SW}$ with $RS = 42.2k\Omega$: $4200$ kHz

**SYNC Logic LOW to HIGH Transition Range**: 0.67 V, 0.75 V, 0.84 V

**SYNC Hysteresis**: 0.17 V

**SYNC Logic Input Leakage Current**
- $V_{IN} = 3.6V$: 3.7 µA
- 5 µA

### PG

**Output Low Voltage**
- IPG = 1mA: 0.3 V

**Delay Time (Rising Edge)**
- Time from $V_{OUT}$ reached regulation: 0.5 ms, 1 ms

**PG Pin Leakage Current**
- $PG = V_{IN}$: 0.01 µA, 0.1 µA

**OVP PG Rising Threshold**: 0.80 V

**UVP PG Rising Threshold**: 80 %

**UVP PG Hysteresis**: 5.5 %

**PGOOD Delay Time (Falling Edge)**: 6.5 µs

### EN

**Logic Input Low (Note 10)**
- $EN_{VIL}$: 0.4 V

**Logic Input High**
- $EN_{VIH}$: 0.9 V

**EN Logic Input Leakage Current**
- Pulled up to 3.6V: 0.1 µA, 1 µA

**Thermal Shutdown**
- Temperature Rising: 150 °C

**Thermal Shutdown Hysteresis**
- Temperature Falling: 25 °C

**NOTE:**

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

10. EN should be held below the EN_VIL until $V_{IN}$ exceeds $V_{UVLO}$ rising.
Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = 25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$.

**FIGURE 4. EFFICIENCY vs LOAD (2MHz, 3.3V$_{IN}$ PWM)**

**FIGURE 5. EFFICIENCY vs LOAD (2MHz, 3.3V$_{IN}$ PFM)**

**FIGURE 6. EFFICIENCY vs LOAD (2MHz, 5V$_{IN}$ PWM)**

**FIGURE 7. EFFICIENCY vs LOAD (2MHz, 5V$_{IN}$ PFM)**

**FIGURE 8. $V_{OUT}$ REGULATION vs LOAD (1MHz, $V_{OUT} = 1.2V$)**

**FIGURE 9. $V_{OUT}$ REGULATION vs LOAD (1MHz, $V_{OUT} = 1.5V$)**
Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$.

SYNCC = $V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $4A$. (Continued)
**Typical Operating Performance**  Unless otherwise noted, operating conditions are: $T_A = +25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$.

SYNC = $V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $4A$. (Continued)
Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$.

SYNC = $V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $4A$. (Continued)
Typical Operating Performance  Unless otherwise noted, operating conditions are: \( T_A = +25^\circ C, V_{IN} = 5V, EN = V_{IN} \) .
SYNC = \( V_{IN} \), L = \( 1.0\mu H \), \( C_1 = 22\mu F, C_2 = 2 \times 22\mu F \), \( I_{OUT} = 0A \) to \( 4A \). (Continued)
Theory of Operation

The ISL78233 and ISL78234 are step-down switching regulators optimized for automotive battery powered applications. The regulator operates at a 2MHz default switching frequency for high efficiency and allow smaller form factor, when FS is connected to VIN. By connecting a resistor from FS to SGND, the operational frequency adjustable range is 500kHz to 4MHz. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 45µA. The supply current is typically only 3.8µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNC pin HI (>0.8V) forces the converter into PWM mode, regardless of output current. The ISL78233 and ISL78234 employ the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 3 on page 4 shows the functional block diagram. The current loop consists of the oscillator, the PWM comparator, current-sensing circuit, and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes proportionally with frequency. The gain for the current-sensing circuit is typically 200mV/A. The control reference for the current loops comes from the Error Amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the PFET and turn on the N-channel MOSFET. The NFET stays on until the end of the PWM cycle. Figure 33 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

The output voltage is regulated by controlling the VEAMP voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and is discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 55pF and 100kΩ RC network. The maximum EAMP voltage output is precisely clamped to 2.5V.

Skip Mode

Pulling the SYNC pin LO (<0.4V) forces the converter into PFM mode. The ISL78233 and ISL78234 enter a Pulse-Skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 34 on page 15 illustrates Skip mode operation. A zero-cross sensing circuit shown in Figure 3 on page 4 monitors the NFET current for zero crossing. When 16 consecutive cycles are detected, the regulator enters Skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

When Skip mode is entered, the pulse modulation starts being controlled by the Skip comparator shown in Figure 3 on page 4. Each pulse cycle is still synchronized by the PWM clock. The PFET is turned on at the clock's rising edge and turned off when the output is higher than 1.2% of the nominal regulation or when its current reaches the peak Skip current limit value. Then, the inductor current is discharging to 0A and stays at zero (the internal clock is disabled), and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the PFET is turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.2% below the nominal voltage.
**Frequency Adjust**

The frequency of operation is fixed at 2MHz when FS is tied to VIN. Adjustable frequency ranges from 500kHz to 4MHz using a simple resistor connecting FS to SGND according to Equation 1:

\[ R_{FS} [\Omega] = \frac{220 \cdot 10^3}{f_{OSC} [kHz]} - 14 \]  

(EQ. 1)

The ISL78233 and ISL78234 have frequency synchronization capability by simply connecting the SYNC pin to an external square pulse waveform. The frequency synchronization feature synchronizes the positive edge trigger and its switching frequency up to 4MHz. The minimum external SYNC frequency is half of the free running frequency (either the default frequency or determined by the FS resistor).

**Overcurrent Protection**

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 3 on page 4. The current sensing circuit has a gain of 200mV/A, from the P-FET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripped to turn off the PFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

If an overcurrent condition is detected, the upper MOSFET is immediately turned off and does not turn on again until the next switching cycle. When the initial overcurrent condition is detected, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter is incremented. If there are 17 sequential OC fault detections, the regulator is shut down under an overcurrent fault condition. An overcurrent fault condition results in the regulator attempting to restart in a Hiccup mode within the delay of eight soft-start periods. At the end of the eighth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of eight soft-start periods, the output resumes back into regulation point after Hiccup mode expires.

**Negative Current Protection**

Similar to overcurrent, the negative current protection is realized by monitoring the current across the low-side NFET, as shown in Figure 3 on page 4. When the valley point of the inductor current reaches -3A for four consecutive cycles, both PFET and NFET are off. The 100Ω in parallel to the NFET activates discharging the output into regulation. The control begins to switch when output is within regulation. The regulator is in PFM for 20µs before switching to PWM if necessary.

**PG**

PG is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After a 1ms soft-start period delay, PG becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 15% below or raises 0.8V above the nominal regulation voltage, the ISL78233 and ISL78234 pull PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor, R1, between PG and VIN. A 100kΩ resistor works well in most applications.

**UVLO**

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.

**Soft Start-Up**

The soft start-up reduces the inrush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current and the output voltage speed, so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in Skip mode to support prebiased output condition.

Tie SS to SGND for internal soft-start is approximately 1ms. Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 2.1μA current source...
sets the soft-start interval of the converter, \( t_{SS} \) as shown by Equation 2.

\[
C_{SS} \[\mu F\] = 3.1 \cdot t_{SS}[\mu s] \quad \text{(EQ. 2)}
\]


**Enable**

The Enable (EN) input allows you to control the turning on or off of the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600\( \mu \)s delay for waking up the bandgap reference and then the soft start-up begins.

To use internal compensation (COMP pin connects to VIN), EN should be held below the EN\_VIL until VIN exceeds V\_UVLO rising during every start up. If EN is connected to VIN directly, it needs to use external compensation.

**Discharge Mode (Soft-Stop)**

When a transition to shutdown mode occurs or the \( V_{IN} \) UVLO is set, the outputs discharge to GND through an internal 100\( \Omega \) switch.

**Power MOSFETs**

The power MOSFETs are optimized for best efficiency. The ON-resistance for the PFET is typically 35m\( \Omega \) and the ON-resistance for the NFET is typically 11m\( \Omega \).

**100% Duty Cycle**

The ISL78233 and ISL78234 feature 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL78233 and ISL78234 can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the PFET.

**Thermal Shutdown**

The ISL78233 and ISL78234 have built-in thermal protection. When the internal temperature reaches +150\(^\circ\)C, the regulator is completely shut down. As the temperature drops to +125\(^\circ\)C, the ISL78233 and ISL78234 resume operation by stepping through the soft-start.

**Applications Information**

**Output Inductor and Capacitor Selection**

To consider steady state and transient operations, the ISL78233 and ISL78234 typically use a 1.0\( \mu \)H output inductor. The higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. Renesas recommends setting the ripple inductor current to approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 3:

\[
\Delta I = \frac{V_{O} \cdot (1 - V_{O}/V_{IN})}{L \cdot f_S} \quad \text{(EQ. 3)}
\]

The inductor’s saturation current rating needs to be at least larger than the peak current. The ISL78233 and ISL78234 protect the typical peak current 4.9A/6.7A. The saturation current needs to be over 7A for maximum output current application.

The ISL78233 and ISL78234 use an internal compensation network and the output capacitor value is dependent on the output voltage. The recommended ceramic capacitor is X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 1 on page 3.

In Table 1, the minimum output capacitor value is given for the different output voltages to make sure that the whole converter system is stable. Additional output capacitance should be added for better performance in applications where high load transient or low output ripple is required. Renesas recommends checking the system level performance along with the simulation model.

**Output Voltage Selection**

The output voltage of the regulator can be programmed using an external resistor divider that scales the output voltage relative to the internal reference voltage, and feeds it back to the inverting input of the error amplifier (see Figure 2 on page 3).

The output voltage programming resistor, \( R_2 \), depends on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor, \( R_3 \), is typically between 10k\( \Omega \) and 100k\( \Omega \), as shown in Equation 4.

\[
R_2 = \frac{R_3}{\frac{V_{O}}{V_{FB}} - 1} \quad \text{(EQ. 4)}
\]

If the output voltage desired is 0.6V, then \( R_3 \) is left unpopulated and \( R_2 \) is shorted. There is a leakage current from VIN to PHASE. Renesas recommends preloading the output with 10\( \mu \)A minimum. For better performance, add 15pF in parallel with \( R_2 \) (200k\( \Omega \)). Check loop analysis before use in application.

**Input Capacitor Selection**

The main functions for the input capacitor are providing decoupling of the parasitic inductance and a filtering function to prevent the switching current flowing back to the battery rail. At least two 22\( \mu \)F X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

**Loop Compensation Design**

When COMP is not connected to VDD, the COMP pin is active for external loop compensation. The ISL78233 and ISL78234 use constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current-sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable because its peak current is constant, and the system becomes a single order
system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 35 on page 17 shows the small signal model of the synchronous buck regulator.

![Small Signal Model of Synchronous Buck Regulator](image)

**FIGURE 35. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR**

Compensator design goal:
- High DC gain
- Choose loop bandwidth \( f_c \) less than 100kHz
- Gain margin: >10dB
- Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of \( f_c \) has a unity gain. Therefore, the compensator resistance \( R_6 \) is determined by **Equation 6**:

\[
R_6 = \frac{2\pi f_c V_o C_o}{\text{GM} \cdot V_{FB}} = 17.45 \times 10^3 \cdot f_c V_o C_o
\]  (EQ. 6)

where GM is the sum of the transconductance, \( g_{m} \), of the voltage error amplifier in each phase. Compensator capacitor \( C_6 \) is then given by **Equation 7**.

\[
C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6} C_7 = \max (\frac{R_o C_o}{R_6} \cdot \frac{1}{\pi f_c R_6})
\]  (EQ. 7)

Place one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in **Equation 7**. An optional zero can boost the phase margin. \( \Omega_{cz2} \) is a zero due to \( R_2 \) and \( C_3 \).

Place compensator zero 2 to 5 times \( f_c \):

\[
C_3 = \frac{1}{\pi f_c R_2}
\]  (EQ. 8)

Example: \( V_{IN} = 5V, V_o = 1.8V, I_o = 4A, FS = 1MHz, R_2 = 200k\Omega, R_3 = 100k\Omega, C_2 = 2\times22\mu F/3m\Omega, L = 1\mu H, f_c = 100kHz \), then compensator resistance \( R_6 \):

\[
R_6 = 17.45 \times 10^3 \cdot 100kHz \cdot 1.8V \cdot 44\mu F = 138k\Omega
\]  (EQ. 9)

It is acceptable to use 137k\Ω\ as the closest standard value for \( R_6 \):

\[
C_6 = \frac{1.8V \cdot 44\mu F}{4A \cdot 137k\Omega} = 144\mu F
\]  (EQ. 10)

\[
C_7 = \max (\frac{3m\Omega \cdot 44\mu F}{137k\Omega} \cdot \frac{1}{\pi \cdot 1MHz(137k\Omega)}) = (1pF, 2.3pF)
\]  (EQ. 11)

It is also acceptable to use the closest standard values for \( C_6 \) and \( C_7 \). There is approximately 3pF parasitic capacitance from \( V_{COMP} \) to GND; Therefore, \( C_7 \) is optional. Use \( C_6 = 150pF \) and \( C_7 = \text{OPEN} \).

\[
C_3 = \frac{1}{\pi 100kHz \cdot 200k\Omega} = 16pF
\]  (EQ. 12)

Use \( C_3 = 15pF \). Note that \( C_3 \) may increase the loop bandwidth from previous estimated value. **Figure 37 on page 18** shows the simulated voltage loop gain. It is shown that it has a 150kHz loop bandwidth with a 42° phase margin and 10dB gain margin. It may be more desirable to achieve an increased phase margin. This can be accomplished by lowering \( R_6 \) by 20% to 30%.
PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For the ISL78233 and ISL78234, the power loop is composed of the output inductor L’s, the output capacitor Cₒ, the PHASE pins, and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short, and wide. The switching node of the converter, the PHASE pins and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. Place the input capacitor as close as possible to the VIN pin. Connect the ground of the input and output capacitors as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. See TB389 for via placement on the copper area of the PCB underneath the thermal pad for optimum thermal performance.

FIGURE 37. SIMULATED LOOP GAIN
# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>CHANGE</th>
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<tr>
<td>Jun 16, 2022</td>
<td>11.01</td>
<td>Updated Figure 2. Updated the Enable section to explain the internal and external compensation selection.</td>
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<tr>
<td>Jan 20, 2022</td>
<td>11.00</td>
<td>Removed Related Literature section. Updated the Ordering Information table formatting. Updated POD L16.5x5D to the latest revision, changes are as follows: -Added Edge protection Technology -Change dimension top view inner dimension 4.75 to 4.71mm -Bottom View: For C_C, moved the horizontal line to the top of the dimple.</td>
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<tr>
<td>Jan 12, 2021</td>
<td>10.00</td>
<td>Added ISL78233BARZ, ISL78233BARZ-T, and ISL78233BARZ-T7A to Ordering Information.</td>
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<tr>
<td>Apr 19, 2018</td>
<td>8.00</td>
<td>Updated Related Literature section. Updated Ordering Information table by adding tape and reel information, Note 3, and updating Note 1. Adding Note 8 and its cross-referencing on page 7. Added symbol name &quot;EN_VIL&quot; to the Logic Input Low parameter and the symbol name &quot;EN_VIH&quot; to the Logic Input High parameter on page 7. Updated Enable section on page 14. Removed About Intersil section and updated disclaimer.</td>
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<tr>
<td>Dec 4, 2015</td>
<td>7.00</td>
<td>Added a new User Guide to Related Literature section. Added EVAL2 part numbers to the ordering information table. Added Table 2 on page 5.</td>
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<tr>
<td>Nov 10, 2015</td>
<td>6.00</td>
<td>Added 5x5mmWFQFN information throughout datasheet. Updated Note 1 on page 5 from &quot;Add <code>-T*</code> suffix for tape and reel.&quot; to &quot;Add <code>-T</code> suffix for 6k unit or <code>-T7A</code> suffix for 250 unit tape and reel options.&quot; In &quot;PWM Control Scheme&quot; on page 14 (last sentence) corrected a typo by changing &quot;1.6V to &quot;2.5V&quot;. Table 1 on page 3: Updated L1 row. Updated the &quot;PCB Layout Recommendation&quot; section on page 18. Added POD L16.5x5D.</td>
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<td>Apr 23, 2015</td>
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<td>Updated the 4th Features bullet page 1 by changing value from &quot;0.8%&quot; to &quot;-1.2%/1%&quot;.</td>
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<tr>
<td>Apr 23, 2014</td>
<td>4.00</td>
<td>Updated electrical table, changed Phase minimum on-time MAX from 133ns to 100ns on page 8 Updated electrical table, modified test conditions for Error Amplifier trans-conductance and Power-good Output Low Voltage on page 8 Removed references to VOUT = 0.8V, and 0.9V Added typical curve for Phase minimum on-time vs VIN on page 10 Added description on synchronized control on page 15</td>
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<tr>
<td>Feb 24, 2014</td>
<td>3.00</td>
<td>Updated ESD rating qual references from Jedec standard references to AEC-Q100 standard references on page 7</td>
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<tr>
<td>Dec 13, 2013</td>
<td>2.00</td>
<td>Last Features bullet on page 1: changed from &quot;Qualified for automotive application&quot; to &quot;AEC-Q100 qualified&quot;</td>
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<tr>
<td>Oct 16, 2013</td>
<td>1.00</td>
<td>Initial Release.</td>
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Package Outline Drawings

For the most recent package outline drawing, see L16.3x3D.

L16.3x3D
16 Lead Thin Quad Flat No-Lead Plastic Package
Rev 0, 3/10

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.
For the most recent package outline drawing, see L16.5x5D.

L16.5x5D
16 Lead Quad Flat No-Lead Plastic Package (Punch QFN with Wettable Flank)
Rev 3, 11/2021

Notes:
1. Dimensions are in millimeters.
3. Unless otherwise specified, tolerance: Decimal 0.50
4. Dimension apply to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone illustrated. The pin #1 identifier can be either a mold or mark feature.
7. Edge Protection Technology.
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