ISL76683

Light-to-Digital Output Sensor with Gain Selection, Interrupt Function and I^2C Interface

FN7697
Rev 9.00
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The ISL76683 is an integrated light sensor with an internal integrating ADC intended for automotive applications. The ADC provides 16-bit resolution and is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources. The I^2C interface provides four user programmable lux sensitivity ranges for optimized counts/lux in a variety of lighting conditions. The I^2C interface also provides multi-function control of the sensor and remote monitoring capabilities.

In normal operation, power consumption is less than 300µA. Furthermore, a software power-down mode controlled with the I^2C interface reduces power consumption to less than 1µA.

The ISL76683 supports twin (upper and lower) user programmed thresholds and provides a hardware interrupt that remains asserted low until the host clears it with the I^2C control interface.

The ISL76683 is designed to operate on supplies from 2.5V to 3.3V, and is AEC-Q100 qualified and specified for operation across the -40°C to +105°C (grade 2) ambient temperature range. To achieve this, the ISL76683 is packaged in a special extended temperature clear package.

Related Literature

For a full list of related documents, visit our website

- ISL76683 product page

Features

- Range select with I^2C
  - Range 1 = 0 lux to 1000 lux
  - Range 2 = 0 lux to 4000 lux
  - Range 3 = 0 lux to 16000 lux
  - Range 4 = 0 lux to 64000 lux
- Human eye response (540nm peak sensitivity)
- Temperature compensated
- 16-bit resolution
- Adjustable sensitivity: up to 65 counts per lux
- User-programmable upper and lower threshold interrupt
- Simple output code, directly proportional to lux
- IR + UV rejection
- 50Hz/60Hz rejection
- 2.5V to 3.3V supply
- 6 Ld ODFN (2.1mmx2mm)
- AEC-Q100 qualified
- Pb-free (RoHS compliant)

Applications

- Automotive ambient light sensing
- Backlight control
- Lighting controls

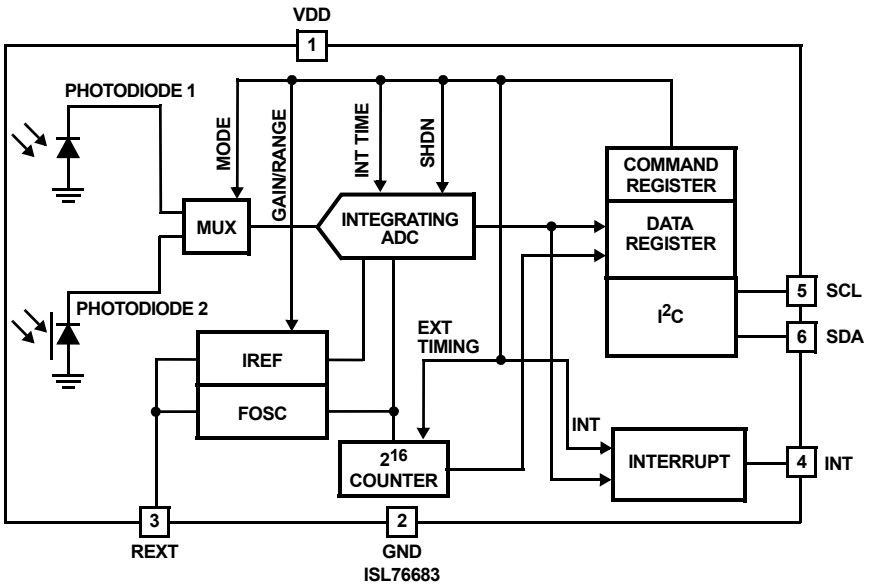
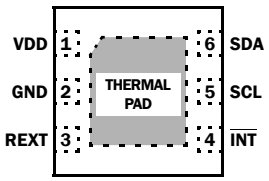


FIGURE 1. BLOCK DIAGRAM

Pin Configuration

ISL76683
(6 LD ODFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	
1	VDD	Positive supply. Connect this pin to a regulated 2.5V to 3.3V supply	
2	GND	Ground pin. The thermal pad is connected to the GND pin	
3	REXT	External resistor pin for ADC reference. Connect this pin to ground through a (nominal) 100kΩ resistor	
4	$\overline{INT}$	Interrupt pin; LO for interrupt/alarming. The $\overline{INT}$ pin is an open drain.	
5	SCL	I^2C serial clock	The I^2C bus lines can be pulled above VDD, 5.5V max
6	SDA	I^2C serial data	

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TEMP RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL76683AROZ-T7	-40 to +105	3k	6 Ld ODFN	L6.2x2.1
ISL76683AROZ-T7A	-40 to +105	250	6 Ld ODFN	L6.2x2.1
ISL76683EVAL1Z	Evaluation Board			

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL76683 product information page. For more information about MSL, refer to TB477.

Absolute Maximum Ratings (T_A = +25°C)

V_{DD}, Supply Voltage between VDD and GND 3.6V
I^2C Bus Pin Voltage (SCL, SDA) . . . . . -0.2V to 5.5V
I^2C Bus Pin Current (SCL, SDA) . . . . . <10mA
INT, R_{EXT} Pin Voltage . . . . . -0.2V to V_{DD}
ESD Rating
Human Body Model (Tested per AEC-Q100-002) 2kV
Machine Model (Tested per AEC-Q100-003) 200V
Charge Device Model (Tested per AEC-Q100-011) 1kV
Latch-Up (Tested per AEC-Q100-004, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
6 Ld ODFN Package (Notes 4, 5)	88	7.94

Maximum Die Temperature . . . . . +105°C
Storage Temperature . . . . . -40°C to +105°C
Operating Temperature . . . . . -40°C to +105°C
Pb-Free Reflow Profile (Note 6) . . . . . see TB477

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside. See TB379.
6. Peak temperature during solder reflow +260°C max.

Electrical Specifications

V_{DD} = 3V, T_A = +25°C, R_{EXT} = 100kΩ 1% tolerance, unless otherwise specified, Internal Timing Mode Operation (see “Principles of Operation” on page 6).

PARAMETER	SYMBOL	TEST CONDITIONS		MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Power Supply Range	V_{DD}			2.25		3.3	V
Supply Current	I_{DD}				0.29	0.33	mA
Supply Current Disabled	I_{DD1}	Software disabled, -40°C to +85°C			0.1	1	µA
		Software disabled, -40°C to +105°C, V_{DD} = 3.3V			0.1	8	µA
Internal Oscillator Frequency	f_{OSC1}	Gain/Range = 1 or 2		290	327	360	kHz
Internal Oscillator Frequency	f_{OSC2}	Gain/Range = 3 or 4		580	655	720	kHz
I^2C Clock Rate	FI^2C			1		400	kHz
Diode1 Dark ADC Code	DATA0	E = 0 lux, Mode1, Gain/Range = 1				5	Counts
Full Scale ADC Code	DATA1					65535	Counts
Diode1 ADC Code Gain/Range = 1 Accuracy	DATA2	Mode1	E = 300 lux, fluorescent light, Gain/Range = 1 (Note 8)	15760	20200	24440	Counts
Diode2 ADC Code Gain/Range = 1 Accuracy	DATA3	Mode2			2020		Counts
Diode1 ADC Code Gain/Range = 2 Accuracy	DATA4	Mode1	E = 300 lux, fluorescent light, Gain/Range = 2 (Note 8)		5050		Counts
Diode2 ADC Code Gain/Range = 2 Accuracy	DATA5	Mode2			505		Counts
Diode1 ADC Code Gain/Range = 3 Accuracy	DATA6	Mode1	E = 300 lux, fluorescent light, Gain/Range = 3 (Note 8)		1262		Counts
Diode2 ADC Code Gain/Range = 3 Accuracy	DATA5	Mode2			126		Counts
Diode1 ADC Code Gain/Range = 4 Accuracy	DATA6	Mode1	E = 300 lux, fluorescent light, Gain/Range = 4 (Note 8)		316		Counts
Diode2 ADC Code Gain/Range = 4 Accuracy	DATA6	Mode2			32		Counts
Voltage of REXT Pin	V_{REF}	-40°C to +85°C		0.485	0.51	0.535	V
		-40°C to +105°C				0.545	V
SCL and SDA Threshold LO	V_{TL}	(Note 9)			1.05		V

Electrical Specifications V_{DD} = 3V, T_A = +25°C, R_{EXT} = 100kΩ 1% tolerance, unless otherwise specified, Internal Timing Mode Operation (see "Principles of Operation" on page 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
SCL and SDA Threshold HI	V_{TH}	(Note 9)		1.95		V
SDA Current Sinking Capability	I_{SDA}		3	5		mA
$\overline{INT}$ Current Sinking Capability	I_{INT}		3	5		mA

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
8. Fluorescent light is substituted by a white LED during production.
9. The voltage threshold levels of the SDA and SCL pins are V_{DD} dependent: V_{TL} = 0.35*V_{DD}. V_{TH} = 0.65*V_{DD}.

Typical Performance Curves (R_{EXT} = 100kΩ)

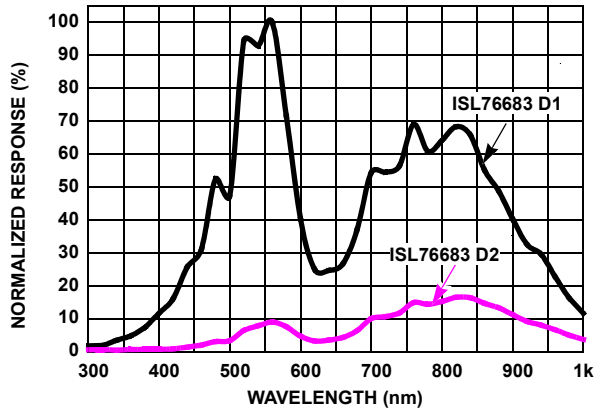


FIGURE 2. SPECTRAL RESPONSE

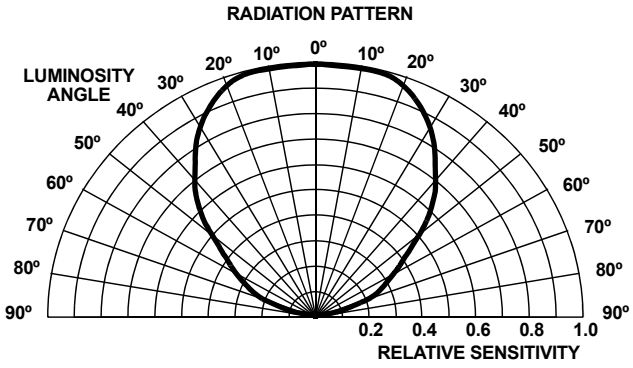


FIGURE 3. RADIATION PATTERN

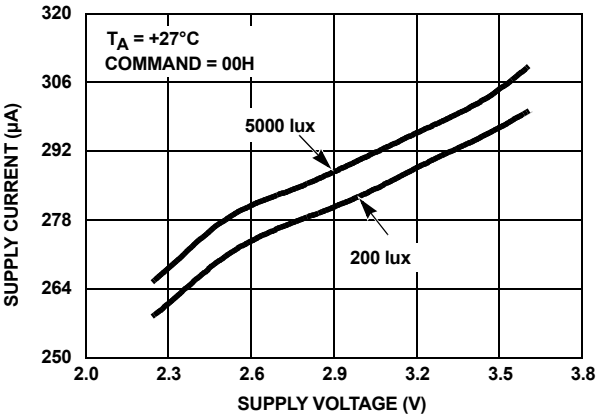


FIGURE 4. SUPPLY CURRENT vs SUPPLY VOLTAGE

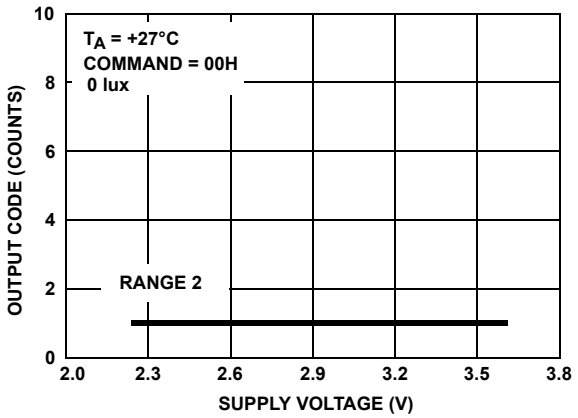


FIGURE 5. OUTPUT CODE FOR 0 LUX vs SUPPLY VOLTAGE

Typical Performance Curves (R_{EXT} = 100kΩ) (Continued)

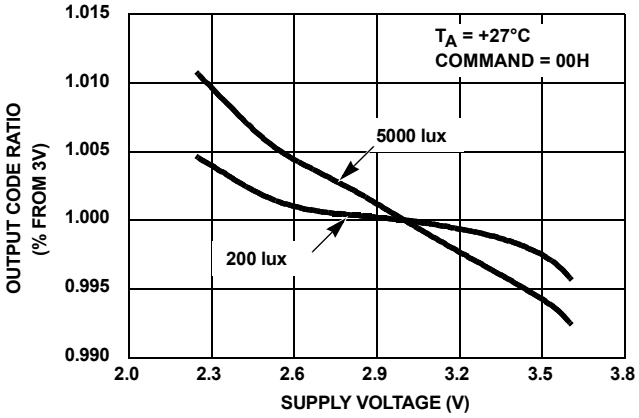


FIGURE 6. OUTPUT CODE vs SUPPLY VOLTAGE

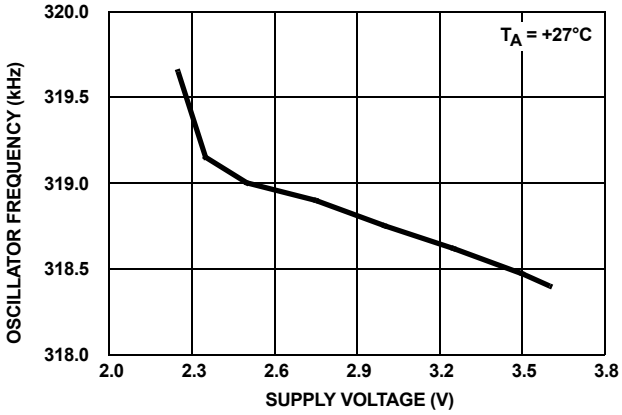


FIGURE 7. OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

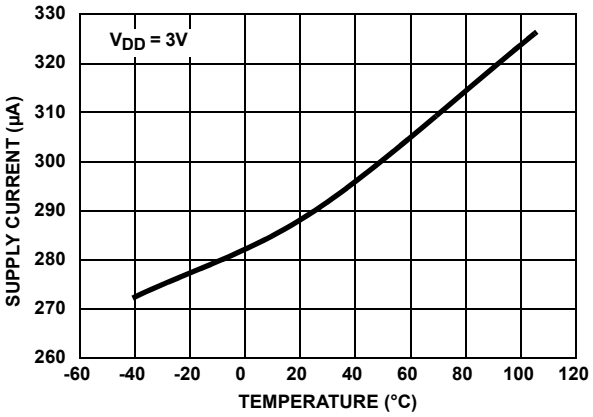


FIGURE 8. SUPPLY CURRENT vs TEMPERATURE

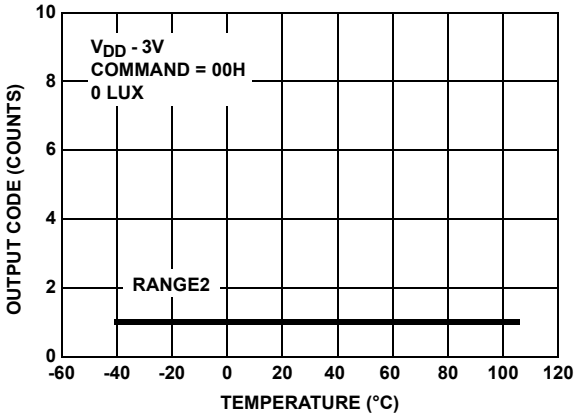


FIGURE 9. OUTPUT CODE FOR 0 LUX vs TEMPERATURE

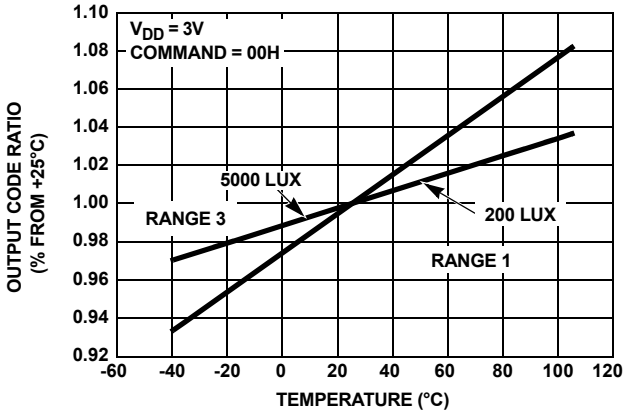


FIGURE 10. OUTPUT CODE vs TEMPERATURE

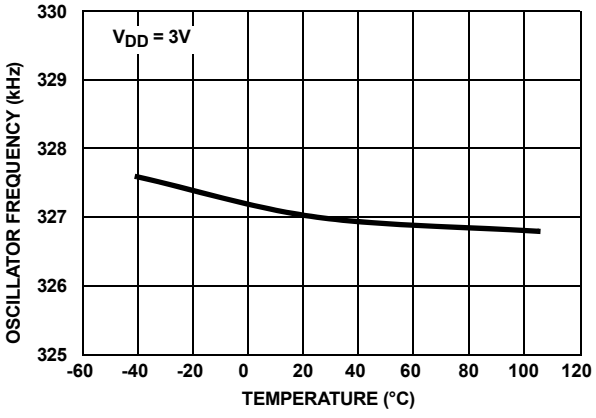


FIGURE 11. OSCILLATOR FREQUENCY vs TEMPERATURE

Principles of Operation

Photodiodes

The ISL76683 contains two photodiodes. Diode1 is sensitive to both visible and infrared light, while Diode2 is sensitive mostly to infrared light. The two diodes' spectral responses are independent from one another. See Figure 2 on page 4 in the "Typical Performance Curves" section. The photodiodes convert light to current, then the diodes' current outputs are converted to digital by a single built-in integrating type 16-bit Analog-to-Digital Converter (ADC). An I^2C command mode determines which photodiode will be converted to a digital signal. Mode1 is Diode1 only. Mode2 is Diode2 only. Mode3 is a sequential Mode1 and Mode2 with an internal subtract function (Diode1 - Diode2).

Analog-to-Digital Converter (ADC)

The converter is a charge-balancing integrating type 16-bit ADC. The chosen method for conversion is best for converting small current signals in the presence of AC periodic noise. For example, a 100ms integration time highly rejects 50Hz and 60Hz power line noise simultaneously. See "Integration Time or Conversion Time" on page 11 and "Noise Rejection" on page 12.

The built-in ADC offers the user flexibility in integration time or conversion time. Two timing modes are available: Internal Timing Mode and External Timing Mode. In Internal Timing Mode, integration time is determined by an internal dual speed oscillator (f_{OSC}), and the n-bit (n = 4, 8, 12, 16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive I^2C External Timing Mode commands. See "External Timing Mode" on page 10. A good balancing act of integration time and resolution depending on the application is required for optimal results.

The ADC has four I^2C programmable range selections to dynamically accommodate various lighting conditions. The ADC can be configured at its lowest range for very dim conditions. The ADC can be configured at its highest range for very bright conditions.

Interrupt Function

The active low interrupt pin is an open-drain pull-down configuration. The interrupt pin serves as an alarm or monitoring function to determine whether the ambient light exceeds the upper threshold or the lower threshold. The user can also configure the persistency of the interrupt pin. This eliminates any false triggers, such as noise or sudden spikes in ambient light conditions. For example, an unexpected camera flash can be ignored by setting the persistency to eight integration cycles.

I^2C Interface

Eight 8-bit registers are available inside the ISL76683. The command and control registers define the operation of the device. The command and control registers do not change until the registers are overwritten. Two 8-bit registers set the high and low interrupt thresholds. There are four 8-bit data Read Only registers; two bytes for the sensor reading and another two bytes for the timer counts. The data registers contain the ADC's latest digital output and the number of clock cycles in the previous integration period.

The ISL76683's I^2C interface slave address is hardwired internally as 1000100. When 1000100x with x as R or $\overline{W}$ is sent after the Start condition, this device compares the first seven bits of this byte to its address and matches.

Figure 12 on page 7 shows a sample one-byte read. Figure 13 on page 7 shows a sample one-byte write. Figure 14 on page 7 shows a sync_iic timing diagram sample for externally controlled integration time. The I^2C bus master always drives the SCL (clock) line, while either the master or the slave can drive the SDA (data) line. Figure 13 shows a sample write. Every I^2C transaction begins with the master asserting a start condition (SDA falling while SCL remains high). The following byte is driven by the master and includes the slave address and read/write bit. The receiving device is responsible for pulling SDA low during the acknowledgment period.

Every I^2C transaction ends with the master asserting a stop condition (SDA rising while SCL remains high).

For more information about the I^2C standard, refer to the Philips I^2C specification documents.

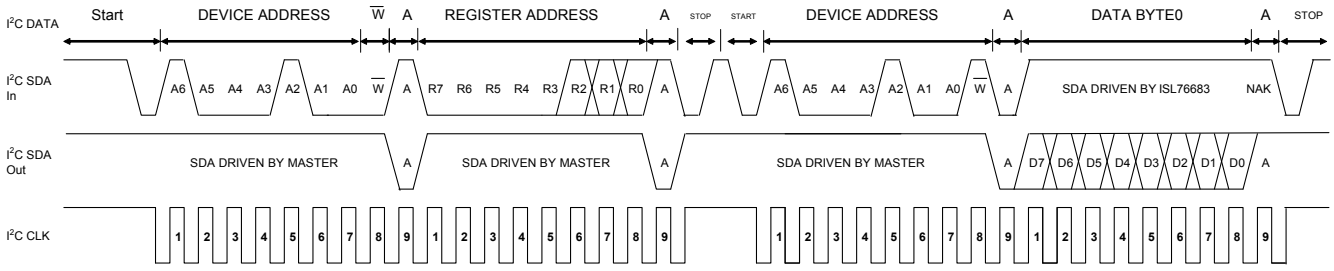


FIGURE 12. I²C READ TIMING DIAGRAM SAMPLE

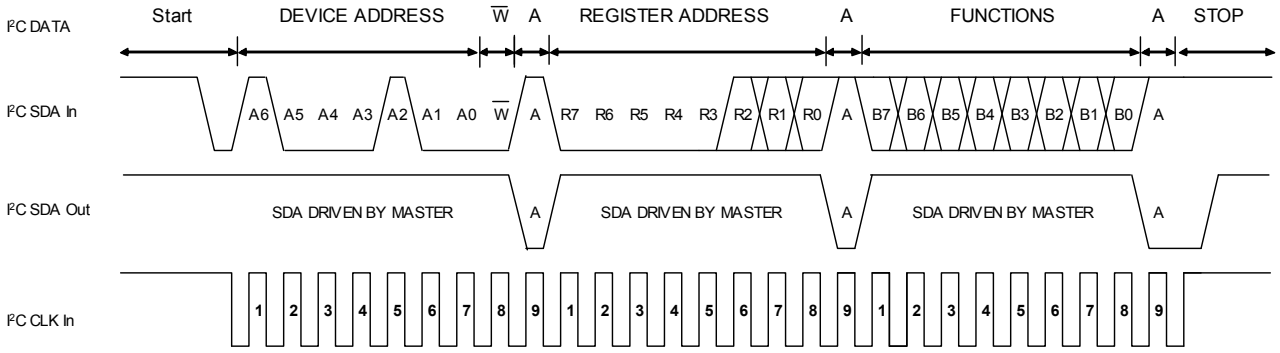


FIGURE 13. I²C WRITE TIMING DIAGRAM SAMPLE

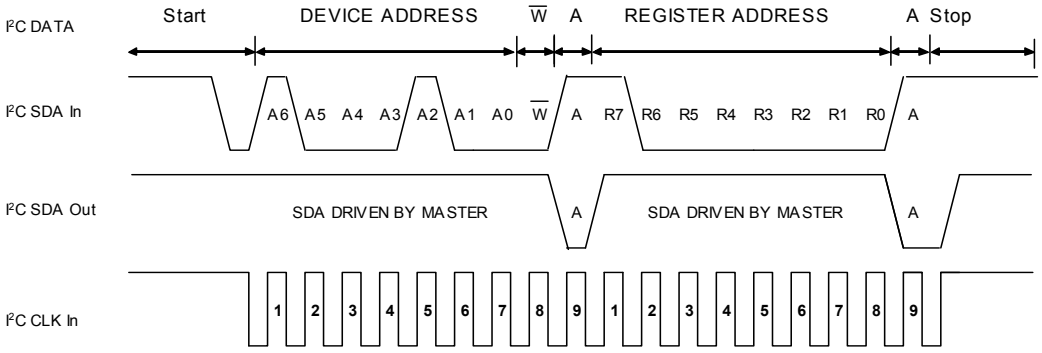


FIGURE 14. I²C sync_iic TIMING DIAGRAM SAMPLE

Register Set

Eight registers are available in the ISL76683. Table 1 summarizes the available registers and their functions.

TABLE 1. REGISTER SET

ADDR (HEX)	REGISTER NAME	BIT(S)	FUNCTION NAME	FUNCTIONS/DESCRIPTION
00	Command	7	Enable	0: Disable ADC-core 1: Enable ADC-core
		6	ADCPD	0: Normal operation 1: Power-down Mode
		5	Timing_Mode	0: Integration is internally timed 1: Integration is externally sync/controlled by I^2C host
		4	Reserved	
		3:2	Mode<1:0>	Selects ADC work mode: 0: Diode1's current to unsigned 16-bit data 1: Diode2's current to unsigned 16-bit data 2: Difference between diodes (I1 - I2) to signed 15-bit data 3: Reserved
		1:0	Width<1:0>	Number of clock cycles; n-bit resolution 0: 2^{16} cycles 1: 2^{12} cycles 2: 2^{8} cycles 3: 2^{4} cycles
01	Control	7	Ext_Mode	Always set to logic 0. Factory use only
		6	Test_Mode	Always set to logic 0
		5	Int_Flag	0: Interrupt is cleared or not yet triggered 1: Interrupt is triggered
		4	Reserved	Always set to logic 0. Factory use only
		3:2	Gain<1:0>	Selects the gain so the range is: 0: 0 to 1000 lux 1: 0 to 4000 lux 2: 0 to 16000 lux 3: 0 to 64000 lux
		1:0	Int_Persist <1:0>	Interrupt is triggered after: 0: 1 integration cycle 1: 4 integration cycles 2: 8 integration cycles 3: 16 integration cycles
02	Interrupt Threshold HI	7:0	Interrupt Threshold HI	High byte of HI interrupt threshold. Default is 0xFF
03	Interrupt Threshold LO	7:0	Interrupt Threshold LO	High byte of the LO interrupt threshold. Default is 0x00
04	LSB_Sensor	7:0	LSB_Sensor	Read-Only data register that contains the Least Significant Byte (LSB) of the latest sensor reading
05	MSB_Sensor	7:0	MSB_Sensor	Read-Only data register that contains the Most Significant Byte (MSB) of the latest sensor reading
06	LSB_Timer	7:0	LSB_Timer	Read-Only data register that contains the LSB of the timer counter value corresponding to the latest sensor reading
07	MSB_Timer	7:0	MSB_Timer	Read-Only data register that contains the MSB of the timer counter value corresponding to the latest sensor reading

TABLE 2. WRITE ONLY REGISTERS

ADDRESS	REGISTER NAME	FUNCTIONS/ DESCRIPTION
b1xxx_xxxx	sync_iic	Writing a logic 1 to this address bit ends the current ADC-integration and starts another. Used with External Timing Mode only
bx1xx_xxxx	clar_int	Writing a logic 1 to this address bit clears the interrupt

Command Register 00(hex)

The Read/Write command register has five functions:

1. Enable; Bit 7. This function either resets the ADC or enables the ADC in normal operation. A logic 0 disables the ADC to reset mode. A logic 1 enables the ADC to normal operation.

TABLE 3. ENABLE

BIT 7	OPERATION
0	Disable ADC-Core to Reset-Mode (default)
1	Enable ADC-Core to Normal Operation

2. ADCPD; Bit 6. This function puts the device in a power-down mode. A logic 0 puts the device in normal operation. A logic 1 powers down the device.

TABLE 4. ADCPD

BIT 6	OPERATION
0	Normal Operation (default)
1	Power-down

For proper shutdown operation, it is recommended to disable the ADC first then disable the chip. First send the I^2C command with Bit 7 = 0, then send the I^2C command with Bit 6 = 1.

3. Timing Mode; Bit 5. This function determines whether the integration time is done internally or externally. In Internal Timing Mode, integration time is determined by an internal dual speed oscillator (f_{OSC}), and the n-bit (n = 4, 8, 12, 16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive external-sync sync_iic pulse commands.

TABLE 5. TIMING MODE

BIT 5	OPERATION
0	Internal Timing Mode. Integration time is internally timed determined by f_{OSC}, REXT, and the number of clock cycles
1	External Timing Mode. Integration time is externally timed by the I^2C host

4. Photodiode Select Mode; Bits 3 and 2. This function controls the mux attached to the two photodiodes. In Mode1, the mux directs the current of Diode1 to the ADC. In Mode2, the mux directs the current of Diode2 only to the ADC. Mode3 is a sequential Mode1 and Mode2 with an internal subtract function (Diode1 - Diode2).

TABLE 6. PHOTODIODE SELECT MODE; BITS 2 AND 3

BITS 3:2	MODE
0:0	MODE1. ADC integrates or converts Diode1 only. Current is converted to an n-bit unsigned data (Note 10)
0:1	MODE2. ADC integrates or coverts Diode2 only. Current is converted to an n-bit unsigned data (Note 10)
1:0	MODE3. A sequential MODE1 then MODE2 operation. The difference current is an (n-1) signed data (Note 10)
1:1	No Operation

NOTE:
10. n = 4, 8, 12, or 16 depending on the number of clock cycles function.

5. Width; Bits 1 and 0. This function determines the number of clock cycles per conversion. Changing the number of clock cycles changes the resolution of the device and changes the integration time, which is the period the device's ADC samples the photodiode current signal for a lux measurement.

TABLE 7. WIDTH

BITS 1:0	NUMBER OF CLOCK CYCLES
0:0	2^{16} = 65536
0:1	2^{12} = 4096
1:0	2^{8} = 256
1:1	2^{4} = 16

Control Register 01(hex)

The Read/Write control register has three functions:

1. Interrupt flag; Bit 5. This is the status bit of the interrupt. The bit is set to logic high when the interrupt thresholds have been triggered, and logic low when not yet triggered.

TABLE 8. INTERRUPT FLAG

BIT 5	OPERATION
0	Interrupt is cleared or not triggered yet
1	Interrupt is triggered

2. Range/Gain; Bits 3 and 2. The Full Scale Range can be adjusted by an external resistor R_{EXT} and/or it can be adjusted with I^2C using the Gain/Range function. Gain/Range has four possible values, Range(k) where k is 1 through 4. Table 9 lists the possible values of Range(k) and the resulting FSR for some typical value R_{EXT} resistors.

TABLE 9. RANGE/GAIN TYPICAL FSR LUX RANGES

BITS 3:2	k	RANGE (k)	FSR LUX RANGE at R_{EXT} = 100k	FSR LUX RANGE at R_{EXT} = 50k	FSR LUX RANGE at R_{EXT} = 500k
0:0	1	973	973	1946	195
0:1	2	3892	3892	7784	778
1:0	3	15,568	15,568	31,136	3114
1:1	4	62,272	62,272	124,544	12,454

3. Interrupt persist; Bits 1 and 0. The interrupt pin and the interrupt flag are triggered/set when the data sensor reading is out of the interrupt threshold window after m consecutive number of integration cycles. The interrupt persist bits determine m.

TABLE 10. INTERRUPT PERSIST

BITS 1:0	NUMBER OF INTEGRATION CYCLES
0:0	1
0:1	4
1:0	8
1:1	16

Interrupt Threshold HI Register 02(hex)

This register sets the HI threshold for the interrupt pin and the interrupt flag. By default, the Interrupt threshold HI is FF(hex). The 8-bit data written to the register represents the upper MSB of a 16-bit value. The LSB is always 00(hex).

Interrupt Threshold LO Register 03(hex)

This register sets the LO threshold for the interrupt pin and the interrupt flag. By default, the Interrupt threshold LO is 00(hex). The 8-bit data written to the register represents the upper MSB of a 16-bit value. The LSB is always 00(hex).

Sensor Data Register 04(hex) and 05(hex)

When the device is configured to output a 16-bit data, the LSB is accessed at 04(hex), and the MSB can be accessed at 05(hex). The sensor data register is refreshed after every integration cycle.

Timer Data Register 06(hex) and 07(hex)

Note that the timer counter value is only available when using the External Timing Mode. The 06(hex) and 07(hex) are the LSB and MSB, respectively, of a 16-bit timer counter value corresponding to the most recent sensor reading. Each clock cycle increments the counter. At the end of each integration period, the value of this counter is made available over the I^2C. This value can be used to eliminate noise introduced by slight timing errors caused by imprecise external timing. For example, microcontrollers often cannot provide high-accuracy command-to-command timing, and the timer counter value can be used to eliminate the resulting noise.

TABLE 11. DATA REGISTERS

ADDRESS (hex)	CONTENTS
04	Least-significant byte of most recent sensor reading.
05	Most-significant byte of most recent sensor reading.
06	Least-significant byte of timer counter value corresponding to most recent sensor reading.
07	Most-significant byte of timer counter value corresponding to most recent sensor reading.

Calculating Lux

The ISL76683's output codes, DATA, are directly proportional to lux.

$$E = \alpha \times DATA \quad \text{(EQ. 1)}$$

The proportionality constant α is determined by the Full Scale Range, FSR, and the n-bit ADC, which is user defined in the command register. The proportionality constant can also be viewed as the resolution; the smallest lux measurement the device can measure is α.

$$\alpha = \frac{FSR}{2^n} \quad \text{(EQ. 2)}$$

Full Scale Range, FSR, is determined by the software programmable Range/Gain, Range(k), in the command register and an external scaling resistor R_{EXT}, which is referenced to 100kΩ.

$$FSR = Range(k) \times \frac{100k\Omega}{R_{EXT}} \quad \text{(EQ. 3)}$$

The transfer function effectively for each timing mode becomes:

INTERNAL TIMING MODE

$$E = \frac{Range(k) \times \frac{100k\Omega}{R_{EXT}}}{2^n} \times DATA \quad \text{(EQ. 4)}$$

EXTERNAL TIMING MODE

$$E = \frac{Range(k) \times \frac{100k\Omega}{R_{EXT}}}{COUNTER} \times DATA \quad \text{(EQ. 5)}$$

n = 4, 8, 12, or 16. This is the number of clock cycles programmed in the command register.

Range(k) is the user defined range in the Gain/Range bit in the command register.

R_{EXT} is an external scaling resistor hardwired to the REXT pin.

DATA is the output sensor reading in number of counts available at the data register.

2^n represents the maximum number of counts possible in Internal Timing Mode. For the External Timing Mode, the maximum number of counts is stored in the data register named COUNTER.

COUNTER is the number increments accrued for between integration time for External Timing Mode.

Gain/Range, Range (k)

The Gain/Range can be programmed in the control register to give Range (k) determining the FSR. Note that Range(k) is not the FSR (see Equation 3). Range(k) provides four constants depending on programmed k that will be scaled by R_{EXT} (see Table 9). Unlike R_{EXT}, Range(k) dynamically adjusts the FSR. This function is especially useful for maintaining excellent resolution when light conditions are varying drastically.

Number of Clock Cycles, n-bit ADC

The number of clock cycles determines "n" in the n-bit ADC; 2^n clock cycles is a n-bit ADC. n is programmable in the command register in the width function. Depending on the application, a good balance of speed and resolution has to be considered when deciding for n. For fast and quick measurement, choose the smallest n = 4. For maximum resolution without regard of time, choose n = 16. Table 12 compares the trade-off between integration time and resolution. See Equations 10 and 11 for the relation between integration time and n. See Equation 3 for the relation between n and resolution.

TABLE 12. RESOLUTION AND INTEGRATION TIME SELECTION

	RANGE1 f_{OSC} = 327kHz		RANGE4 f_{OSC} = 655kHz	
n	t_{INT} (ms)	RESOLUTION LUX/COUNT	t_{INT} (ms)	RESOLUTION (LUX/COUNT)
16	200	0.01	100	1
12	12.8	0.24	6.4	16
8	0.8	3.90	0.4	250
4	0.05	62.5	0.025	4000

NOTE: R_{EXT} = 100kΩ

External Scaling Resistor R_{EXT} and f_{osc}

The ISL76683 uses an external resistor R_{EXT} to fix its internal oscillator frequency, f_{OSC}. Consequently, R_{EXT} determines the f_{OSC}, integration time, and the FSR of the device. f_{OSC}, a dual speed mode oscillator, is inversely proportional to R_{EXT}. For user simplicity, the proportionality constant is referenced to fixed constants 100kΩ and 655kHz:

$$fosc1 = \frac{1}{2} \times \frac{100k\Omega}{R_{EXT}} \times 655kHz \quad \text{(EQ. 6)}$$

$$fosc2 = \frac{100k\Omega}{R_{EXT}} \times 655kHz \quad \text{(EQ. 7)}$$

$f_{OSC}1$ is the oscillator frequency when Range1 or Range2 are set. This is nominally 327kHz when R_{EXT} is 100kΩ.

$f_{OSC}2$ is the oscillator frequency when Range3 or Range4 are set. This is nominally 655kHz when R_{EXT} is 100kΩ.

When the Range/Gain bits are set to Range1 or Range2, f_{OSC} runs at half speed compared to when Range/Gain bits are set to Range3 and Range4.

$$f_{OSC}1 = \frac{1}{2}(f_{OSC}2) \quad \text{(EQ. 8)}$$

The automatic f_{OSC} adjustment feature allows significant improvement of signal-to-noise ratio when detecting very low lux signals.

Integration Time or Conversion Time

Integration time is the period during which the device's ADC samples the photodiode current signal for a lux measurement. Integration time, in other words, is the time to complete the conversion of analog photodiode current into a digital signal (number of counts).

Integration time affects the measurement resolution. For better resolution, use a longer integration time. For short and fast conversions, use a shorter integration time.

The ISL76683 offers user flexibility in the integration time to balance resolution, speed, and noise rejection. Integration time can be set internally or externally and can be programmed in the command register 00(hex) Bit 5.

INTEGRATION TIME IN INTERNAL TIMING MODE

This timing mode is programmed in the command register 00(hex) Bit 5. Most applications use this timing mode. When using the Internal Timing Mode, f_{OSC} and n-bits resolution determine the integration time. t_{int} is a function of the number of clock cycles and f_{OSC}.

$$t_{int} = 2^n \times \frac{1}{f_{osc}} \quad \text{for Internal Timing Mode only} \quad \text{(EQ. 9)}$$

n = 4, 8, 12, and 16. n is the number of bits of resolution.

Therefore, 2^n is the number of clock cycles. n can be programmed at the command register 00(hex) bits 1 and 0.

t_{int} is dual time because f_{OSC} is dual speed depending on the Gain/Range bit. Integration time as a function of R_{EXT} and n is:

$$t_{int1} = 2^n \times \frac{R_{EXT}}{327kHz \times 100k\Omega} \quad \text{(EQ. 10)}$$

t_{int1} is the integration time when the device is configured for Internal Timing Mode and Gain/Range is set to Range1 or Range2.

$$t_{int2} = 2^n \times \frac{R_{EXT}}{655kHz \times 100k\Omega} \quad \text{(EQ. 11)}$$

t_{int2} is the integration time when the device is configured for Internal Timing Mode and Gain/Range is set to Range3 or Range4.

TABLE 13. INTEGRATION TIMES FOR TYPICAL R_{EXT} VALUES (Note 11)

R_{EXT} (kΩ)	RANGE1 RANGE2		RANGE3 RANGE4	
	n = 16-BIT	n = 12-BIT	n = 12-BIT	n = 4
50	100	6.4	3.2	0.013
100 (Note 12)	200	13	6.5	0.025
200	400	26	13	0.050
500	1000	64	32	0.125

NOTES:

11. Integration time in milliseconds.
12. Recommended R_{EXT} resistor value.

INTEGRATION TIME IN EXTERNAL TIMING MODE

This timing mode is programmed in the command register 00(hex) Bit 5. External Timing Mode is recommended when integration time can be synchronized to an external signal (such as a PWM) to eliminate noise.

For Mode1 or Mode2 operation, the integration starts when the sync_iic command is sent over the I^2C lines. The device needs two sync_iic commands to complete a photodiode conversion. The integration then stops when another sync_iic command is received. Writing a logic 1 to the sync_iic bit ends the current ADC integration and starts another one.

For Mode3, the operation is a sequential Mode1 and Mode2. The device needs three sync_iic commands to complete two photodiode measurements. The first sync_iic command starts the conversion of the Diode1. The second sync_iic completes the conversion of Diode1 and starts the conversion of Diode2. The third sync_iic pulse ends the conversion of Diode2 and starts over again to commence conversion of Diode1.

The integration time, t_{int}, is determined by Equation 12:

$$t_{int} = \frac{i_{I^2C}}{f_{I^2C}} \quad \text{(EQ. 12)}$$

i_{I^2C} is the number of I^2C clock cycles to obtain the t_{int}.
f_{I^2C} is the I^2C operating frequency.

The internal oscillator, f_{OSC}, operates identically in both the internal and external timing modes, with the same dependence on R_{EXT}. However, in External Timing Mode, the number of clock cycles per integration is no longer fixed at 2^n. The number of clock cycles varies with the chosen integration time, and is limited to 2^{16} = 65536. To avoid erroneous lux readings, the integration time must be short enough to not allow an overflow in the counter register.

$$t_{int} < \frac{65{,}535}{f_{OSC}} \quad \text{(EQ. 13)}$$

f_{OSC} = 327kHz*100kΩ/R_{EXT} when Range/Gain is set to Range1 or Range2.

f_{OSC} = 655kHz*100kΩ/R_{EXT} when Range/Gain is set to Range3 or Range4.

Noise Rejection

Integrating type ADCs generally have excellent noise-rejection characteristics for periodic noise with frequencies that are an integer multiple of the integration time. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms (k = 1, 2...k_i) is zero. Similarly, setting the device's integration time to an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise.

DESIGN EXAMPLE 1

The ISL76683 will be designed in a portable system. The ambient light conditions that the device will be exposed to are at most 500 lux, which is a good office lighting. The light source has a 50/60Hz power line noise, which is not visible to the human eye. The I^2C clock is 10kHz.

Solution 1 - Using Internal Timing Mode

To achieve both 60Hz and 50Hz AC noise rejection, the integration time must be adjusted to coincide with an integer multiple of the AC noise cycle times.

$$t_{int} = i(1/60Hz) = j(1/50Hz) \quad \text{(EQ. 14)}$$

The first instance of integer values at which t_{int} rejects both 60Hz and 50Hz is when i = 6 and j = 5.

$$t_{int} = 6(1/60Hz) = 5(1/50Hz) \quad \text{(EQ. 15)}$$

$$t_{int} = 100ms$$

Next, determine the Gain/Range. Based on the application condition given, lux(max) = 500 lux, a range of 1000 lux is desirable. This corresponds to a Gain/Range Range1 mode. Impose a resolution of n = 16-bit. Equation 10 determines R_{EXT}.

$$R_{EXT} = \frac{t_{int} \times 327kHz \times 100k\Omega}{2^n} \quad \text{(EQ. 16)}$$

$$\mathbf{R_{EXT} = 50k\Omega}$$

Note: For Internal Timing Mode and Gain/Range set to Range3 or Range4 only.

Equation 3 determines the Full Scale Range, FSR:

$$FSR = 1000\ lux\frac{100k\Omega}{50k\Omega} \quad \text{(EQ. 17)}$$

$$\mathbf{FSR = 2000\ lux}$$

The effective transfer function becomes:

$$\mathbf{E = \frac{data}{2^{16}} \times 2000\ lux} \quad \text{(EQ. 18)}$$

TABLE 14. SOLUTION1 SUMMARY TO EXAMPLE DESIGN PROBLEM

DESIGN PARAMETER	VALUE
t_{int}	100ms
R_{EXT}	50kΩ
Gain/Range Mode	Range1 = 1000 lux
FSR	2000 lux
Number of Clock Cycles	2^{16}
Transfer Function	$E = \frac{DATA}{2^{16}} \times 2000\ lux$

Solution 2 - Using External Timing Mode

From Solution 1, the desired integration time is 100ms. Note that the R_{EXT} resistor only determines the inter oscillator frequency when using External Timing mode. Instead, the integration time is the time between two sync_iic commands sent through the I^2C. The programmer determines how many I^2C clock cycles to wait between two external timing commands.

$i_{I^2C} = f_{I^2C} * t_{int}$ = number of I^2C clock cycles

i_{I^2C} = 10kHz *100ms

i_{I^2C} = 1,000 I^2C clock cycles. An external sync_iic command sent 1000 cycles after another sync_iic command rejects both 60Hz and 50Hz AC noise signals.

Next, pick an arbitrary R_{EXT} = 100kΩ and choose the Gain/Range Mode. For a maximum 500 lux, Range1 is adequate. From Equation 3:

$$FSR = 1000\ lux \frac{100k\Omega}{100k\Omega}$$

$$\mathbf{FSR = 1000\ lux}$$

The effective transfer function becomes:

$$\mathbf{E = \frac{DATA}{COUNTER} \times 1000\ lux}$$

DATA is the sensor reading data located in data registers 04(hex) and 05(hex)

COUNTER is the timer counter value data located in data registers 06(hex) and 07(hex). In this sample problem, COUNTER = 1000.

TABLE 15. SOLUTION 2 SUMMARY TO EXAMPLE DESIGN PROBLEM

DESIGN PARAMETER	VALUE
t_{int}	100ms
R_{EXT}	100kΩ
Gain/Range Mode	Range1 = 1000 lux
FSR	1000 lux
# of Clock Cycles	COUNTER = 1000
Transfer Function	$E = \frac{DATA}{COUNTER} \times 1000\ lux$

IR Rejection

All filament type light sources have a high presence of infrared component invisible to the human eye. A white fluorescent lamp, however, has a low IR content. As a result, output sensitivity may vary depending on the light source. Maximum attenuation of IR can be achieved by properly scaling the readings of Diode1 and Diode2. Obtain data readings from sensor Diode1 (D1), which is sensitive to visible and IR, then read from sensor Diode2 (D2), which is mostly sensitive from IR. Equation 19 describes the method of cancelling IR in Internal Timing mode.

$$D3 = n(D1 - kD2) \quad \text{(EQ. 19)}$$

where:

Data = lux amount in number of counts less IR presence

D1 = data reading of Diode1

D2 = data reading of Diode2

n = 1.85. This is a rounding factor to scale back the sensitivity to ensure Equation 4 is valid.

k = 7.5. This is a scaling factor for the IR sensitive Diode2.

Flat Window Lens Design

A window lens will surely limit the viewing angle of the ISL76683. The window lens should be placed directly on top of the device. The thickness of the lens should be kept at minimum to minimize loss of power due to reflection and also to minimize loss of loss due to absorption of energy in the plastic material. A thickness of t = 1mm is recommended for a window lens design. The bigger the diameter of the window lens, the wider the viewing angle is of the ISL76683. Table 16 on page 14 shows the recommended dimensions of the optical window to ensure both 35° and 45° viewing angle. These dimensions are based on a window lens thickness of 1.0mm and a refractive index of 1.59.

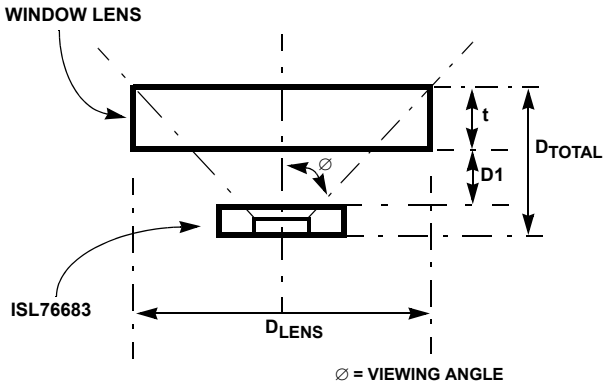


FIGURE 15. FLAT WINDOW LENS

Window with Light Guide Design

If a smaller window is desired while maintaining a wide effective viewing angle of the ISL76683, a cylindrical piece of transparent plastic called the light guide or light pipe is needed to trap the light and focus the light on to the device. The pipe should be placed directly on top of the device with a distance of D1 = 0.5mm to achieve peak performance. The light pipe should have a minimum diameter of 1.5mm to ensure that whole area of the sensor will be exposed (see Figure 16).

TABLE 16. RECOMMENDED DIMENSIONS FOR A FLAT WINDOW DESIGN

D_{TOTAL}	D1	D_{LENS} AT 35° VIEWING ANGLE	D_{LENS} AT 45° VIEWING ANGLE
1.5	0.50	2.25	3.75
2.0	1.00	3.00	4.75
2.5	1.50	3.75	5.75
3.0	2.00	4.30	6.75
3.5	2.50	5.00	7.75

t = 1	Thickness of lens
D1	Distance between ISL76683 and inner edge of lens
D_{LENS}	Diameter of lens
D_{TOTAL}	Distance constraint between the ISL76683 and lens outer edge

NOTE: All dimensions are in mm.

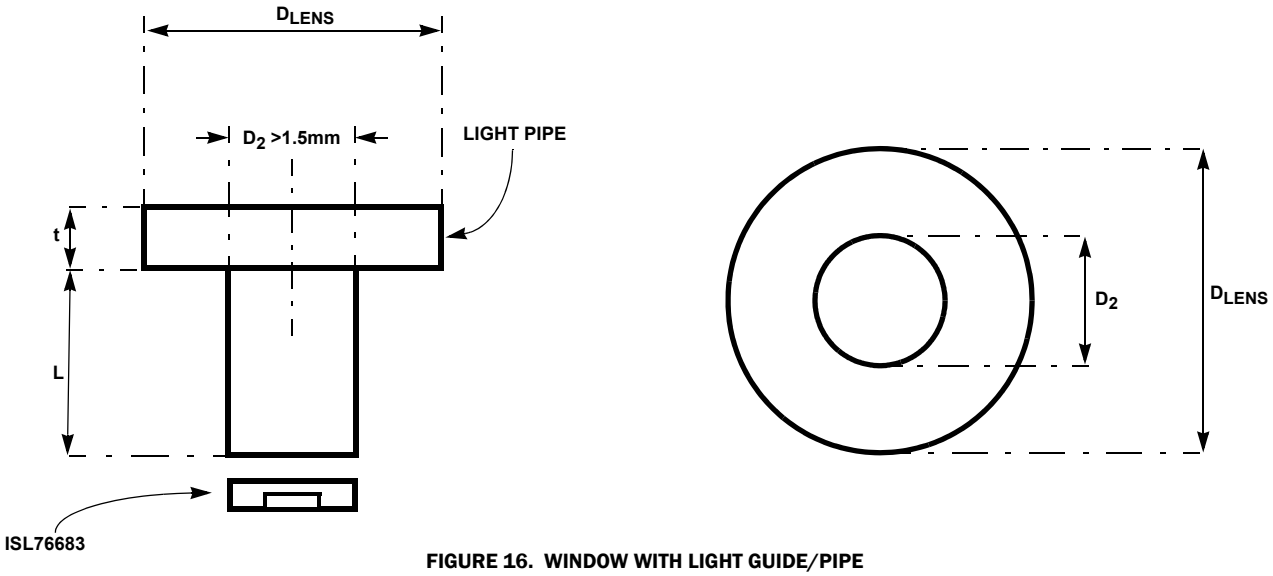


FIGURE 16. WINDOW WITH LIGHT GUIDE/PIPE

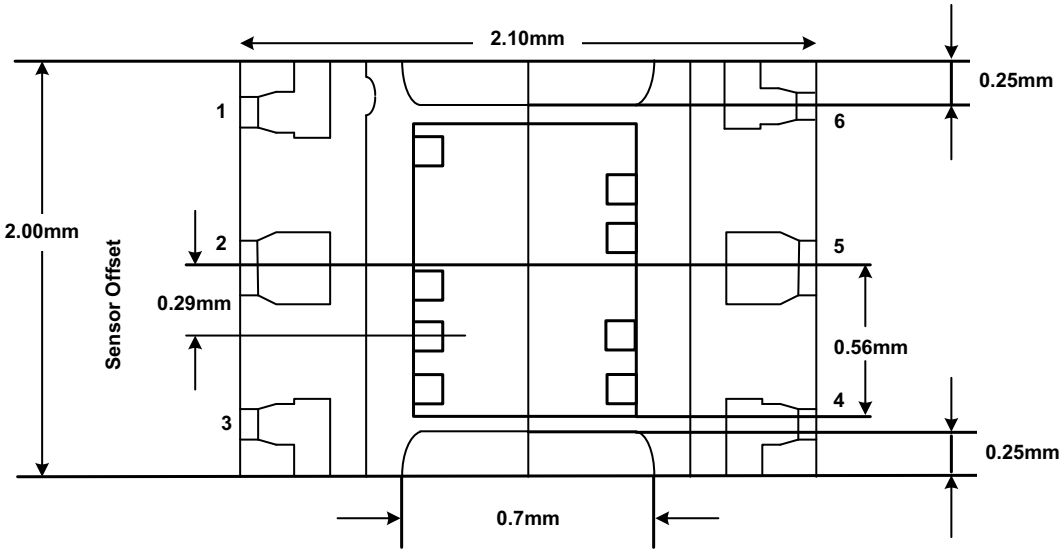


FIGURE 17. SENSOR LOCATION DRAWING

Suggested PCB Footprint

Footprint pads should be a nominal 1-to-1 correspondence with package pads. Because ambient light sensor devices do not dissipate high power, heat dissipation through the exposed pad is not important; instead, similar to DFN or QFN, the exposed pad provides robustness in board mount process. Renesas recommends mounting the exposed pad to the PCB, but this is not mandatory.

Layout Considerations

The ISL76683 is relatively insensitive to layout. Like other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. The following considerations will ensure the best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use two power supply decoupling capacitors, 4.7µF and 0.1µF, placed close to the device.

Typical Circuit

A typical application for the ISL76683 is shown in Figure 18. The ISL76683's I^2C address is internally hardwired as 1000100. The device can be tied onto a system's I^2C bus together with other I^2C compliant devices.

Soldering Considerations

Convection heating is recommended for reflow soldering; direct infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile, and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

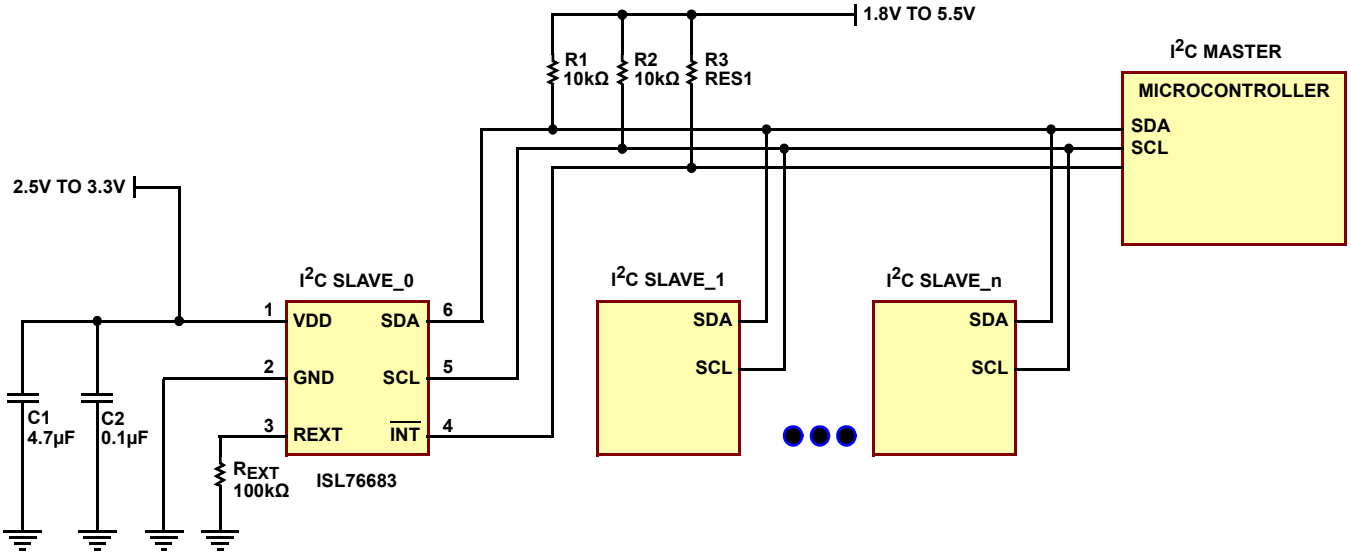


FIGURE 18. ISL76683 TYPICAL CIRCUIT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Mar 2, 2018	FN7697.9	Applied Renesas logo in header and footer. Updated Related Literature section on page 1. Updated Figure 17 on page 14. Removed About Intersil section and added Renesas disclaimer.
Feb 26, 2016	FN7697.8	Removed sentence from “IR Rejection” on page 13, which referred to Figure 2. Added Tape and Reel column to show units in “Ordering Information Table” on page 2. Abs Max Ratings on page 3 - changed testing information from “Charge Device Model (Tested per JESD22-C101C)” to “Charge Device Model (Tested per AEC-Q100-011)”. “Human Body Model (Tested per JESD22-A114E)” to Human Body Model (Tested per AEC-Q100-002)”. “Machine Model (Tested per JESD-A115-A)” to Machine Model (Tested per AEC-Q100-003). “Latch-up (Tested per JESD78B” to Latch-Up (Tested per AEC-Q100-004, Class II, Level A). Updated POD to most current revision. Revision POD change is as follows: Changed Note 5 From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and maybe located on any of the 4 sides (or ends).
Mar 24, 2014	FN7697.7	Added AEC-Q100 qualified to features on page 1. Added Related Literature on page 1. Added Eval board to ordering information on page 2. Updated Figure 17 Sensor Location Drawing with Pin 1 Marking.
Dec 23, 2013	FN7697.6	Page 16 - 2nd line of the disclaimer changed from: "Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted" to: "Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted"
Jul 22, 2013	FN7697.5	Removed Confidential Watermark, Updated Product Information verbiage to About Intersil verbiage.
Oct 30, 2012	FN7697.4	Added ISL76683AROZ-T7A to “Ordering Information” on page 2. Updated “Package Outline Drawing” on page 17. Added "MAX 0.75" dimension to Side View.
Jul 9, 2012	FN7697.3	In “Control Register 01(hex)” on page 9, removed sentence: “Writing a logic low clears/resets the status bit.” from “1. Interrupt flag; Bit 5”
Mar 8, 2011	FN7697.2	Changed TechBrief reference in ordering information for MSL info from TB363 to TB477.
Jan 24, 2011	FN7697.1	Initial Release to web.

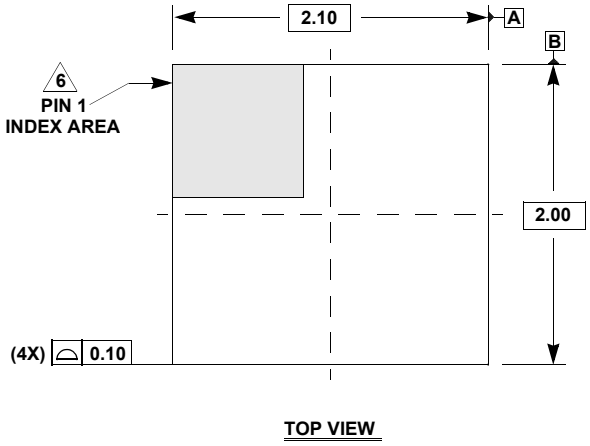
Package Outline Drawing

For the most recent package outline drawing, see L6.2x2.1.

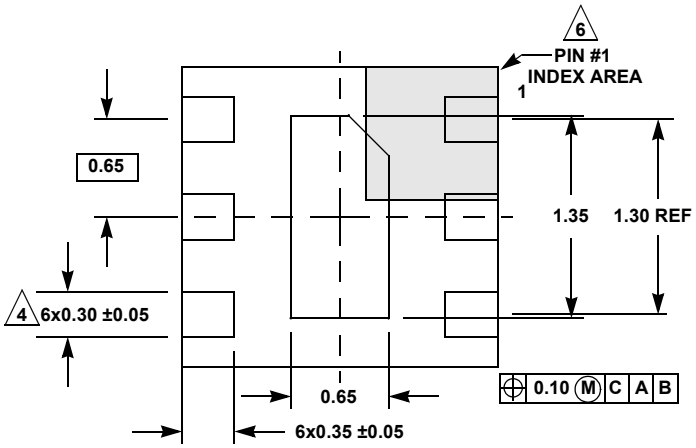
L6.2x2.1

6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)

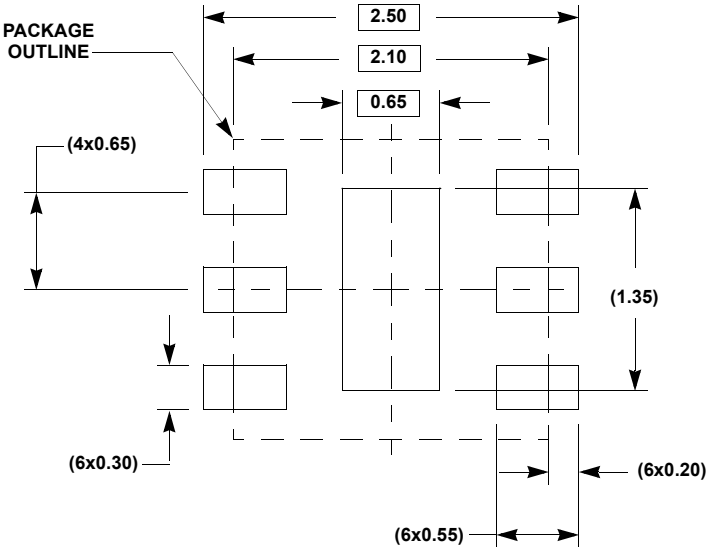
Rev 4, 2/15



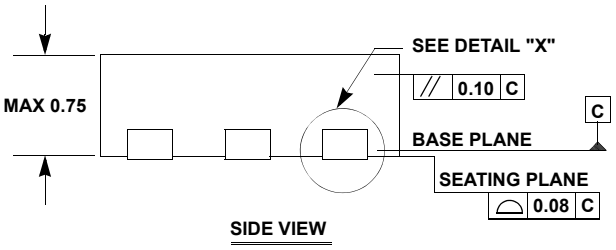
TOP VIEW



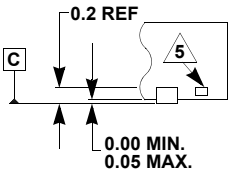
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and maybe located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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(Rev.4.0-1 November 2017)

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