

ISL7457SRH

Radiation Hardened, SEE Hardened, Non-Inverting, Quad CMOS Driver

FN6874
Rev.4.0
May 6, 2021

The [ISL7457SRH](#) is a radiation hardened, SEE hardened, high speed, non-inverting, quad CMOS driver. It is capable of running at clock rates up to 40MHz and features 2A typical peak drive capability and a nominal ON-resistance of just 3.5Ω. The ISL7457SRH is ideal for driving highly capacitive loads, such as storage and vertical clocks in CCD applications. It is also well suited to level-shifting and clock-driving applications.

Each output of the ISL7457SRH can be switched to either the high (V_H) or low (V_L) supply pins, depending on the related input pin. The inputs are compatible with both 3.3V and 5V CMOS logic. The Output Enable (OE) pin can be used to put the outputs into a high-impedance state. This is especially useful in CCD applications that disable the driver during power-down.

The ISL7457SRH also features very fast rise and fall times, which are typically matched to within 1ns. The propagation delay is also matched between rising and falling edges to typically within 1.5ns.

The ISL7457SRH is available in a 16 Ld ceramic flatpack package and specified for operation across the full -55°C to +125°C ambient temperature range.

Applications

- CCD drivers, clock/line drivers, level-shifters

Features

- Electrically screened to SMD [5962-08230](#)
- QML qualified per MIL-PRF-38535 requirements
- Full mil-temp range operation: T_A = -55°C to +125°C
- Radiation hardness
 - TID [50-300 rad(Si)/s]: 10krad(Si) minimum
- **SEE hardness**
 - LET (SEL and SEB Immunity): 40MeV/mg/cm² minimum
 - LET [SET = ΔV_{OUT} < 15V, Δt < 500ns]: 40MeV/mg/cm²
- 4 channels
- Clocking speeds up to 40MHz
- 11ns/12ns typical t_R/t_F with 1nF Load (15V bias)
- 1ns typical rise and fall time match (15V bias)
- 1.5ns typical prop delay match (15V bias)
- Low quiescent current - < 1mA Typical
- Fast output enable function - 12ns typical (15V bias)
- Wide output voltage range
 - 0V ≤ V_L ≤ 8V
 - 2.5V ≤ V_H ≤ 16.5V
- 2A typical peak drive current (15V Bias)
- 3.5Ω typical ON-resistance (15V bias)
- Input level shifters
- 3.3V/5V CMOS compatible inputs

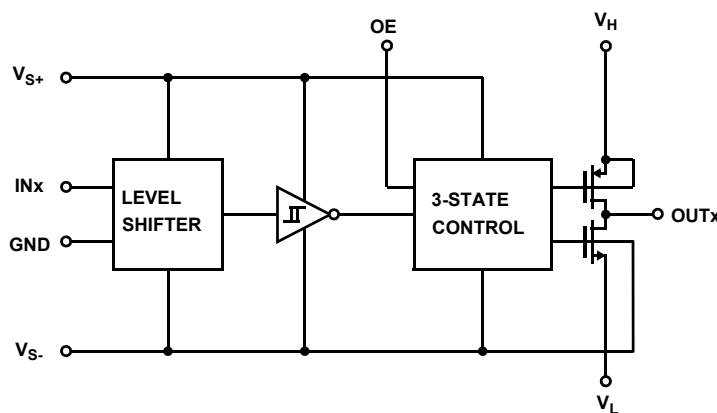


Figure 1. Block Diagram

1. Overview

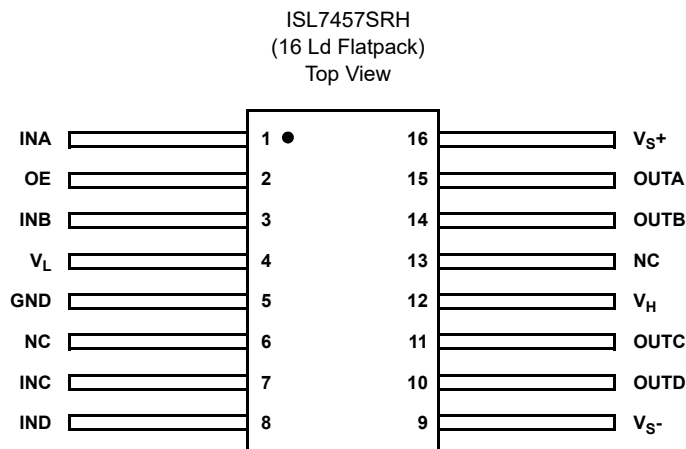
1.1 Ordering Information

Ordering SMD Number (Note 1)	Part Number (Note 2)	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Temp. Range
5962D0823001QXC	ISL7457SRHQF	16 Ld Flatpack	K16.A	Tray	-55 to +125°C
5962D0823001VXC	ISL7457SRHVF			Tray	
NA	ISL7457SRHF/PROTO (Note 3)			Tray	
5962D0823001V9A	ISL7457SRHVX (Note 4)	Die	-	-	
NA	ISL7457SRHX/SAMPLE (Notes 3, 4)				
	ISL7457SRHEVAL2Z (Note 5)	Evaluation Board			

Notes:

- Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
- These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
- The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
- Die product tested at $T_A = +25^\circ\text{C}$. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in ["Electrical Specifications" on page 5](#).
- Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

1.2 Pin Configuration



1.3 Pin Descriptions

Pin Number	Pin Name	Function	Equivalent Circuit
1	INA	Input Channel A	<p>CIRCUIT 1</p>
2	OE	Output enable	(Reference Circuit 1)
3	INB	Input Channel B	(Reference Circuit 1)
4	V _L	Low voltage input pin	
5	GND	Input logic ground	
6, 13	NC	No connection	
7	INC	Input Channel C	(Reference Circuit 1)
8	IND	Input Channel D	(Reference Circuit 1)
9	V _{S-}	Negative supply voltage	
10	OUTD	Output Channel D	<p>CIRCUIT 2</p>
11	OUTC	Output Channel C	(Reference Circuit 2)
12	V _H	High voltage input pin	
14	OUTB	Output Channel B	(Reference Circuit 2)
15	OUTA	Output Channel A	(Reference Circuit 2)
16	V _{S+}	Positive supply voltage	

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage (+Vs to -Vs)		18	V
Input Voltage	-Vs - 0.3	+Vs +0.3	V
Input Current		10	mA
Continuous Output Current per Output		100	mA
Power Dissipation (P_D)			
$T_A = +25^\circ\text{C}$ (Derate linearly at 10.1mW/°C above $T_A = +25^\circ\text{C}$)		1.26	W
$T_A = +125^\circ\text{C}$ (Derate linearly at 10.1mW/°C above $T_A = +125^\circ\text{C}$)		0.25	W
$T_C = +25^\circ\text{C}$ (Derate linearly at 66.7mW/°C above $T_C = +25^\circ\text{C}$)		8.33	W
$T_C = +125^\circ\text{C}$ (Derate linearly at 66.7mW/°C above $T_C = +125^\circ\text{C}$)		1.66	W
ESD Rating		Value	Unit
Human Body Model		1	kV
Charged Device Model		1.5	kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld Flatpack (Notes 6, 7)	99	15

Notes:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board. See [TB379](#).
7. For θ_{JC} , the "case temp" location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage (+Vs to -Vs)	4.5	16.5	V
Ambient Operating Temperature Range	-55	+125	°C

2.4 Electrical Specifications

Typical values reflect $V_{S+} = V_H = 5V$, $V_{S-} = V_L = 0V$, $OE = V_{S+}$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
Logic "1" Input Voltage	V_{IH}		2	1.3		V
Logic "1" Input Current	I_{IH}	$INx = V_{S+}$	-10	0.01	10	μA
Logic "0" Input Voltage	V_{IL}			1.23	0.8	V
Logic "0" Input Current	I_{IL}	$INx = 0V$	-10	0.005	10	μA
Input Capacitance	C_{IN}	$T_A = +25^{\circ}C$		5.7		pF
Input Resistance	R_{IN}	$T_A = +25^{\circ}C$		500		M Ω
Output						
ON-Resistance V_H to $OUTx$	R_{OH}	$INx = V_{S+}$, $I_{OUTx} = -100mA$		8	15	Ω
ON-Resistance V_L to $OUTx$	R_{OL}	$INx = 0V$, $I_{OUTx} = +100mA$		6	12	Ω
Positive Output Leakage Current	I_{LEAK+}	$INx = V_{S+}$, $OE = 0V$, $OUTx = V_{S+}$		0.005	10	μA
Negative Output Leakage Current	I_{LEAK-}	$INx = V_{S+}$, $OE = 0V$, $OUTx = V_{S-}$	-10	-0.005		μA
Power Supply						
V_{S+} Supply Current	I_{S+}	$INx = 0V$ and V_{S+}		0.2	1.5	mA
V_{S-} Supply Current	I_{S-}	$INx = 0V$ and V_{S+}	-1.5	-0.2		mA
V_H Supply Current	I_H	$INx = 0V$ and V_{S+}		0.1	10	μA
V_L Supply Current	I_L	$INx = 0V$ and V_{S+}	-10	-0.1		μA
Switching Characteristics						
Rise Time	t_R	$INx = 0V$ to 4.5V step, $C_L = 1nF$		23	47	ns
Fall Time	t_F	$INx = 4.5V$ to 0V step, $C_L = 1nF$		20	36	ns
t_R , t_F Mismatch	t_{RFA}	$C_L = 1nF$		3	5	ns
Turn-On Delay Time	t_{D+}	$INx = 0V$ to 4.5V step, $C_L = 1nF$		20	38	ns
Turn-Off Delay Time	t_{D-}	$INx = 4.5V$ to 0V step, $C_L = 1nF$		22	40	ns
t_{D+} , t_{D-} Mismatch	t_{DD}	$C_L = 1nF$		2	4	ns
Enable Delay Time	t_{ENABLE}	$INx = V_{S+}$, $OE = 0V$ to 4.5V step, $R_L = 1k\Omega$		21	68	ns
Disable Delay Time	$t_{DISABLE}$	$INx = V_{S+}$, $OE = 4.5V$ to 0V step, $R_L = 1k\Omega$		46	70	ns

Typical values reflect $V_{S+} = V_H = 15V$, $V_{S-} = V_L = 0V$, $OE = V_{S+}$, $T_A = +25^\circ C$, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
Logic "1" Input Voltage	V_{IH}		2.4	1.63		V
Logic "1" Input Current	I_{IH}	$INx = V_{S+}$	-10	0.01	10	μA
Logic "0" Input Voltage	V_{IL}			1.4	0.8	V
Logic "0" Input Current	I_{IL}	$INx = 0V$	-10	0.005	10	μA
Input Capacitance	C_{IN}	$T_A = +25^\circ C$		5.7		pF
Input Resistance	R_{IN}	$T_A = +25^\circ C$		1.5		$G\Omega$
Output						
ON-Resistance V_H to $OUTx$	R_{OH}	$INx = V_{S+}$, $I_{OUTx} = -100mA$		3.5	6	Ω
ON-Resistance V_L to $OUTx$	R_{OL}	$INx = 0V$, $I_{OUTx} = +100mA$		3	6	Ω
Positive Output Leakage Current	I_{LEAK+}	$INx = V_{S+}$, $OE = 0V$, $OUTx = V_{S+}$		0.015	10	μA
Negative Output Leakage Current	I_{LEAK-}	$INx = V_{S+}$, $OE = 0V$, $OUTx = V_{S-}$	-10	-0.015		μA
Power Supply						
V_{S+} Supply Current	I_{S+}	$INx = 0V$ and V_{S+}		0.8	5	mA
V_{S-} Supply Current	I_{S-}	$INx = 0V$ and V_{S+}	-5	-0.8		mA
V_H Supply Current	I_H	$INx = 0V$ and V_{S+}		0.1	13	μA
V_L Supply Current	I_L	$INx = 0V$ and V_{S+}	-10	0.1		μA
Switching Characteristics						
Rise Time	t_R	$INx = 0V$ to $5V$ step, $C_L = 1nF$		11	20	ns
Fall Time	t_F	$INx = 5V$ to $0V$ step, $C_L = 1nF$		12	20	ns
t_R , t_F Mismatch	$t_{R\Delta}$	$C_L = 1nF$		1	3	ns
Turn-On Delay Time	t_{D+}	$INx = 0V$ to $5V$ step, $C_L = 1nF$		11.5	30	ns
Turn-Off Delay Time	t_{D-}	$INx = 5V$ to $0V$ step, $C_L = 1nF$		13	24	ns
t_{D+} , t_{D-} Mismatch	t_{DD}	$C_L = 1nF$		1.5	5	ns
Enable Delay Time	t_{ENABLE}	$INx = V_{S+}$, $OE = 0V$ to $5V$ step, $R_L = 1k\Omega$		12	30	ns
Disable Delay Time	$t_{DISABLE}$	$INx = V_{S+}$, $OE = 5V$ to $0V$ step, $R_L = 1k\Omega$		27	70	ns

3. Typical Performance Curves (Pre-Rad)

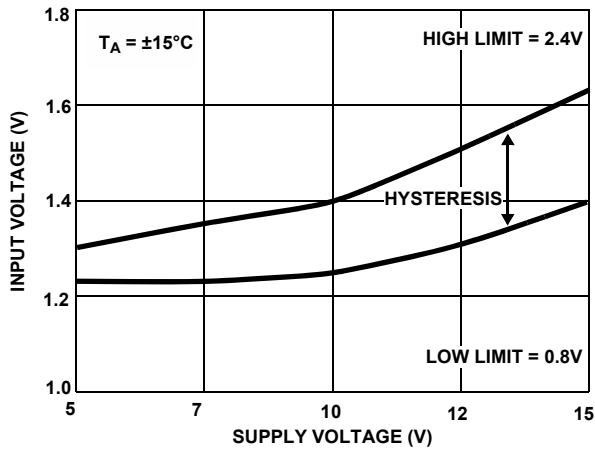


Figure 2. Switch Threshold vs Supply Voltage

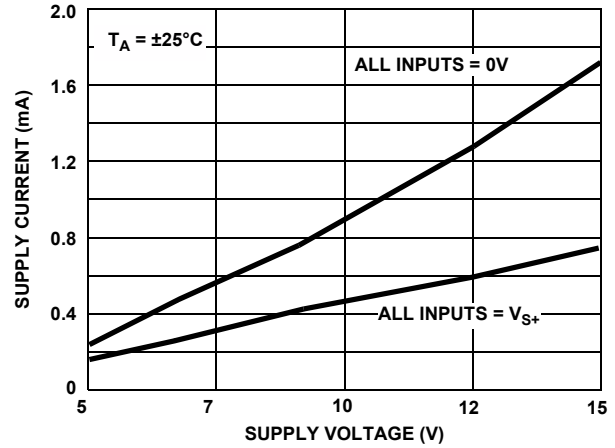


Figure 3. Quiescent Supply Current vs Supply Voltage

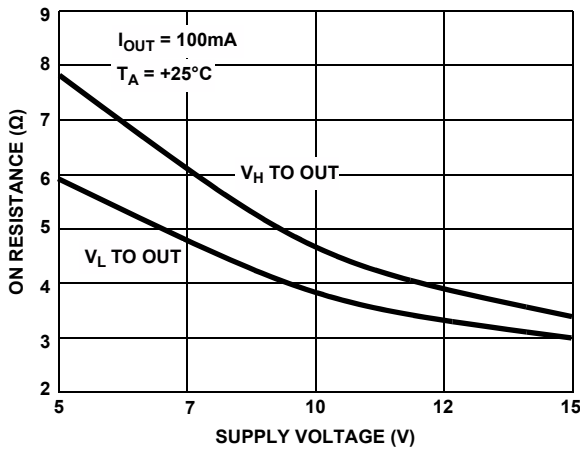


Figure 4. ON-Resistance vs Supply Voltage

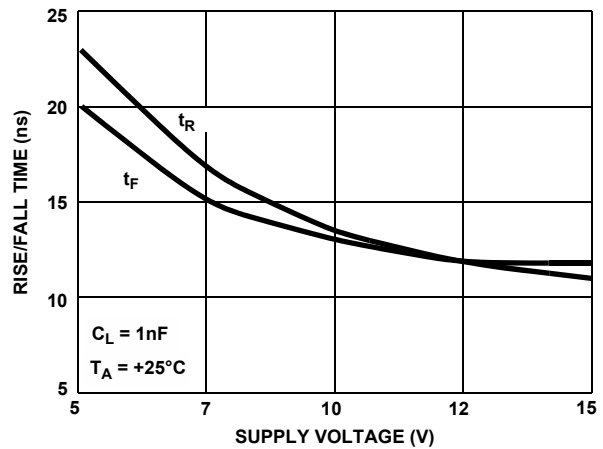


Figure 5. Rise/Fall Time vs Supply Voltage

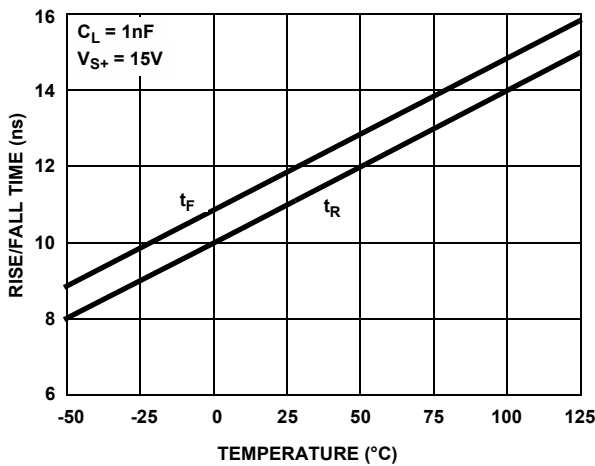


Figure 6. Rise/Fall Time vs Temperature

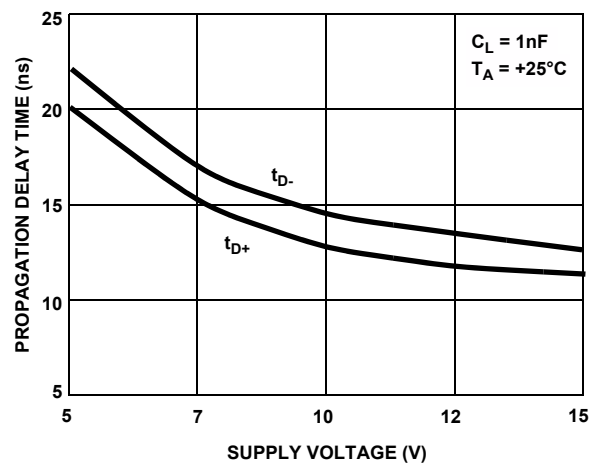


Figure 7. Propagation Delay Time vs Supply Voltage

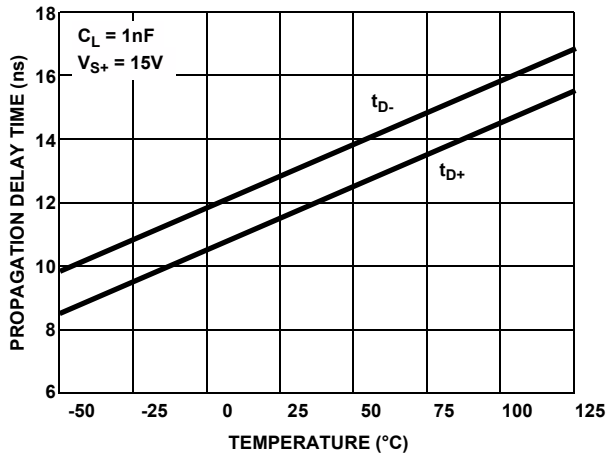


Figure 8. Propagation Delay Time vs Temperature

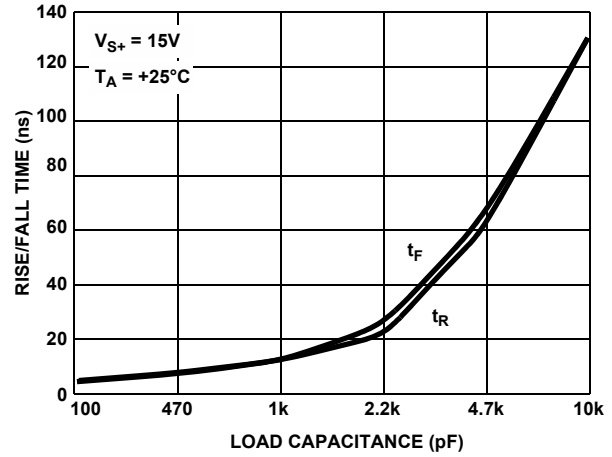


Figure 9. Rise/Fall Time vs Load Capacitance

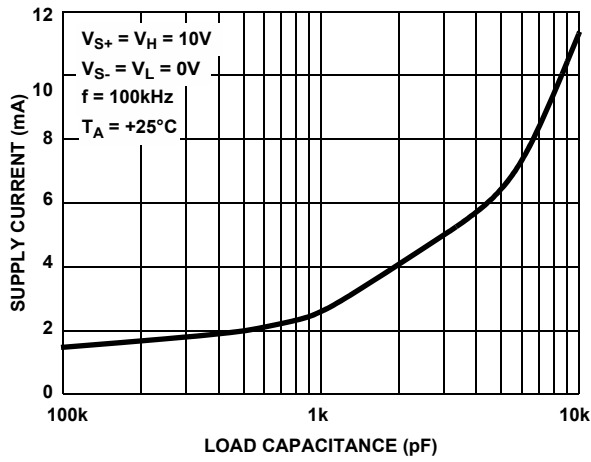


Figure 10. Supply Current Per Channel vs Load Capacitance

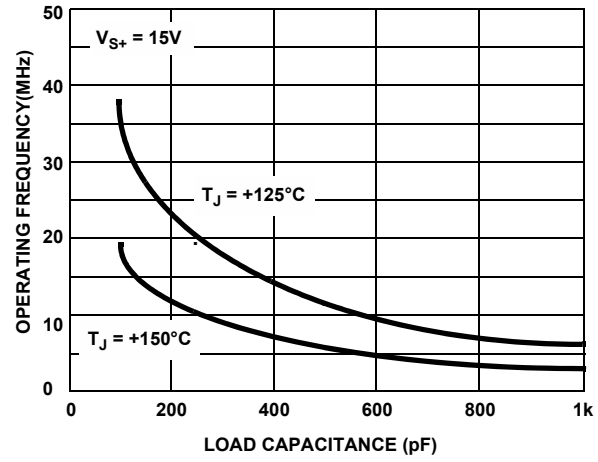


Figure 11. Operating Frequency vs Load Capacitance Derating Curves

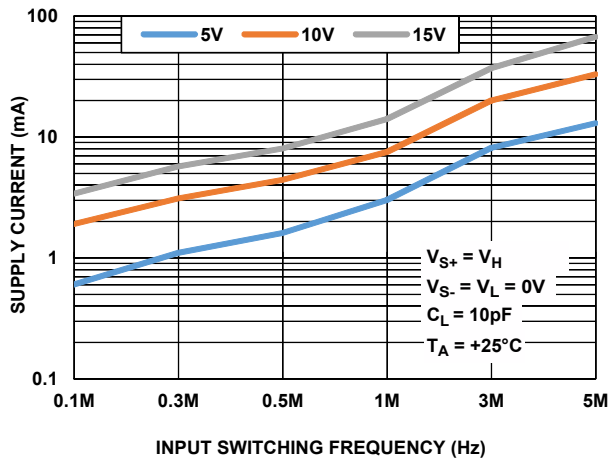


Figure 12. Supply Current for All 4 Channels vs Voltage and Switching Frequency

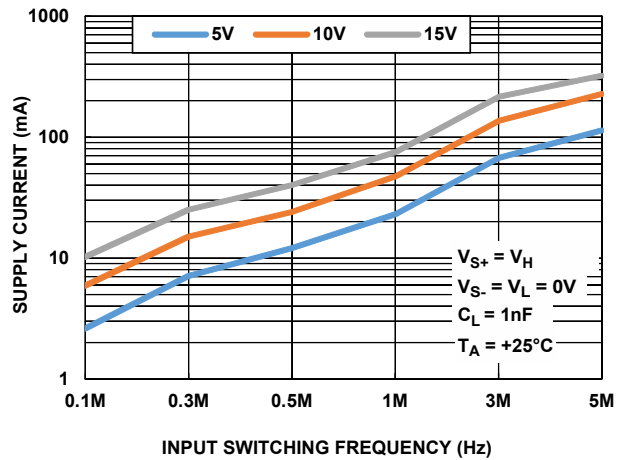


Figure 13. Supply Current for All 4 Channels vs Voltage and Switching Frequency

Table 1. Operating Voltage Range

Pin	Minimum	Maximum
V_{S+} to V_{S-}	4.5V	16.5V
V_{S-} to GND	0V	0V
V_H	$V_{S-} + 2.5V$	V_{S+}
V_L	V_{S-}	V_{S+}
V_H to V_L	0V	16.5V
V_L to V_{S-}	0V	8V

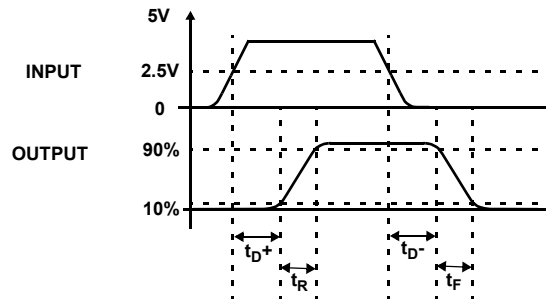


Figure 14. Timing Diagram

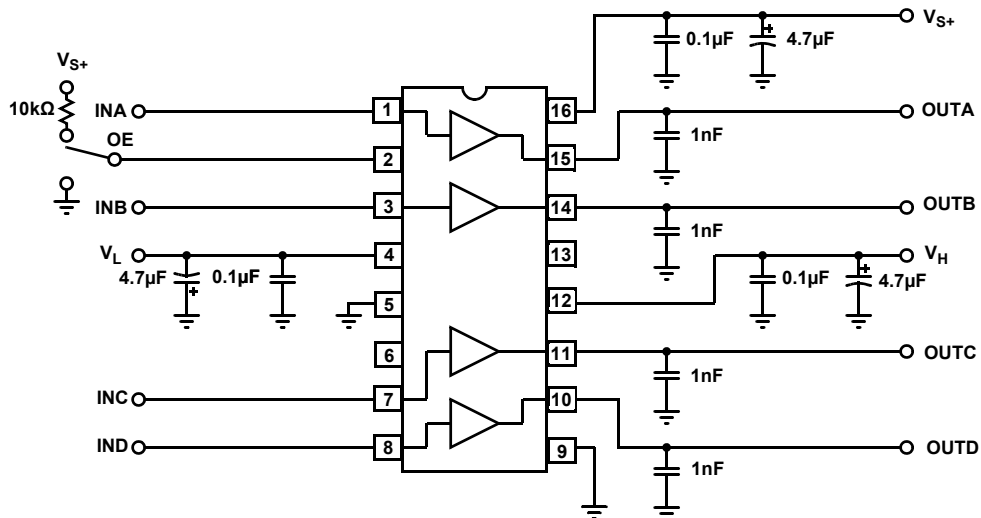


Figure 15. Standard Test Configuration

4. Application Information

4.1 Product Description

The ISL7457SRH is a high performance, high speed quad CMOS driver. Each channel of the ISL7457SRH consists of a single P-channel high-side driver and a single N-channel low-side driver. These 3.5Ω devices will pull the output (OUTx) to either the high or low voltage, on V_H and V_L respectively, depending on the input logic signal (INx). It should be noted that there is only one set of high and low voltage pins.

A common Output Enable (OE) pin is available on the ISL7457SRH. When this pin is pulled low, it will put all outputs in a high impedance state.

4.2 Supply Voltage Range and Input Compatibility

The ISL7457SRH is designed to operate on nominal 5V to 15V supplies with ±10% tolerance. [Table 1 on page 9](#) shows the specifications for the relationship between the V_{S+}, V_{S-}, V_H, V_L, and GND pins. The ISL7457SRH does not contain a true analog switch and therefore V_L should always be less than V_H.

All input pins are compatible with both 3.3V and 5V CMOS signals.

4.3 PCB Layout Guidelines

- (1) A ground plane must be used, preferably located on layer #2 of the PCB.
- (2) Connect the GND and V_{S-} pins directly to the ground plane.
- (3) The V_{S+}, V_H and V_L pins should be bypassed directly to the ground plane using a low-ESR, 4.7μF solid tantalum capacitor in parallel with a 0.1μF ceramic capacitor. Locate all bypass capacitors as close as possible to the respective pins of the IC.
- (4) Keep all input and output connections to the IC as short as possible.
- (5) For high frequency operation above 1MHz, consider use of controlled impedance traces terminated into 50Ω on all inputs and outputs.

4.4 Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the ISL7457SRH drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation, die temperature must be kept below T_{JMAX} (+150°C).

Power dissipation can be calculated as shown in [\(EQ. 1\)](#):

$$P_D = (V_S \times I_S) + \sum_1^4 [(C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)] \quad (\text{EQ. 1})$$

where:

- P_D is the power dissipated in the device.
- V_S is the total power supply to the ISL7457SRH (from V_{S+} to V_{S-}).
- I_S is the quiescent supply current.
- C_{INT} is the internal load capacitance (150pF).
- f is the operating frequency.
- C_L is the load capacitance.
- V_{OUT} is the swing on the output (V_H - V_L).

4.5 Junction Temperature Calculation

After the power dissipation for the application is determined, the maximum junction temperature can be calculated as shown in [\(EQ. 2\)](#):

$$T_{JMAX} = T_{SMAX} + (\theta_{JC} + \theta_{CS}) \times P_D \quad (\text{EQ. 2})$$

where:

- T_{JMAX} is the maximum operating junction temperature (+150°C).
- T_{SMAX} is the maximum operating sink temperature of the PCB.
- θ_{JC} is the thermal resistance, junction-to-case, of the package.
- θ_{CS} is the thermal resistance, case-to-sink, of the PCB.
- P_D is the power dissipation calculated in [\(EQ. 1\)](#).

4.6 PCB Thermal Management

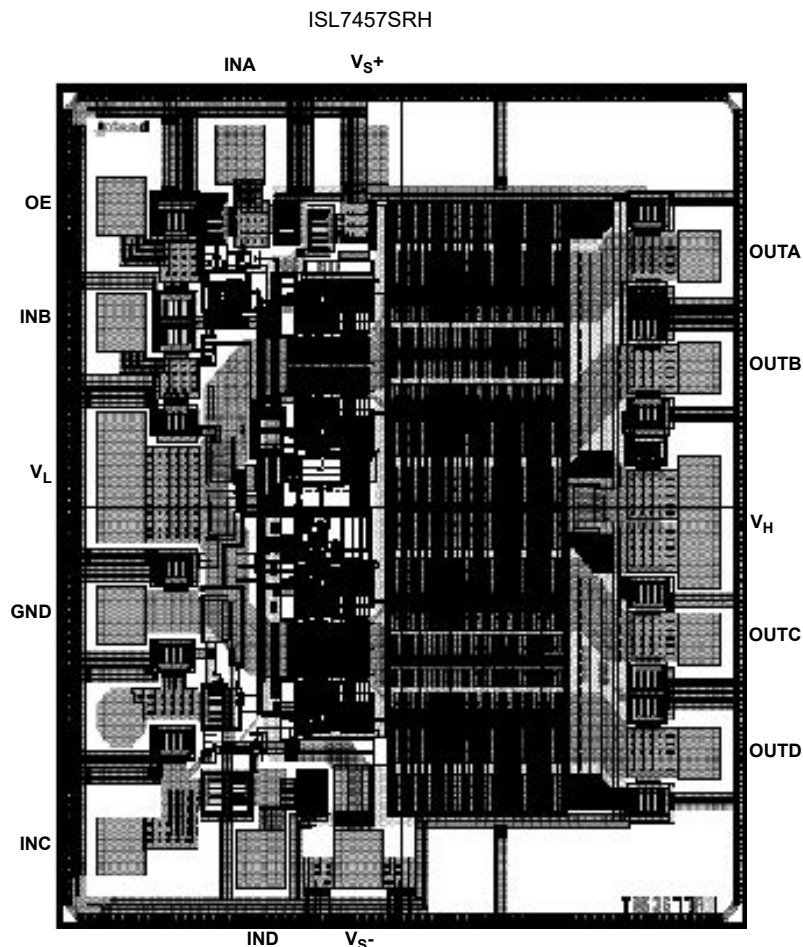
To minimize the case-to-sink thermal resistance, it is recommended that multiple vias be placed on the top layer of the PCB directly underneath the IC. The vias should be connected to the ground plane, which functions as a heatsink. A gap filler material (for example, a Sil-Pad or thermally conductive epoxy) can be used to ensure good thermal contact between the bottom of the IC and the vias.

5. Die Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	2390 μ m x 2445 μ m (94.1 mils x 96.3 mils) Thickness: 13.0 mils \pm 0.5 mil
Interface Materials	
Glassivation	Type: PSG and Silicon Nitride Thickness: 0.5 μ m \pm 0.05 μ m to 0.7 μ m \pm 0.05 μ m
Top Metallization	Type: AlCuSi (1%/0.5%) Thickness: 1.0 μ m \pm 0.1 μ m
Substrate	Type: Silicon Isolation: Junction
Backside Finish	Silicon
Assembly Information	
Substrate Potential	V_{s-}
Additional Information	
Worst Case Current Density	$< 2 \times 10^5$ A/cm ²
Transistor Count	1142

5.1 Metallization Mask Layout



5.2 Layout Characteristics

Step and Repeat: 2390 μm x 2445 μm

The DELAY pad is not bonded.

Table 3. Layout X-Y Coordinates

Pad Name	X (μm)	Y (μm)	DX (μm)	DY (μm)	Probes Per Pad
IND	675	190	140	140	1
V _{S-}	995	190	140	140	1
OUTD	2118	490	122	133	1
OUTC	2118	795	122	133	1
V _H	2118	1125	122	345	2
OUTB	2118	1554	122	133	1
OUTA	2118	1861	122	133	1
V _{S+}	1015	2140	140	140	1
INA	608	2140	140	140	1
OE	213	1993	140	140	1
INB	213	1673	140	140	1
V _L	213	1245	140	345	2
GND	213	864	140	140	1
INC	213	213	140	140	1

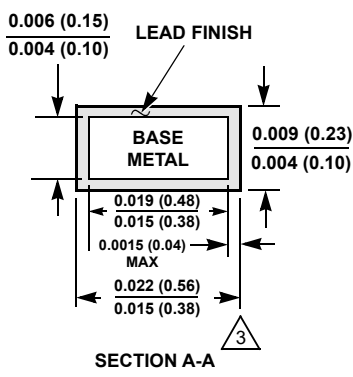
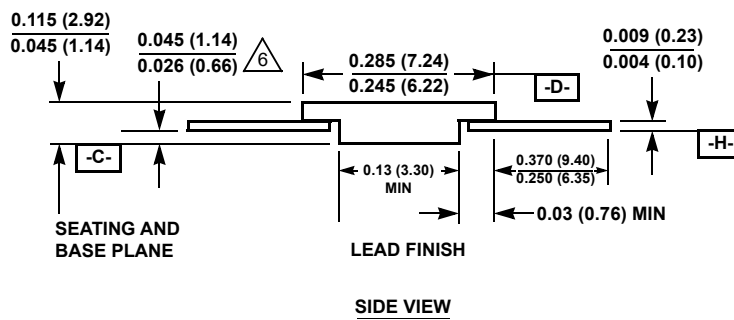
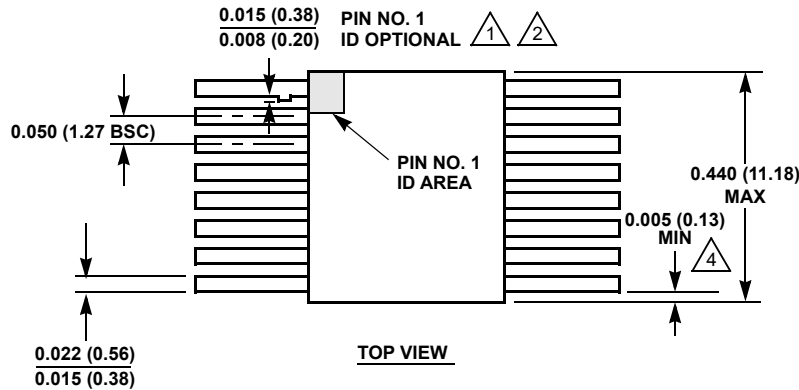
6. Revision History

Rev.	Date	Description
4.0	May 6, 2021	Updated ordering information table by reformatting, adding evaluation board, updating Note 3, and adding Notes 4 and 5. Updated links throughout. Added min/max limits to specification table. Removed About Intersil section.
3.	Jul 28, 2017	Applied new formatting. Updated Related Literature section. Added Note 3. Added Figures 12 and 13. Updated Table 3 to fix V_H and V_L Y-coordinates and remove DELAY. Added Absolute Maximum Ratings, Thermal Information, Recommended Operation Conditions, Revision History, and About Intersil sections.

7. Package Outline Drawing

For the most recent package outline drawing, see [K16.A](#).

K16.A
 16 Lead Ceramic Metal Seal Flatpack Package
 Rev 2, 1/10



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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