ISL73847SEH

Radiation Hardened Single/Dual Phase Current Mode PWM Controller

The ISL73847SEH is a synchronous buck controller that can operate as a single or dual-phase controller. It works with the ISL73041SEH (half-bridge GaN FET driver) to generate point-of-load voltage rails for commercial space applications.

Supporting an input voltage range of 4.5V to 19V, the ISL73847SEH offers a programmable PWM switching frequency from 250kHz to 1.5MHz, adjustable with a single resistor. The output voltage is configurable above 600mV, with the upper limit determined by the minimum off-time and selected switching frequency.

The ISL73847SEH features built-in current sharing, enabling two-phase operation within a single device and four-phase operation using two ISL73847SEH devices, all without requiring an external clock at ≤1.04MHz. For multi-phase operation at other frequencies, the ISL74420 provides additional scalability, making it a flexible solution for multi-phase power architectures.

Its wide input voltage range makes it ideal for high-current FPGA core power and general-purpose power applications. The current mode modulation architecture simplifies loop compensation, enhances power supply rejection, and supports remote sensing to compensate for voltage drops under load. These features deliver a high-density, robust power solution that minimizes external components while ensuring efficient and reliable performance.

The ISL73847SEH operates across the military temperature range from -55°C to +125°C and is available in a 24 Ld Ceramic Dual Flatpack (CDFP) package or die form.

Features

- Qualified to Renesas rad hard QML-V equivalent screening and QCI flow (R34TB0001EU)
  - All screening and QCI is in accordance with MIL-PRF-38535L Class-V
- Wide operating voltage range:
  - Input: 4.5V to 19V
  - Output: 0.6V to $V_{PWR_STAGE} \times ((T_{SW}-120ns)/T_{SW})$
- Programmable PWM output switching frequency
  - 250kHz to 1.5MHz
- Optional Droop regulation
- Current mode control provides
  - Excellent power supply rejection
  - Simplified control scheme
- Output differential remote sensing
- Programmable soft-start
- Enable control
- Power-good Indicator
- TID rad hard assurance (RHA) wafer-by-wafer testing
  - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE characterization
  - No DSEE with V_{DD} = 25V and 86MeV•cm^2/mg
  - SEFI <3µm^2 at 86MeV•cm^2/mg
  - SET <2% on V_{OUT} at 86MeV•cm^2/mg

Applications

- FPGA Core Power Supply
- General Purpose Power Supply

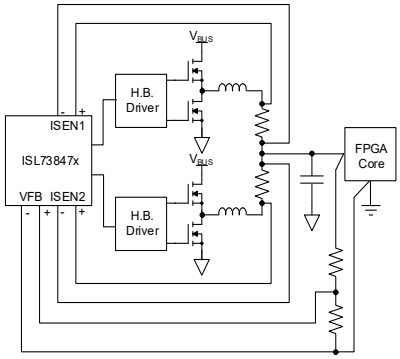

Figure 1. FPGA Core Power Supply Application

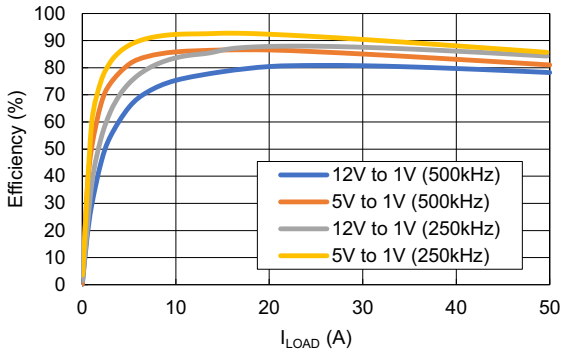

Figure 2. 12V to 1V and 5V to 1V Conversion Efficiency

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1. Overview

1.1 Typical Application Diagrams

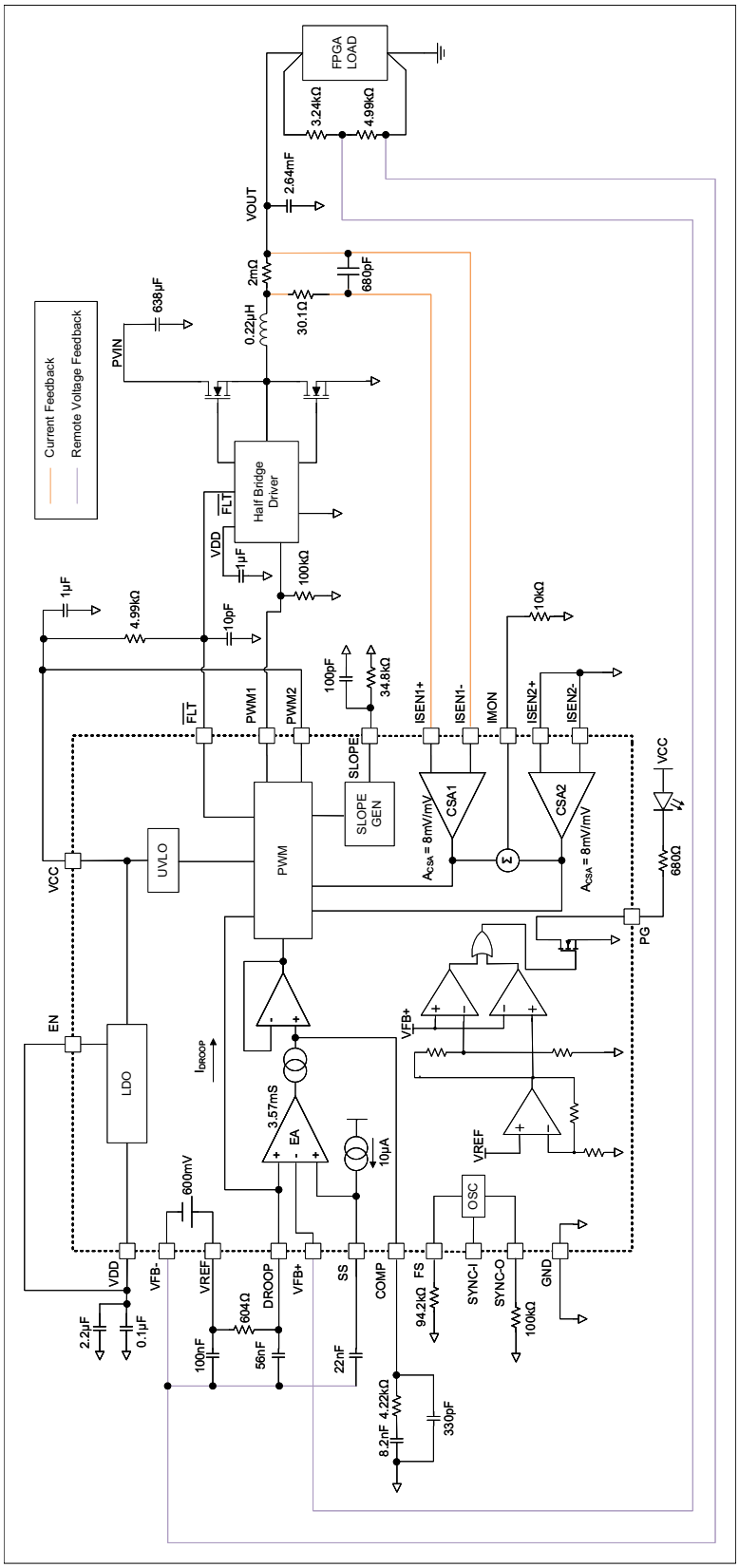


Figure 3. Typical Application (Single Phase) using One ISL73041SEH Half-Bridge Driver

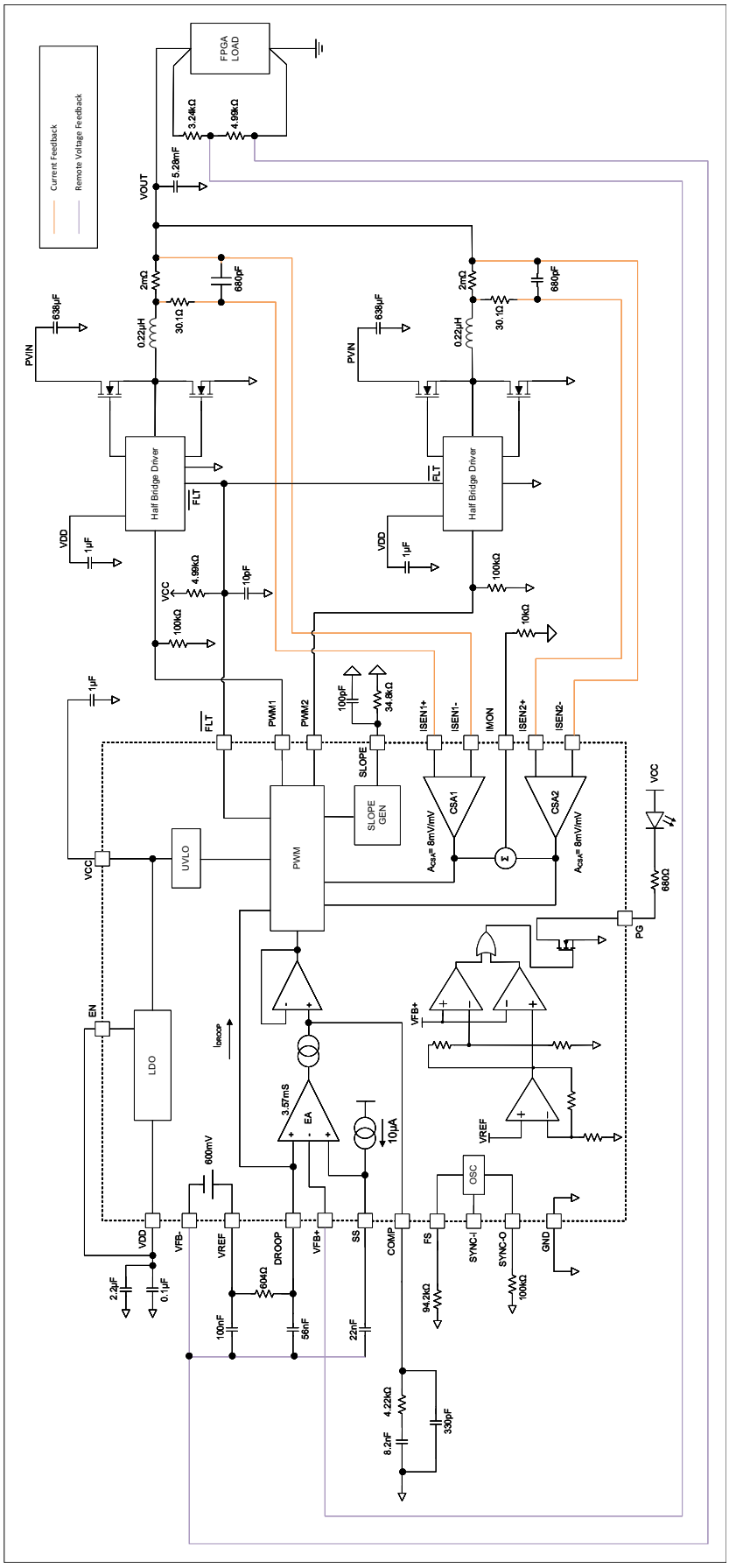


Figure 4. Typical Application (Dual-Phase) using Two ISL73041SEH Half-Bridge Drivers

1.2 Functional Block Diagram

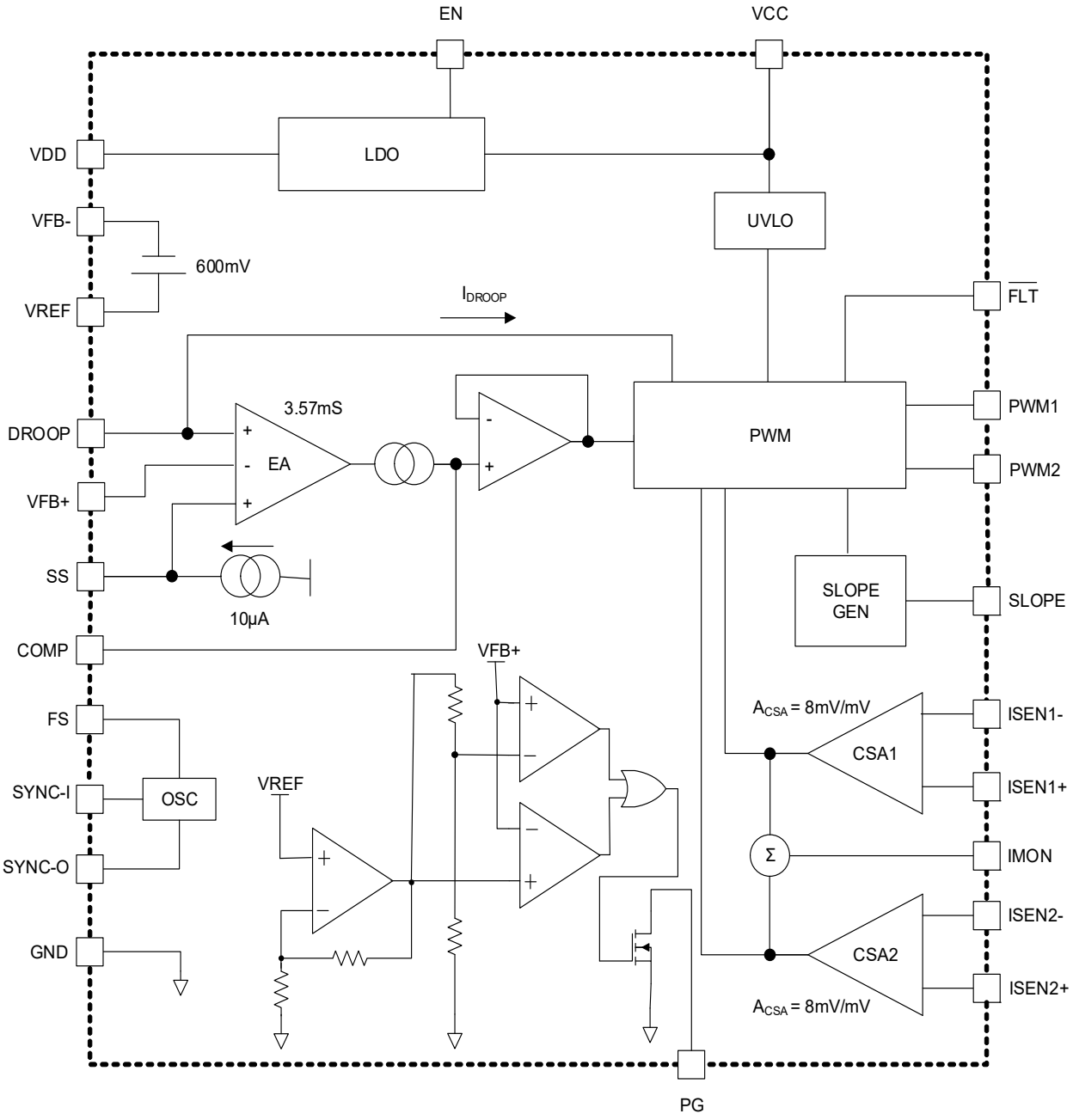


Figure 5. Block Diagram

2. Pin Information

2.1 Pin Assignments

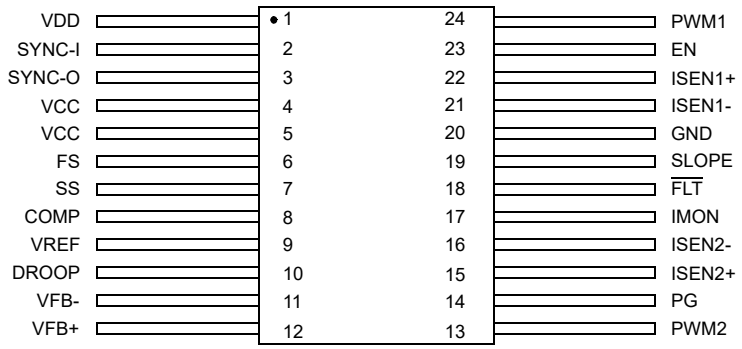


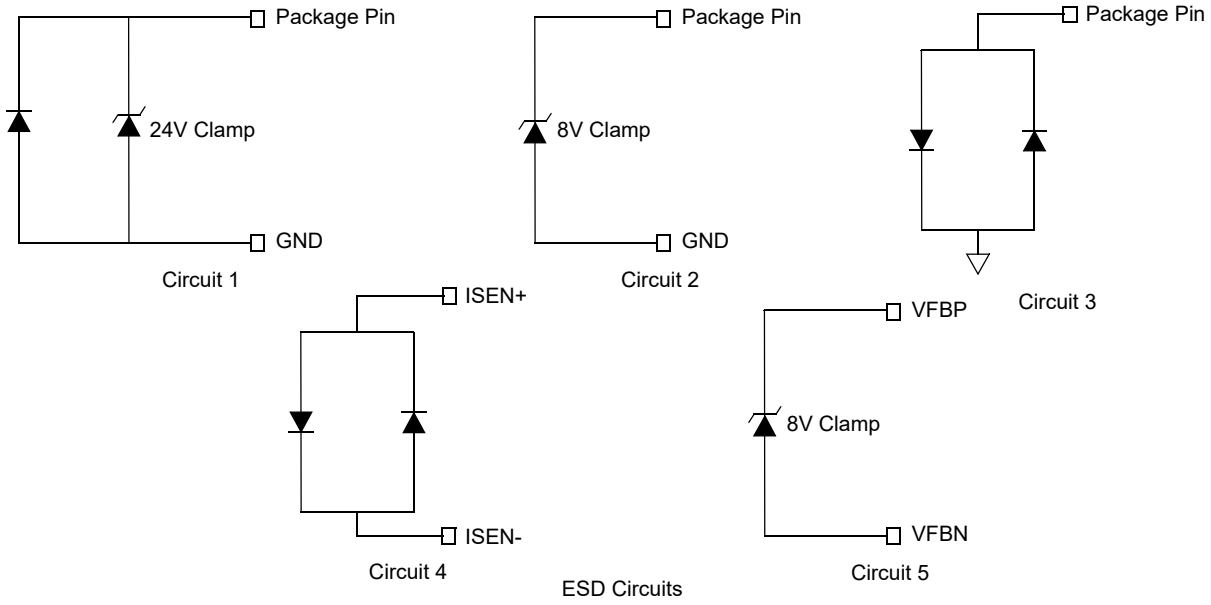
Figure 6. Pin Assignments - 24 Lead CDFP Package Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	VDD	1	The power supply input to the IC. The voltage range on this pin is 4.5V to 19V. Connect a 2.2µF or larger capacitor and a 100nF capacitor from the VDD pin to GND.
2	SYNC-I	2	This pin is an input that accepts 2x the required PWM output switching frequency (regardless of single or dual phase). Internally the IC divides the clock down to get two clocks 180° from each other for each phase. *Note:* This pin has an internal pull down, leave it floating if SYNC function is not needed.
3	SYNC-O	2	This pin can output either 1x or 2x the PWM output switching frequency depending on the loading present on the pin during power up (before soft-start). When outputting 1x, the SYNC-O is 180° out of phase with phase 1 clock. The 2x SYNC-O output is in phase with the SYNC-I. 100kΩ to VCC: SYNC-O outputs 1x PWM output switching frequency. 100kΩ to GND: SYNC-O outputs 2x PWM output switching frequency.
4, 5	VCC	2	Output of internal LDO for analog circuity. Short pins 4 and 5 together. Connect a 1µF ceramic capacitor from VCC to GND.
6	FS	2	This pin sets the frequency for the internal oscillator between 0.5MHz and 3MHz. This sets the output between 0.25 MHz and 1.5MHz for each phase. When FS is tied to VCC the internal oscillator frequency (f_{OSC}) is 1MHz. To adjust the internal oscillator frequency between 0.5MHz and 3MHz (0.25MHz to 1.5MHz PWM switching frequency), use a resistor between FS and GND. If SYNC-I is being used to sync to an external clock, FS needs to be set such that the internal oscillator frequency is 15% less than the external frequency. Use Equation 3 to find which resistor is needed for a given frequency.
7	SS	2	This is the soft-start pin. Connect a ceramic capacitor from SS to GND to set the soft-start ramp. The soft-start time is adjustable between 2ms and 200ms. Equation 24 shows the relationship between the soft-start capacitor and soft-start time.
8	COMP	2	The output of the error amplifier. Connect a resistor and capacitor in series to ground for type 2 compensation adjustment. For type-3 compensation, add an additional capacitor in parallel with the type-2 series RC components.
9	VREF	2	The output of the internal voltage reference. Insert a resistor between VREF and DROOP to enable droop regulation. Short VREF and DROOP pin together to disable droop regulation.

Pin Number	Pin Name	ESD Circuit	Description
10	DROOP	2	This pin is a current mirrored version of the output of the current sense amp output (sum of both phases). This output can be tied to the VREF pin through a resistor to enable droop regulation. The voltage created by the mirrored current and the resistor between VREF and DROOP sets the droop level.
11	VFB-	3	This pin is the negative input for differential voltage feedback.
12	VFB+	5	This pin is the positive input for differential voltage feedback.
13	PWM2	2	This pin is the PWM output for the secondary phase. This pin needs a 100kΩ to GND.
14	PG	1	This pin is the power good indicator. It is an open-drain output. Limit the sink current through this pin to below 7.2mA.
15	ISEN2+	4	This pin is the positive input for the secondary phase current sense amplifier.
16	ISEN2-	1	This pin is the negative input for the secondary phase current sense amplifier.
17	IMON	2	This pin outputs the summed average of the current sense amplifiers outputs for telemetry purposes.
18	$\overline{FLT}$	2	This pin sequences the startup between the ISL73847SEH and compatible drivers. On the ISL73847SEH, this pin operates as a bi-directional I/O during power up (before soft-start) and as an input while switching (during and after soft-start). This pin's input threshold voltage is $V_{\overline{FLT}MID}$. A logic low on this pin indicates that either the ISL73847SEH or compatible driver has encountered a fault or is not ready to start switching. A logic high indicates that there are not faults for either device. Because $\overline{FLT}$ is an open-drain output, use a 4.99kΩ typical pull-up resistor to VCC for a proper high level.
19	SLOPE	2	This pin adjusts the slope compensation of the ISL73847SEH. Place a resistor in the range of 25kΩ to 100kΩ to adjust slope compensation.
20	GND	N/A	This is the ground reference for the ISL73847SEH. This pin is tied to the package seal ring (lid).
21	ISEN1-	1	This pin is the negative input for the primary phase current sense amplifier.
22	ISEN1+	4	This pin is the positive input for the primary phase current sense amplifier.
23	EN	1	This pin is the chip enable for the ISL73847SEH.
24	PWM1	2	This pin is the PWM output for the primary phase. This pin needs a 100kΩ to GND.

Pin Number	Pin Name	ESD Circuit	Description
-	Lid	N/A	The lid is electrically connected to pin 20 (GND).



ESD Circuits

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VDD, ISENSx, EN, PG	GND - 0.3	GND + 20	V
VDD, EN, PG[1]	GND - 0.3	GND + 20	V
ISENSx[1][2]	GND - 0.3	GND + 12	V
VCC	GND - 0.3	6.5	V
VCC[1]	GND - 0.3	6.3	V
VREF, DROOP, VFBx, FS, COMP, SLOPE, $\overline{FLT}$, IMON	GND - 0.3	VCC + 0.3	V
PWMx, SYNC-I, SYNC-O	GND - 0.3	VCC + 0.3	V
Differential Voltage Across Current Sense Inputs V(ISENx+) - V(ISENx-)[3]	-0.3	+0.3	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2	kV
Charged Device Model (Tested per JS-002-2018)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

1. Tested under a heavy ion environment at LET = 86MeV•cm^2/mg at 125°C (T_C) for Single Event Burnout (SEB). See the SEE Test Report for more details.
2. No SEFI seen ≤10V at LET 86MeV•cm^2/mg.
3. Maximum current through anti-parallel diodes should be ≤10mA.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VDD, EN, PG	GND + 4.5	GND + 19.0	V
ISENx Common Mode Range	GND - 0.3	19	V
Differential Voltage Across Current Sense Inputs V(ISENx+) - V(ISENx-)	-75	100	mV
PWM Output Switching Frequency	0.25	1.5	MHz
Regulated Output Voltage	0.6	PVIN×((T_{SW}-120ns)/T_{SW})	V
Ambient Temperature	-55	125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	24 Lead CDFP Package	θ_{JA}[1]	Junction to ambient.	23	°C/W
		θ_{JC}[2]	Junction to case.	1.7	

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board (two buried 1 oz copper planes) using direct attach features with package base mounted to PCB thermal land (with thermal vias below) with Epoxy (10 mils thick with a k of 1W/m-K). See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

3.4 Electrical Specifications

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Input Power Supply							
Supply Voltage Range	V_{DD}	-	-55 to +125°C	**4.5**	-	**19**	V
Rising V_{DD} UVLO	$VDD_{UV(R)}$	EN = V_{DD}		**4.05**	4.2	**4.4**	V
Falling V_{DD} UVLO	$VDD_{UV(F)}$	EN = V_{DD}		**3.85**	4.0	**4.1**	V
V_{DD} UVLO Hysteresis	$VDD_{UV(HYS)}$	EN = V_{DD}		**150**	220	**300**	mV
Operating Supply Current	I_{DDO}	V_{DD} = 4.5V, 12V, 19V EN = 3.3V, f_{SW} = 500kHz, C_L=100pF		**9**	12	**16**	mA
Shutdown Supply Current	I_{DDSD}	V_{DD} = 4.5V, 12V, 19V EN = GND		-	11	**35**	µA
Internal LDO							
Output Range	VCC	V_{DD} = 6.0V, 19V I_{OUT} = 0mA, 20mA	-55 to +125°C	**4.7**	5.0	**5.3**	V
Dropout Voltage	VCC_{DO}	V_{DD} = 4.5V, I_{OUT} = 50mA		**85**	160	**250**	mV
Rising V_{CC} UVLO	$VCC_{UV(R)}$	EN = V_{DD}		**3.4**	3.6	**3.7**	V
Falling V_{CC} UVLO	$VCC_{UV(F)}$	EN = V_{DD}		**3.2**	3.3	**3.5**	V
V_{CC} UVLO Hysteresis	$VCC_{UV(HYS)}$	EN = V_{DD}		**150**	210	**300**	mV
V_{CC} Foldback Current	I_{CC-SC}	V_{DD} = 19V, V_{CC} = 0V, EN = 1.6V		**40**	72	**90**	mA
V_{CC} Overcurrent Limit	I_{CC-CL}	V_{DD} = 19V, V_{CC} = 4.3V, EN = 1.6V		**75**	98	**130**	mA
Output Regulation							
Set Point Voltage[2]	V_{FB+}	V_{REF} = V_{DROOP} V_{SEN1} = V_{SEN2} = 0mV, 50mV	-55°C	0.596	0.597	0.601	V
			+25°C	0.599	0.600	0.603	V
			+125°C	0.597	0.600	0.604	V
			+25°C (Post Rad)	0.597	0.600	0.604	V

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Set Point Accuracy Over Line Delta[2][3]	V_{FB+}	$V_{REF} = V_{DROOP}$ VSEN1 = VSEN2 = 0mV	-55 to +125°C	**-1**	0.2	**0.6**	mV
Set Point Accuracy Over Load Delta[2][3]	V_{FB+}	$V_{REF} = V_{DROOP}$ $V_{SEN1} = V_{SEN2}$ = 0mV, 50mV		**-0.75**	0.05	**0.75**	mV
FB+ Input Bias Current	$I_{FB+BIAS}$	V(FB+) = 0.6V		**-50**	-0.25	**50**	nA
FB- Input Bias Current	$I_{FB-BIAS}$	V(FB-) = 0V, EN>$V_{IH-EN-G}$ $V_{SEN1} = V_{SEN2}$ = 0mV		**30**	121	**350**	µA
Soft-Start Sourcing Current	$I_{SOFTSTART}$	-		**9.2**	10	**10.5**	µA
Soft-Start Pull-Down Resistance	$R_{SS-PULLDN}$	EN = 0V		**4**	11	**18**	Ω
Protection Features							
Peak Positive Current Limit Threshold	V_{PCL}	V_{CM} = 0.6V, 5.0V, 19V	-55 to +125°C	**67.5**	75	**82.5**	mV
Peak Positive Overcurrent Threshold	V_{POC}	V_{CM} = 0.6V, 5.0V, 19V		**90**	100	**110**	mV
Peak Negative Overcurrent Threshold	V_{NOC}	V_{CM} = 0.6V, 5.0V, 19V		**-84**	-71	**-60**	mV
Overvoltage Threshold	$V_{(FB, OV)}$	V_{DD} = 4.5V and 19V		**112**	115	**118**	%
Undervoltage Threshold	$V_{(FB, UV)}$	V_{DD} = 4.5V and 19V		**82**	85	**88**	%
$\overline{FLT}$ Drive current	$I_{\overline{FLT}}$	V_{DD} = 4.5V and 19V, $\overline{FLT}$ = 400mV		**20**	50	**75**	mA
$\overline{FLT}$ Mid Threshold Voltage	$V_{\overline{FLT}MID}$	V_{DD} = 4.5V and 19V		**1.6**	2.08	**2.55**	V
$\overline{FLT}$ Leakage Current	$I_{\overline{FLT}LKG}$	$\overline{FLT}$ = 4.5V when V_{DD} = 4.5V $\overline{FLT}$ = 5V when V_{DD} = 19V		**-2**	0.07	**2**	µA
Error Amplifier							
Transconductance	g_{m-EA}	-	-55°C	3	4.1	4.5	mA/V
			+25°C	3	3.57	4	mA/V
			+125°C	2.5	3.04	3.5	mA/V
			+25°C (Post Rad)	3	3.6	4	mA/V
DC Gain[4]	A_{V-EA}	-	-55 to +125°C	66	80	-	dB
Gain-Bandwidth Product[4]	GBW_{EA}	-		15	-	-	MHz
Output Voltage Range	$V_{COMP(RNG)}$	V_{DD} = 4.5V		**0.4**	-	**4.1**	V
		V_{DD} = 19V		**0.4**	-	**4.6**	
Output Slew Rate[4]	SR_{EA}			-	8.5	-	V/µs

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Current-Sense Amplifier							
Droop Transconductance	$g_{m(CSA, DRP)}$	$V(I_{SEN+}, I_{SEN-})$ = 10mV, 50mV V_{CM} = 0.6V, 5.0V, 19V	-55°C	0.38	0.4	0.42	µA/mV
			+25°C	0.38	0.4	0.42	µA/mV
			+125°C	0.375	0.39	0.41	µA/mV
			+25°C (Post Rad)	0.38	0.4	0.42	µA/mV
Droop Current	$Error_{DRP}$	$V(I_{SEN+}, I_{SEN-})$ = 50mV, V_{CM} = 0.6V, 5.0V, 19V	-55°C	16	18.7	23.5	µA
			+25°C	18.2	19.9	21.8	µA
			+125°C	17.5	20.5	23.5	µA
			+25°C (Post Rad)	16	19.7	23.5	µA
IMON Transconductance	$g_{m(CSA, IMON)}$	$V(I_{SEN+}, I_{SEN-})$ = 10mV, 50mV V_{CM} = 0.6V, 5.0V, 19V	-55 to +125°C	**0.36**	0.39	**0.47**	µA/mV
Gain from CSA input to PWM Comparator input	$A_{CSA-PWM}$	$V(I_{SEN+}, I_{SEN-})$ = 50mV		**7.5**	8	**8.5**	mV/mV
Offset Voltage	$V_{OS(CSA)}$	$V(I_{SEN+} - I_{SEN-})$ = 0mV V_{CM} = 0.6V, 5.0V, 19V	-55°C	-4.5	-0.2	4.5	mV
			+25°C	-2	-0.05	2	mV
			+125°C	-4.5	0.15	4.5	mV
			+25°C (Post Rad)	-4.5	-0.13	4.5	mV
Positive Input Leakage Current	$I_{LKG+(CSA)}$	EN = 0V, V_{CM} = 0.6V, 5.0V, 19V	-55 to +125°C	**-50**	4	**50**	nA
Negative Input Leakage Current	$I_{LKG-(CSA)}$	EN = 0V, V_{CM} = 0.6V		-	1.55	**200**	nA
		EN = 0V, V_{CM} = 5.0V, 19V		-	0.325	**1.0**	µA
HS CSA Supply Current per Phase (Current into ISENx- pin)	I_{CSA}	EN = 3.3V, V_{CM} = 2.7V		-	2	**3**	µA
Transition from Low Side to High Side	$V_{CS(TRAN)}$	V_{DD} = 4.5V		**1.95**	2.13	**2.35**	V
Transition from Low Side to High Side	$V_{CS(TRAN)}$	V_{DD} = 19V		**2.25**	2.37	**2.5**	V
Gain-Bandwidth Product[4]	GBW_{CSA}	-		**10**	-	-	MHz

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Oscillator/Slope Generator							
Default Oscillator Frequency	f_{OSC-D}	FS = V_{CC}, V_{DD} = 4.5V, 19V	-55 to +125°C	**0.90**	1.00	**1.10**	MHz
Oscillator Frequency Range	$f_{OSC-0.5M}$	R_{FS} = 205kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**0.45**	0.5	**0.55**	MHz
	f_{OSC-1M}	R_{FS} = 94.2kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**0.90**	1.00	**1.10**	MHz
	f_{OSC-2M}	R_{FS} = 37kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**1.80**	2.00	**2.20**	MHz
	f_{OSC-3M}	R_{FS} = 16.7kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**2.70**	3.00	**3.30**	MHz
Slope Pin Current	I_{SLOPE}	V_{SLOPE} = 400mV, V_{DD} = 4.5V, 19V		**11.2**	12	**12.6**	µA
Default Slope Compensation Reference Voltage	V_{SLOPE_DFLT}	-	-55 to +125°C	**1.14**	1.2	**1.26**	V
Ramp Slope	$V_{RAMP-SLOPE}$	f_{SW} = 500kHz, V_{SLOPE} = 0.4V	-55 to +125°C	**0.065**	0.098	**0.150**	V/µs
Enable							
Rising Enable Threshold (Gross)	$V_{IH-EN-G}$	FS = V_{CC}	-55 to +125°C	**0.9**	1.3	**1.6**	V
Falling Enable Threshold (Gross)	$V_{IL-EN-G}$	FS = V_{CC}		**0.6**	1.0	**1.2**	V
Enable Threshold Hysteresis (Gross)	$V_{HYS-EN-G}$	FS = V_{CC}		**200**	350	**500**	mV
Rising Enable Threshold (Fine)	$V_{IH-EN-F}$	FS = V_{CC}		**1.74**	1.8	**1.85**	V
Falling Enable Threshold (Fine)	$V_{IL-EN-F}$	FS = V_{CC}		**1.46**	1.5	**1.54**	V
Enable Threshold Hysteresis (Fine)	$V_{HYS-EN-F}$	FS = V_{CC}		**260**	295	**320**	mV
EN Rising to Boot Refresh Delay	t_{EN}	FS = V_{CC}		**1.9**	2.3	**2.8**	ms
Pull Down Resistance	R_{EN}	EN = 19V		-	1	-	MΩ
EN Leakage	EN_{LK}	V_{DD} = EN = 19V		**20**	120	**250**	nA

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Power-Good							
Overvoltage Error Threshold	V_{OVH}	EN = 3.3V, FB as a percent of V_{REF}	-55 to +125°C	**106**	108	**110**	%
Overvoltage Error Threshold Recovery	V_{OVL}	EN = 3.3V, FB as a percent of V_{REF}		**104**	106	**109**	%
Overvoltage Error Hysteresis	V_{OVH}	EN = 3.3V, FB as a percent of V_{REF}		**1.2**	2	**3.0**	%
Undervoltage Error Threshold	V_{UVL}	EN = 3.3V, FB as a percent of V_{REF}		**90**	92	**94**	%
Undervoltage Error Threshold Recovery	V_{UVH}	EN = 3.3V, FB as a percent of V_{REF}		**92**	94	**96**	%
Undervoltage Error Hysteresis	V_{UVH}	EN = 3.3V, FB as a percent of V_{REF}		**1.2**	2.05	**3.0**	%
Sink Current	$I_{PG-SINK}$	V_{DD} = 4.5V, V(FB+, FB-) = V_{PG} = 0.4V EN = 0V		**5**	18	**35**	mA
PG Leakage	I_{PG-LKG}	V_{DD} = 4.5V, V(FB+, FB-) = 0.6V, V_{PG} = 19V EN = 0V	-55 to +125°C	-	0.02	**0.5**	µA
SS Voltage for PG to be Active After Power-Up	V_{SS-PG}	V(SS) = 0V to 1V.		**0.82**	0.9	**0.98**	V
PG Reaction Time to OV Fault	$t_{PG-PROP-OV}$	V(FB+, FB-) = 0.6V to 0.7V		**12**	14.5	**18**	µs
PG Reaction time to UV Fault	$t_{PG-PROP-UV}$	V(FB+, FB-) = 0.6V to 0.5V		**12**	14.6	**18**	µs
Hiccup Retry Delay	$t_{HIC-DLY}$	C_{SS} = 10nF		**2**	2.7	**4**	ms

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
PWM Outputs							
PWM Output High	V_{OH}	V_{DD} = 4.5V, I_{PWM} = -500µA	-55 to +125°C	**4.0**	-	-	V
		V_{DD} = 19V, I_{PWM} = -500µA		**4.5**	-	-	
PWM Output Mid	V_{OZ}	I_{PWM} = ±100µA		**1.8**	2.0	**2.3**	V
PWM Output Low	V_{OL}	I_{PWM} = +500µA			0.05	**0.4**	V
Turn-On Blanking Time	$t_{MINONBLK}$	-		**90**	99	**115**	ns
Turn-Off Blanking Time	$t_{MINOFFBLK}$	-		**100**	112	**130**	ns
Minimum Controllable ON-Time	$t_{MINCTRLON}$	-		**100**	115	**135**	ns
Minimum Controllable OFF-Time	$t_{MINCTRLOFF}$	-		**100**	116	**135**	ns
Passive Pull-Down	$R_{PWM-PLDN}$	-		-	5	-	MΩ
Current Share between Phase 1 & 2[4]	$I_{PHSHARE}$	V_{CM} = 1V, 5V		**-4**	0	**4**	mV
Boot Refresh Repeat Timer	t_{BOOT}	-		**62**	68	**75**	µs
SYNC							
SYNC-I Input Voltage High	V_{SYNCH}	-	-55 to +125°C	**1.7**	-	-	V
SYNC-I Input Voltage Low	V_{SYNCL}	-		-	-	**0.8**	V
SYNC-I Frequency (Referred to Internal Oscillator)	f_{SYNCI}	FOSC = 500kHz, R_{FS} = 205kΩ		**15**	-	-	%
SYNC-I Frequency (Referred to Internal Oscillator)	f_{SYNCI}	FOSC = 2MHz, R_{FS} = 37kΩ		**15**	-	-	%
SYNC-I Input Current	$I_{SYNC-IN}$	V_{SYNC} = 5V		**2.5**	5	**7.0**	µA
SYNC-I Pull-Down Resistance	$R_{SYNC-PULLDN}$	V_{SYNC} = 5V		-	1	-	MΩ
SYNC-O Output Voltage High	$V_{SYNC-OH}$	V_{DD} = 4.5V, I_{SYNC-O} = -500µA		**4.2**	-	-	V
		V_{DD} = 19V, I_{SYNC-O} = -500µA		**4.6**	-	-	
SYNC-O Output Voltage Low	$V_{SYNC-OL}$	I_{SYNC-O} = +500µA		-	-	**0.4**	V
SYNC-I to PWM2 Delay	$t_{SYNC-I-DEL}$	-		-	260	-	ns
SYNC-O to PWM2 Delay	$t_{SYNC-O-DEL}$	-		-	20	-	ns
SYNC-I to SYNC-O Delay	$t_{SYNC-DLY}$	50% of SYNC-I to 50% of SYNC-O		**215**	240	**275**	ns

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
SYNC-O to PWM1 Phase Shift	$t_{SYNCO-PWM1}$	Phase shift from PWM1	-55 to +125°C	**178**	180	**184**	°
PWM1 to PWM2 Phase Shift	$t_{PWM1-PWM2}$	Phase shift from PWM1 to PWM2		**174**	180	**186**	°

1. Typical values are at 25°C and are not guaranteed.
2. This test is conducted in a closed loop circuit as shown in Figure 7 and includes the error amplifier offset.
3. This specification is included within the Set Point Voltage specification.
4. Limits established by characterization and/or design analysis and are not production tested.

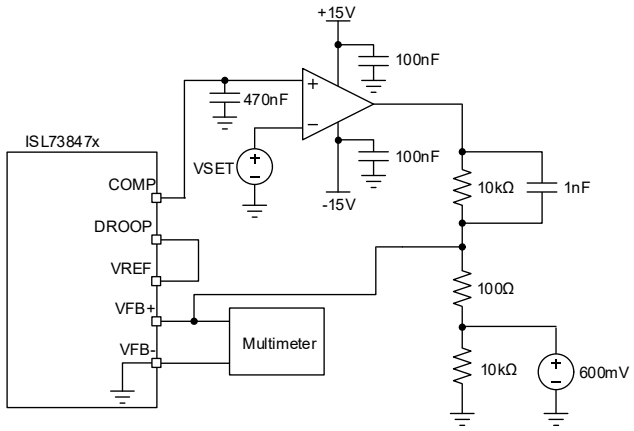


Figure 7. Closed-Loop Circuit

Table 1. Burn-in and Operating Life Test Delta Parameters

Parameters	Symbol	Conditions	Delta Limits		Limit
			Min	Max	
Shutdown Current 19V	I_{DDSD}	V_{DD} = 19V, EN = GND	-1.5	1.5	µA
Operating Current 19V	I_{DDO}	V_{DD} = 19V	-0.75	0.75	mA
EN Leakage 19V	EN_{LK}	V_{DD} = 19V	-12	12	nA
PG Drive Current 19V	$I_{PG-SINK}$	V_{DD} = 19V	-1.6	1.6	mA
SS Charging I 19V	$I_{SOFTSTART}$	V_{DD} = 19V	-0.5	0.5	µA
SS Charging I 4.5V	$I_{SOFTSTART}$	V_{DD} = 4.5V	-0.5	0.5	µA
ISEN1-I Leak 19V 19V	$I_{LKG-(CSA1)}$	V_{DD} = 19V, V_{CM} = 19V	-0.07	0.07	µA
ISEN2-I Leak 19V 19V	$I_{LKG-(CSA2)}$	V_{DD} = 19V, V_{CM} = 19V	-0.07	0.07	µA
CSA1DROOPI2 0.6V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 0.6V	-1.1	1.1	µA
CSA1DROOPI2 5V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 5V	-1.1	1.1	µA
CSA2DROOPI2 0.6V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 0.6V	-1.1	1.1	µA
CSA2DROOPI2 5V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 5V	-1.1	1.1	µA
PWM1MidSink 19V	V_{OZ1+}	V_{DD} = 19V, I_{PWM1} = +100µA	-0.2	0.2	V

Table 1. Burn-in and Operating Life Test Delta Parameters (Cont.)

Parameters	Symbol	Conditions	Delta Limits		Limit
			Min	Max	
PWM2MidSink 19V	V_{OZ2+}	V_{DD} = 19V, I_{PWM2} = +100µA	-0.2	0.2	V
PWM1MidSource 19V	V_{OZ1-}	V_{DD} = 19V, I_{PWM1} = -100µA	-0.2	0.2	V
PWM2MidSource 19V	V_{OZ2-}	V_{DD} = 19V, I_{PWM2} = -100µA	-0.2	0.2	V
PWM1Vol 19V	V_{OL1+}	V_{DD} = 19V, I_{PWM1} = +500µA	-10	10	mV
PWM2Vol 19V	V_{OL2+}	V_{DD} = 19V, I_{PWM2} = +500µA	-10	10	mV
PWM1Voh 19V	V_{OH1-}	V_{DD} = 19V, I_{PWM1} = -500µA	-0.23	0.23	V
PWM2Voh 19V	V_{OH2-}	V_{DD} = 19V, I_{PWM2} = -500µA	-0.23	0.23	V
OscFS0.5M 19V	$f_{OSC-0.5M}$	V_{DD} = 19V, f_{OSC} = 500kHz	-0.025	0.025	MHz
OscFS3M 19V	f_{OSC-3M}	V_{DD} = 19V, f_{OSC} = 3MHz	-0.16	0.16	MHz
SYNC-I Input Current 19V	$I_{SYNCI-IN}$	V_{DD} = 19V, V_{SYNC} = 5V	-0.32	0.32	µA
SYNC-O Vol 19V	$V_{SYNC-OL}$	V_{DD} = 19V, I_{SYNC-O} = +500µA	-10	10	mV
SYNC-O Voh 19V	$V_{SYNC-OH}$	V_{DD} = 19V, I_{SYNC-O} = -500µA	-0.23	0.23	V

4. Typical Performance Curves

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C

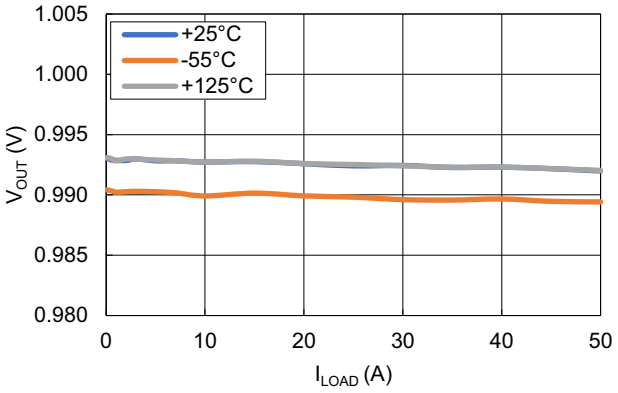


Figure 8. Load Regulation for Various Temperatures (P_{VIN} = V_{DD} = 5V)

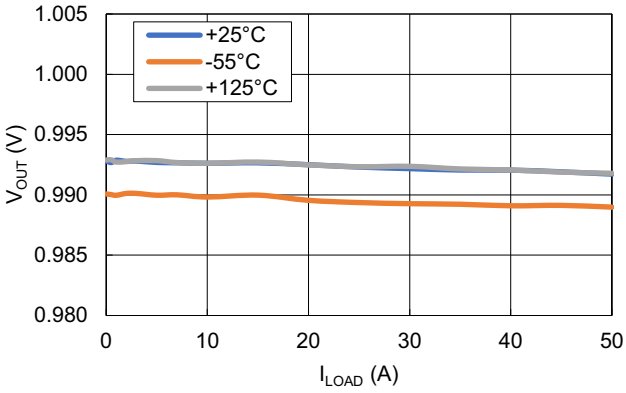


Figure 9. Load Regulation for Various Temperatures (P_{VIN} = V_{DD} = 12V)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

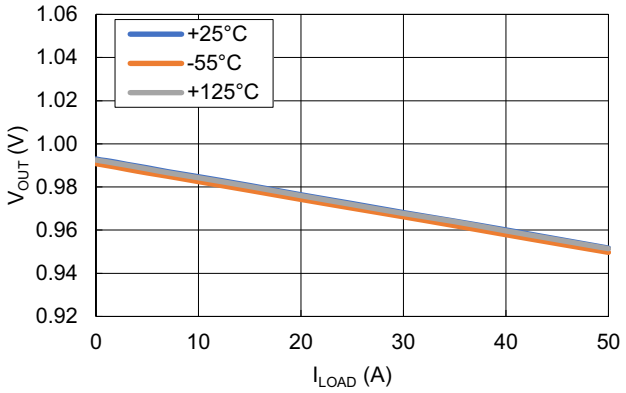


Figure 10. Droop Regulation for Various Temperatures (P_{VIN} = V_{DD}= 5V, R_{DROOP} = 604Ω)

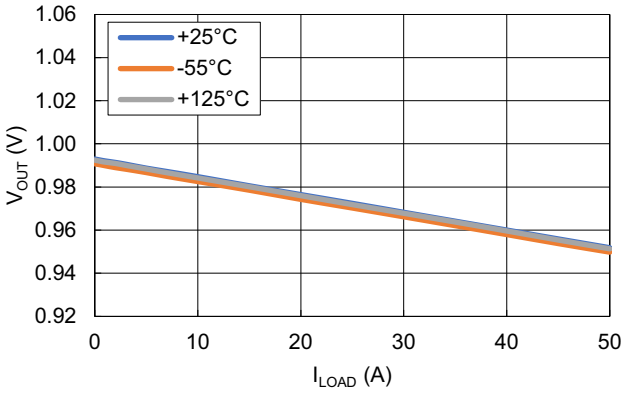


Figure 11. Droop Regulation for Various Temperatures (P_{VIN} = V_{DD} = 12V, R_{DROOP} = 604Ω)

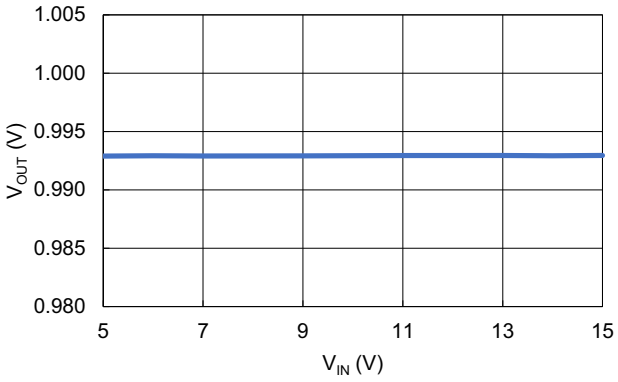


Figure 12. Line Regulation for Various Temperatures (I_{LOAD} = 0A)

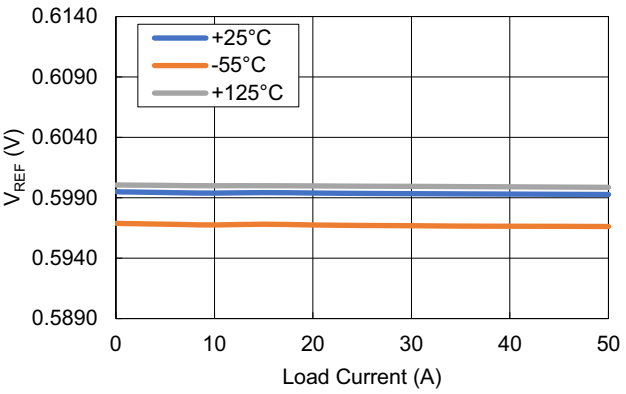


Figure 13. V_{REF} Accuracy for Various Temperatures (P_{VIN} = V_{DD} = 5V)

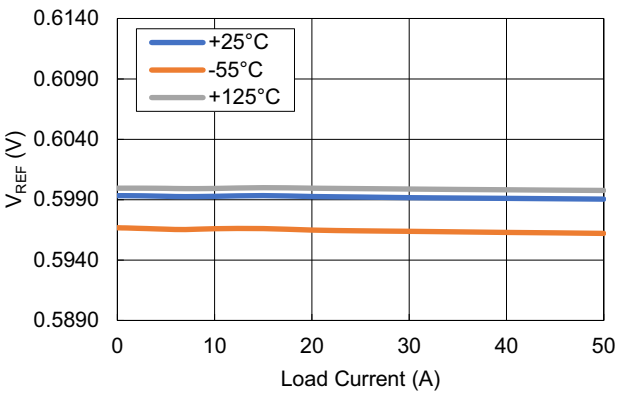


Figure 14. V_{REF} Accuracy for Various Temperatures (P_{VIN} = V_{DD} = 12V)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

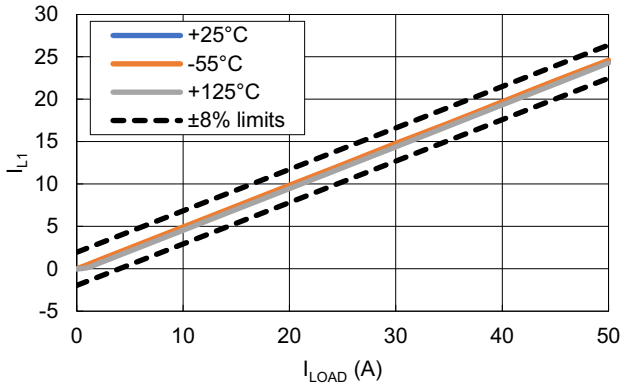


Figure 15. Phase 1 Current Share vs Temperature (P_{VIN} = V_{DD} = 5V)

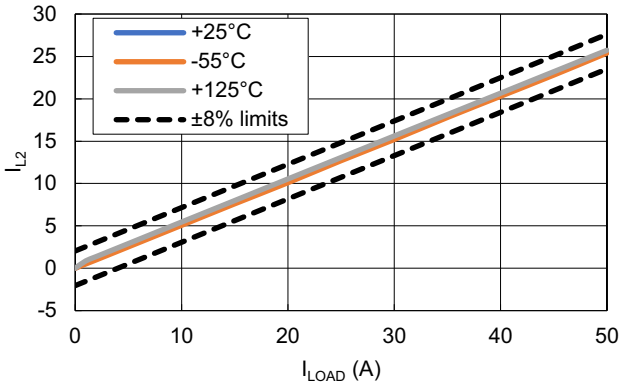


Figure 16. Phase 2 Current Share vs Temperature (P_{VIN} = V_{DD} = 5V)

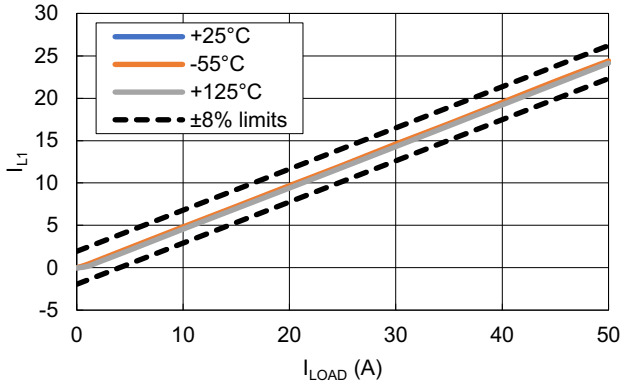


Figure 17. Phase 1 Current Share vs Temperature (P_{VIN} = V_{DD} = 12V)

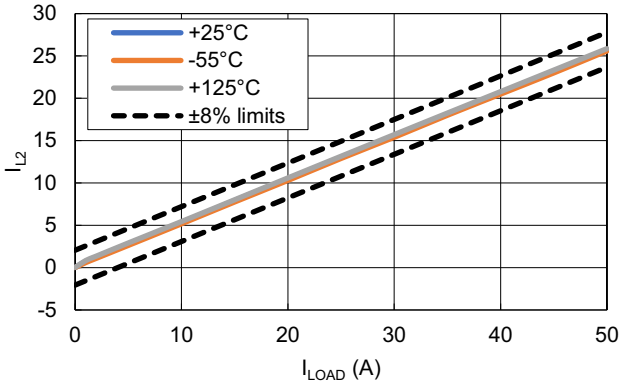


Figure 18. Phase 2 Current Share vs Temperature (P_{VIN} = V_{DD} = 12V)

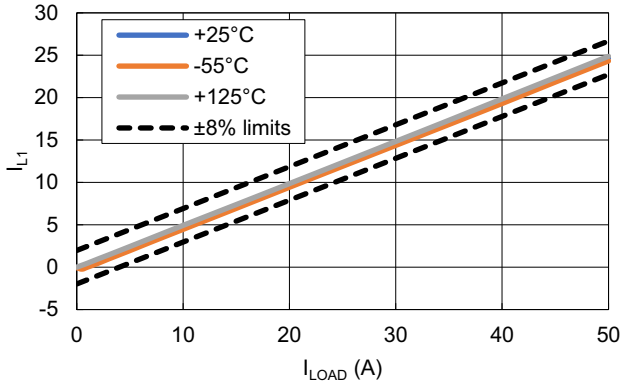


Figure 19. Phase 1 Current Share vs Temperature (P_{VIN} = V_{DD} = 12V, V_{OUT} = 5V)

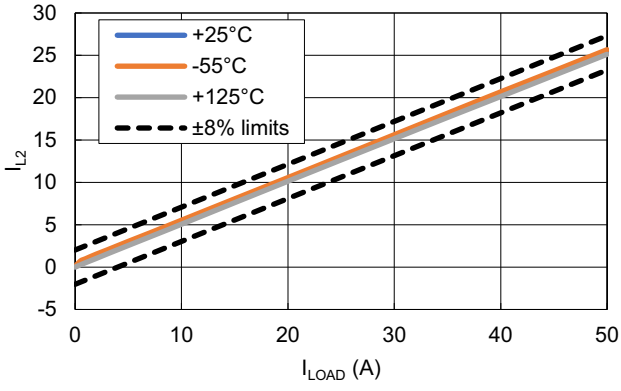


Figure 20. Phase 2 Current Share vs Temperature (P_{VIN} = V_{DD} = 12V, V_{OUT} = 5V)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

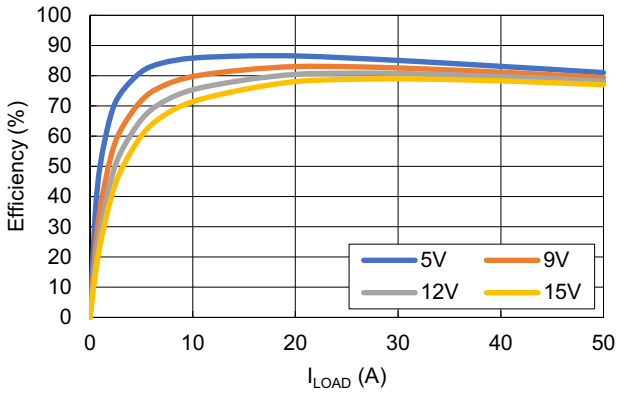


Figure 21. Conversion Efficiency for Various V_{IN} (f_{SW} = 500kHz, Tested on the ISL73847SEHEV2Z)

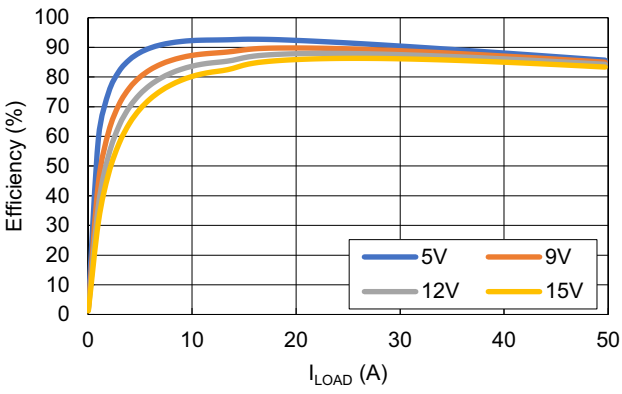


Figure 22. Conversion Efficiency for Various V_{IN} (f_{SW} = 250kHz, Tested on the ISL73847SEHEV2Z), L_{OUT} = 450nH per phase, C_{OUT} = 5.28mF per phase, C_{COMP} = 15nF, C_{DROOP} = 100nF, R_{FS} = 205kΩ

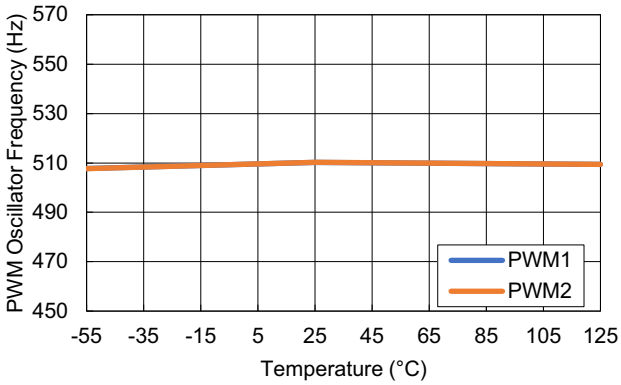


Figure 23. PWMx Frequency vs Temperature (P_{VIN} = V_{DD} = 12V, I_{LOAD} = 0A)

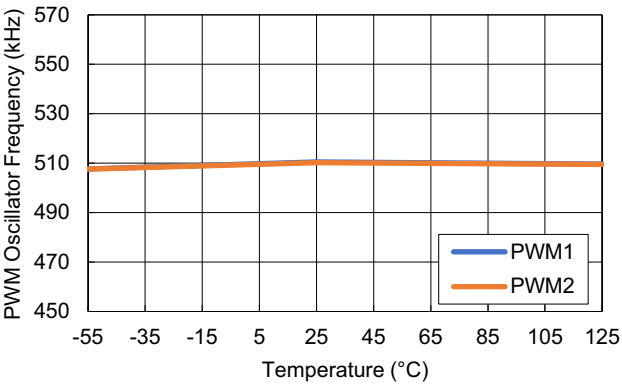


Figure 24. PWMx Frequency vs Temperature (P_{VIN} = V_{DD} = 12V, I_{LOAD} = 50A)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

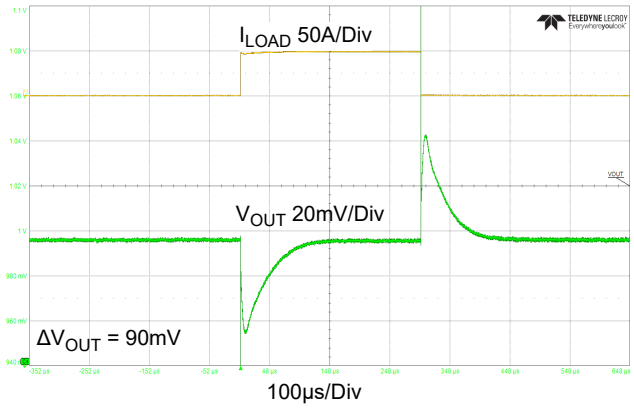


Figure 25. Load Transient Response (P_{VIN} = V_{DD} = 5V)

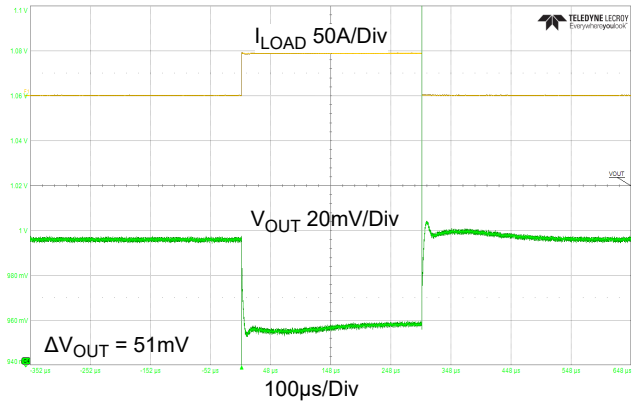


Figure 26. Load Transient Response (P_{VIN} = V_{DD} = 5V, R_{DROOP} = 604Ω)

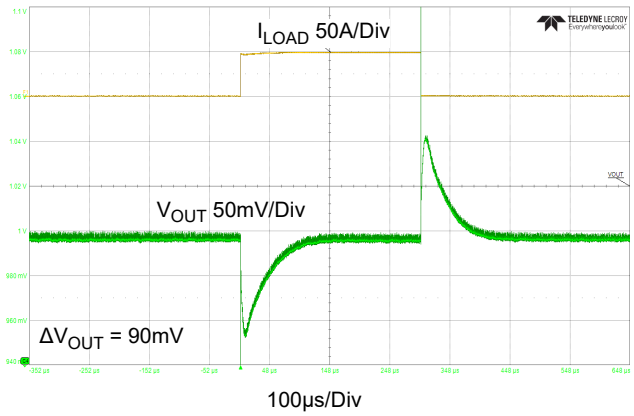


Figure 27. Load Transient Response (P_{VIN} = V_{DD} = 12V)

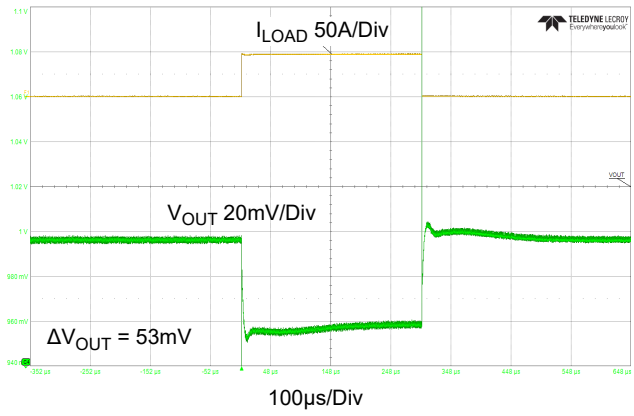


Figure 28. Load Transient Response (P_{VIN} = V_{DD} = 12V, R_{DROOP} = 604Ω)

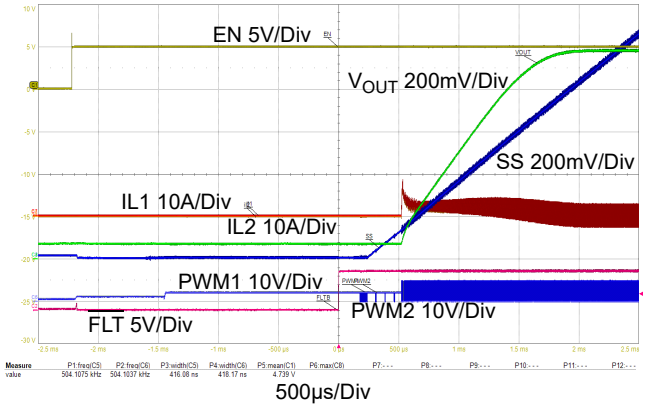


Figure 29. Start-Up with EN (P_{VIN} = V_{DD} = 4.62V, I_{LOAD} = 0A)

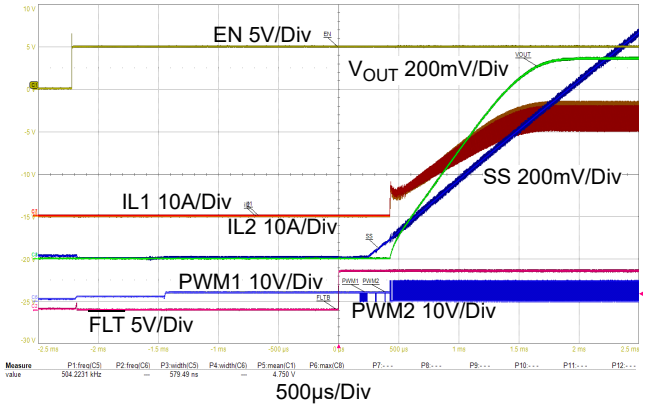


Figure 30. Start-Up with EN (P_{VIN} = V_{DD} = 4.62V, I_{LOAD} = 50A)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

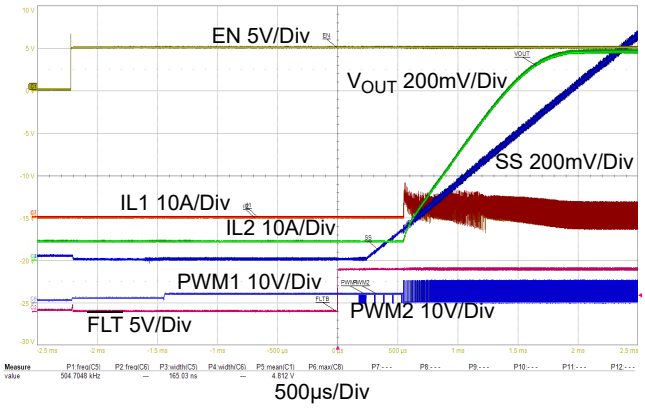


Figure 31. Start-Up with EN (P_{VIN} = V_{DD} = 12V, I_{LOAD} = 0A)

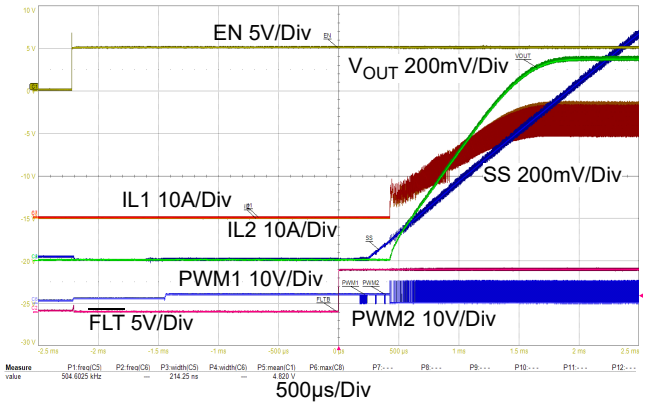


Figure 32. Start-Up with EN (P_{VIN} = V_{DD} = 12V, I_{LOAD} = 50A)

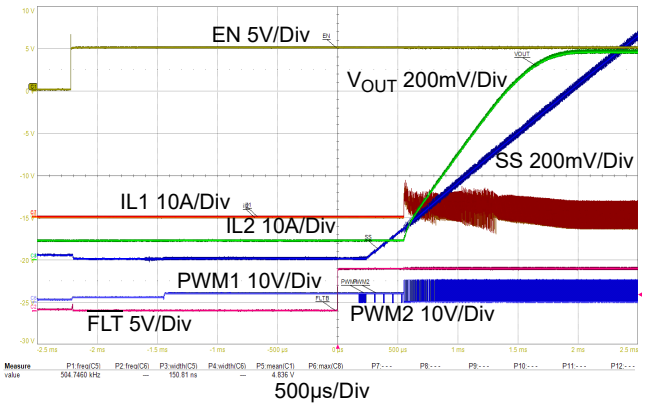


Figure 33. Start-Up with EN (P_{VIN} = V_{DD} = 13.2V, I_{LOAD} = 0A)

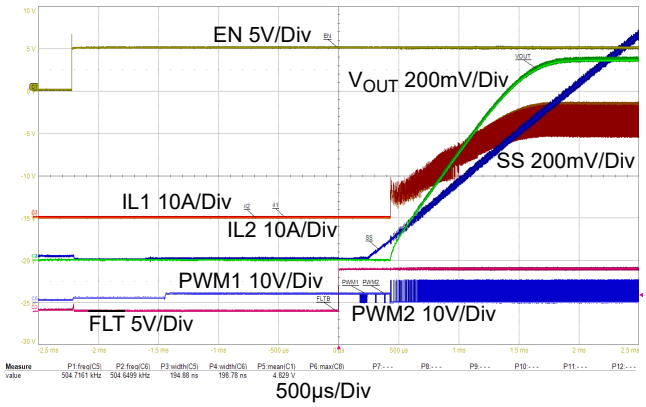


Figure 34. Start-Up with EN (P_{VIN} = V_{DD} = 13.2V, I_{LOAD} = 50A)

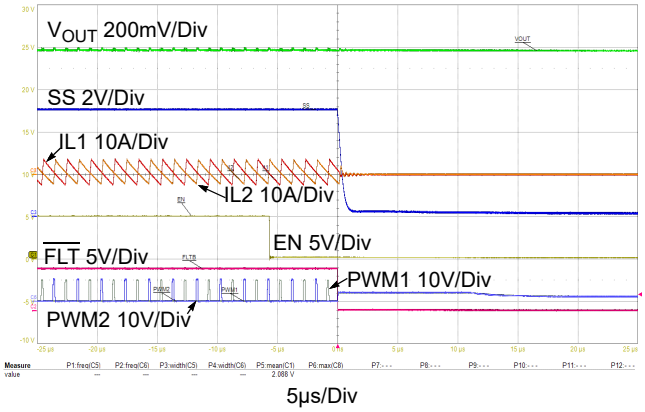


Figure 35. Shutdown with EN (P_{VIN} = V_{DD} = 12V, I_{LOAD} = 0A)

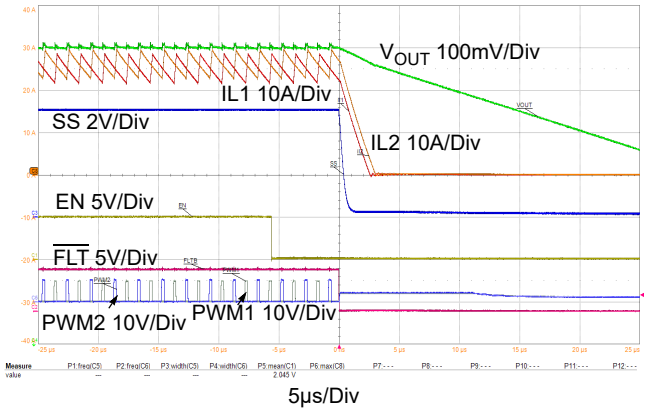


Figure 36. Shutdown with EN (P_{VIN} = V_{DD} = 12V, I_{LOAD} = 50A)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

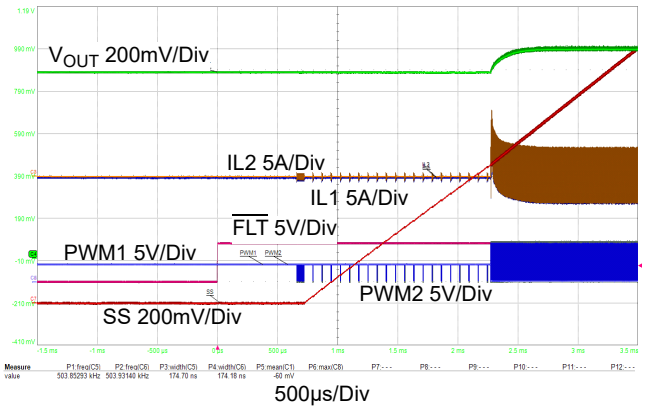


Figure 37. Pre-Biased Start-Up (V_{DD} = 4.62V, P_{VIN} = 12V, I_{LOAD} = 0A, Vpre-bias = 900mV)

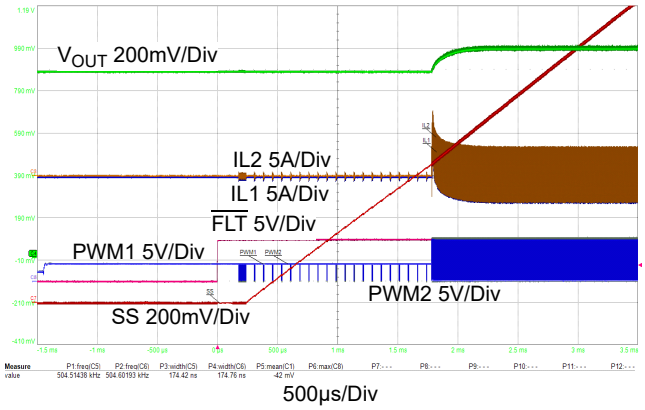


Figure 38. Pre-Biased Start-Up (P_{VIN} = V_{DD} = 12V, I_{LOAD} = 0A, Vpre-bias = 900mV)

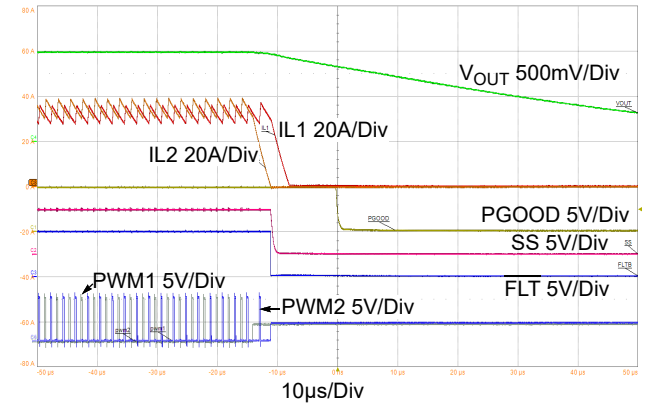


Figure 39. Overcurrent Protection (P_{VIN} = 12V, V_{DD} = 5V)

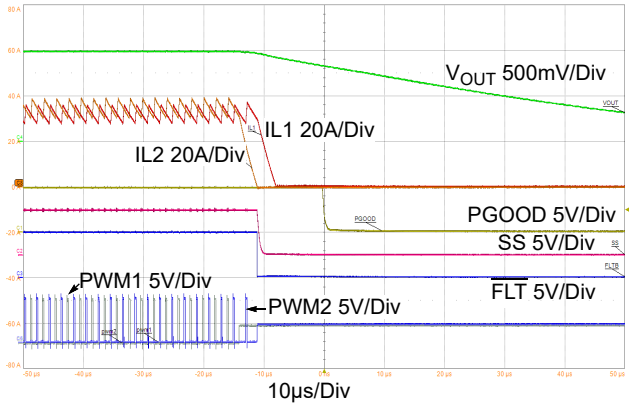


Figure 40. Overcurrent Protection (P_{VIN} = V_{DD} = 12V)

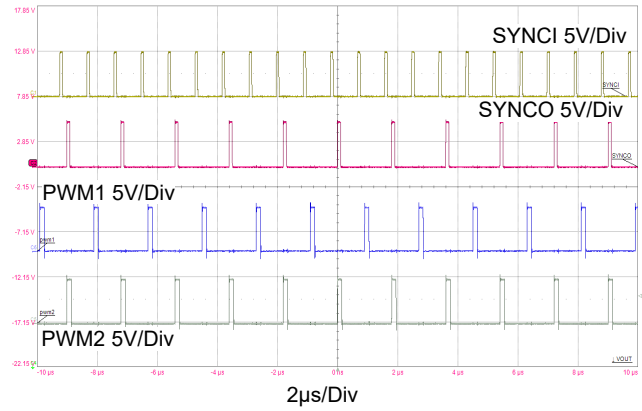


Figure 41. Sync (V_{DD} = 5V, P_{VIN} = 12V, R_{SYNC-O} = 100kΩ to VCC, f_{SYNC-I} = 1.15MHz)

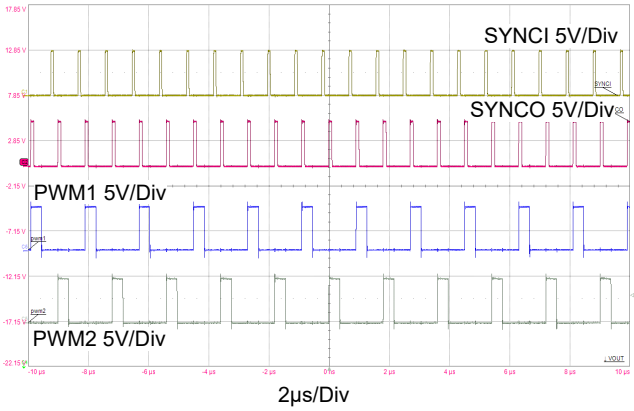


Figure 42. Sync (V_{DD} = 5V, P_{VIN} = 12V, R_{SYNC-O} = 100kΩ to GND, f_{SYNC-I} = 1.15MHz)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

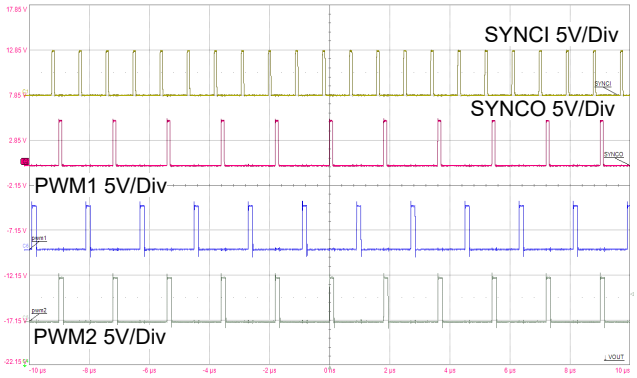


Figure 43. Sync (P_{VIN} = V_{DD} = 12V, R_{SYNC-O} = 100kΩ to VCC, f_{SYNC-I} = 1.15MHz)

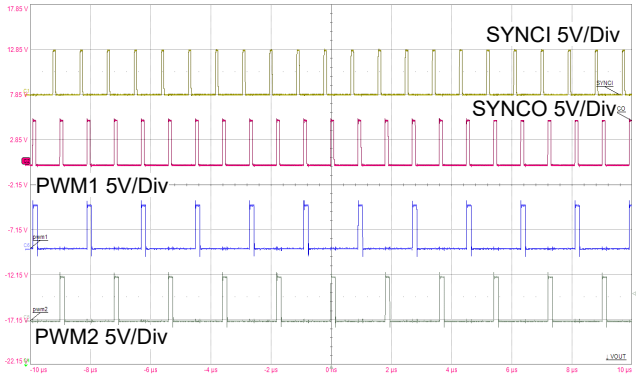


Figure 44. Sync (P_{VIN} = V_{DD} = 12V, R_{SYNC-O} = 100kΩ to GND, f_{SYNC-I} = 1.15MHz)

5. Operational Description

5.1 Dual Phase Operation

The ISL73847SEH can operate in single-phase or dual-phase mode. The part is configured to work in dual-phase mode by default. To operate in single-phase mode, short the PWM output to VCC. Either PWM1 or PWM2 can be chosen for single-phase operation if the other is shorted to VCC. The flexibility of using either output in single-phase can help during layout, as it may be easier to route the current-sense feedback signals to one channel or the other.

5.2 Oscillator and Clock Synchronization

The switching frequency of the controller is determined by a resistor to ground on the FS pin (R_{FS}). The ISL73847SEH can operate with an oscillator frequency of 500kHz to 3MHz. If the FS pin is shorted to ground, the ISL73847SEH reads this as a fault and stops switching.

5.2.1 External Synchronization (SYNC-I)

The ISL73847SEH has a SYNC-I pin that allows synchronizing it to an external clock. It is necessary to set the internal oscillator to 15% less than the required frequency of the external oscillator to use this functionality, ensuring that if the SYNC-I frequency stops at any point, the internal oscillator takes over and continues operating. The allowable frequency range for the external clock is 588kHz to 3MHz. The SYNC-I frequency should be twice the required PWM output switching frequency.

Note: The maximum SYNC-I frequency should not exceed the maximum oscillator frequency (3MHz).

5.2.2 Clock Output (SYNC-O)

The ISL73847SEH has a SYNC-O pin that can output either the oscillator frequency or the PWM output switching frequency. Place a 100kΩ resistor on the SYNC-O pin to ground to output the oscillator frequency. Place a 100kΩ resistor on the SYNC-O pin to VCC to output the PWM output switching frequency. The choice to use one or the other depends on what is receiving the clock pulse. If the clock output is being used to synchronize another ISL73847SEH, it expects a frequency twice the PWM switching frequency (load the pin with 100kΩ to ground). Other PWM regulators such as the ISL7000x family of parts, switch at the same frequency as the incoming frequency (tie with 100kΩ to VCC). When SYNC-O is unloaded, it is in phase with PWM2. During a fault condition, the SYNC-O is asserted low.

5.2.3 Multi-Phase Operation

More phases can be added to the system by connecting multiple ISL73847SEH devices together in a single leader, multi-follower configuration. To synchronize the two or more controllers external clocks can be supplied to the SYNC-I inputs. The frequency of the clocks should be twice the target switching frequency. The phase relationship between the clocks depends on the number of controllers being synchronized. Use Equation 1 to calculate the recommended phase delay required between each SYNC-I clock depending on the number of controllers. The total phase delay should add up to 360°.

(EQ. 1) $$\text{Phase[deg]} = \frac{360}{\text{Controllers}}$$

A simple way to synchronize a 4-phase design is to use the SYNC-O of the leader controller to drive the SYNC-I of the follower controller as shown in Figure 45. The SYNC-O pin needs a 100kΩ to GND to output twice the switching frequency. Because the internal oscillator of the Follower must be set to 15% lower than the external clock, the RFS and RSLOPE resistors are different from the Leader. For a 1MHz switching frequency, the typical SYNC-I to SYNC-O delay of the leader controller creates the 180° phase delay required to drive the SYNC-I of the follower controller directly. As shown, tie the DROOP pins together, tie all the VFB- pins together, and tie all the

FLTb pins together. Tie the COMP pins of all controllers together and only install the compensation components on the leader. Lastly, tie the FB+ pin on each follower to its own DROOP pin.

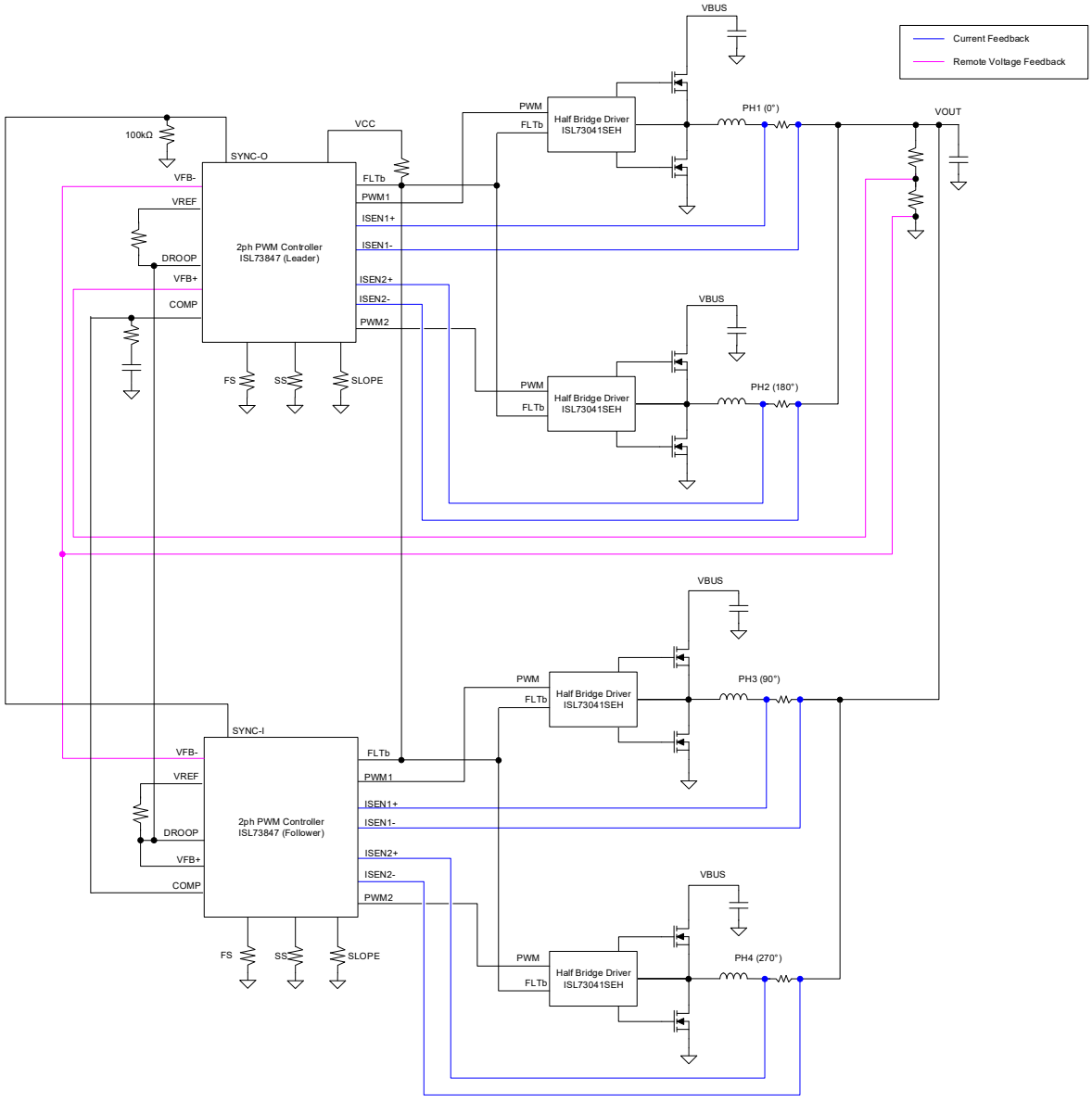


Figure 45. Leader-Follower Configuration for 1MHz 4-Phase Operation

Figure 46 is an oscilloscope capture where 93° phase separation is obtained between Phase 1 and Phase 3 by driving the SYNC-I of the follower with the SYNC-O of the leader directly with no extra delay circuit.

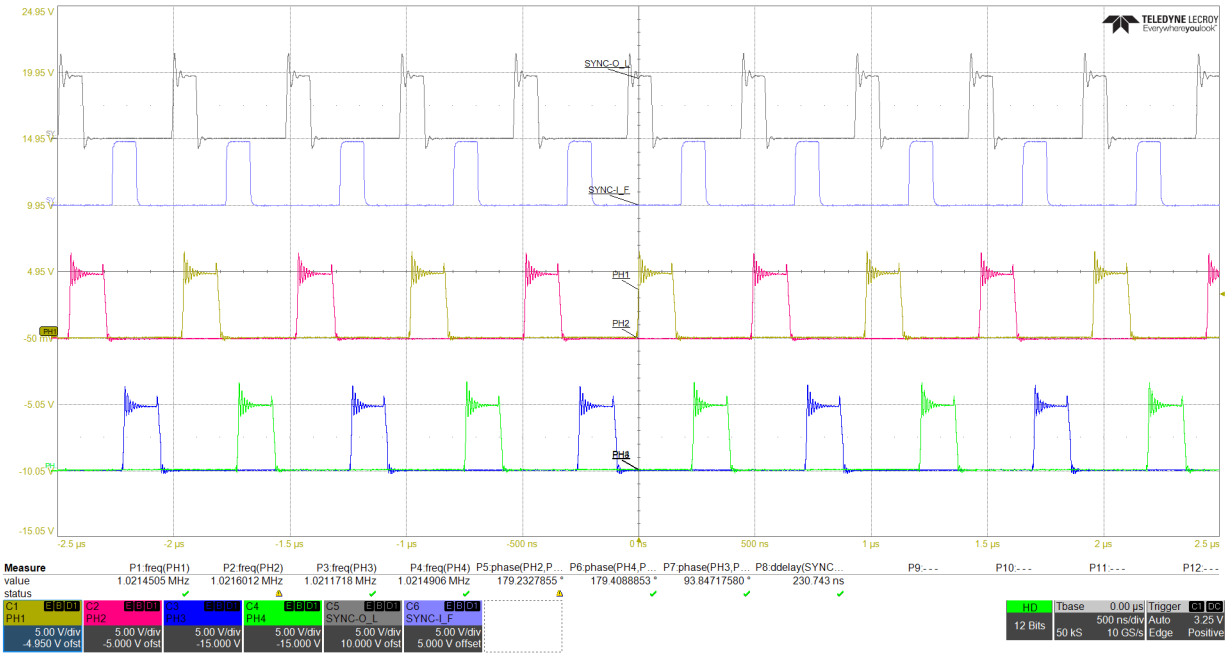


Figure 46. Using SYNC-O of Leader to drive SYNC-I of Follower Phase Shifting

For frequencies above 1MHz or phase counts over 4, an external delay circuit is required. This can be discreetly placed between the leader's SYNC-O and the follower's SYNC-I (Figure 47) or more flexibly with a smaller solution size using the ISL74420 (Figure 48).

Use Equation 2 to calculate the time delay from phase.

(EQ. 2) $$Delay = \frac{Phase}{(720 \times f_{SW})}$$

- Delay is the time delay in seconds.
- Phase is the phase delay in degrees.
- f_{SW} is the target switching frequency in Hertz.

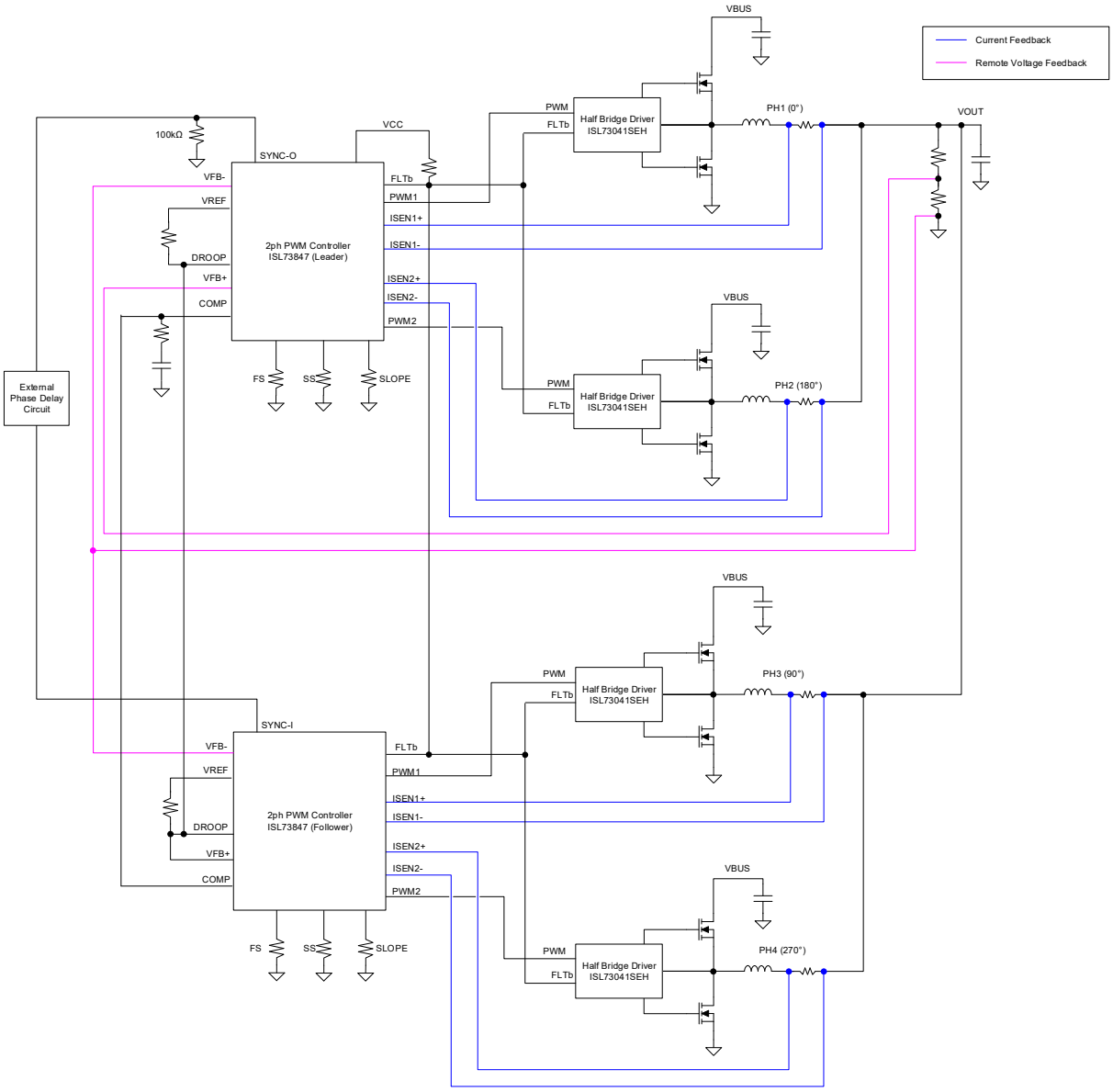


Figure 47. Leader-Follower Configuration for 4-Phase Operation

Another way to synchronize multiple ISL73847SEH devices is to use the ISL74420. Figure 48 is an example of a 4-phase using the ISL74420 to provide one clock to each controller. Both clocks are twice the converter switching frequency and 180° out-of-phase with each other for ideal multi-phase interleaving.

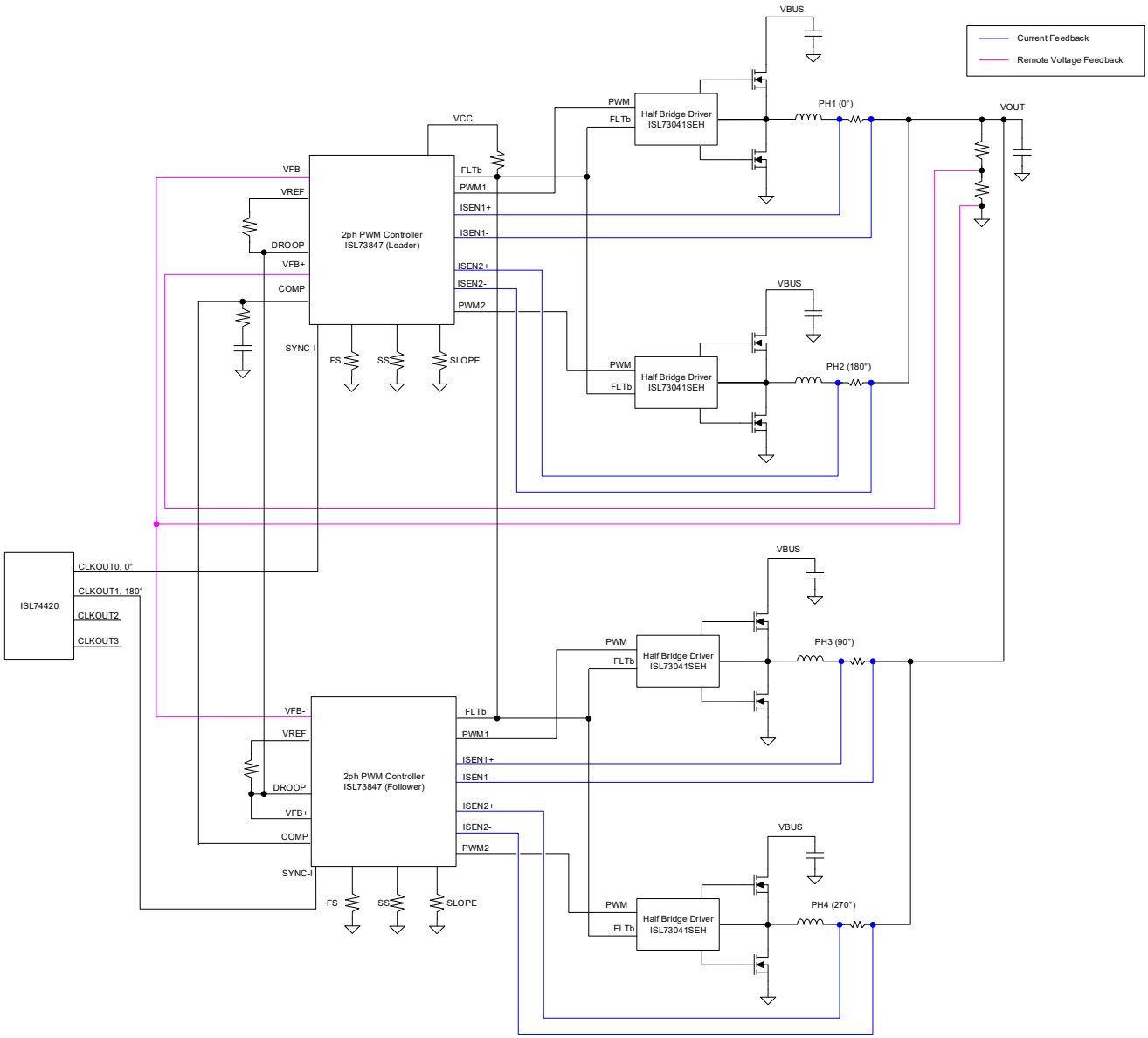


Figure 48. Leader-Follower Configuration for 4-Phase Operation

Figure 49 is an oscilloscope capture for a 4-phase, 1MHz, 5V to 0.8V, 100A reference design that uses the ISL74420 to output two 2MHz clocks, 180° out-of-phase for synchronization.

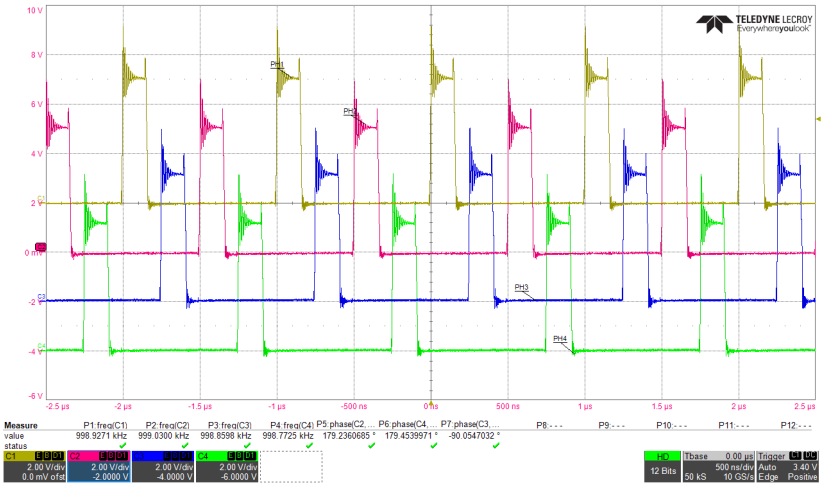


Figure 49. 4-Phase Clock Phase Shifting

5.3 Remote Sensing

The ISL73847SEH can provide differential remote sensing. This sensing allows for the power stage to reside close to the point of load and has the controller further away to reduce the possibility of noise injection because of switching noise from the power stage. In this configuration, the remote sensing also allows the ISL73847SEH to compensate for any loss along the copper planes carrying large currents.

5.4 Droop Regulation

Droop regulation can minimize transient voltages on the regulated output during large load steps. It lowers the output voltage as the load current increases, effectively increasing the DC output impedance for the power supply.

Droop regulation is tuned by adding a resistor between VREF and DROOP. The ISL73847SEH sinks a current on DROOP that is proportional to the sum of the differential voltage across both current sense inputs. This current through the resistor between VREF and DROOP changes the reference voltage presented to the error amplifier, thereby changing the DC regulation point. The larger the resistor, the greater the variation in regulated voltage with respect to the load current.

5.5 Peak Current Mode Control

The ISL73847SEH regulates peak current mode by presenting the current-sense signal directly to the PWM comparator. The current-sense amplifier has a minimum bandwidth of 10MHz, allowing it to keep up with the ripple current through the inductor. The PWM pulse is terminated when the current crosses the error amplifier output.

The ISL73847SEH has two identical peak mode control comparators, one for each set of PWM and ISEN pins. The matching between these two comparators is important to consider when setting the overcurrent thresholds of the part. The current sharing accuracy of the two phases is specified as the millivolts of offset between the phase's actual current and what that current would ideally be. For example, if a 50A load is pulled from a 2-phase system, ideally an average current of 25A per phase is achieved. With a 2mΩ sense resistor, that corresponds to 50mV on each pair of ISEN pins. A 4mV current sharing limit ($I_{PHSHARE}$) means that one phase might be as high as 54mV, which corresponds to 27A of load current. The other phase must be 23A (or 46mV) to supply the 50A load.

5.6 Tri-State PWM Control

The ISL73847SEH features a tri-level PWM output with low-level, high-level, and mid-level voltage. The high-level output turns on the high-side FET, while a low-level output turns on the low-side FET, and the mid-level output

turns off both the high-side and low-side FETs. This state is helpful during fault conditions where you want to protect any downstream devices and the power stage. Connect a 100kΩ resistor on PWM1 and PWM2 to GND.

The ISL73847SEH works with drivers that accept a tri-level input, like the ISL73041SEH.

5.7 Boot Refresh

When the ISL73847SEH first powers up before soft-start, it issues a boot refresh command that consists of 32 mid-to-low transitions on the PWM output, allowing sufficient time for the boot capacitor to charge up. The switching frequency determines the frequency of the boot refresh pulses and the pulse is equal to the minimum on-time (t_{MIN_ON}). An appropriate boot capacitor value can be determined using the frequency and pulse widths.

Whenever the ISL73847SEH is tri-stated, it starts an analog timer that lasts 60µs ±60% (tolerance because of process and part-to-part variation). Four additional boot refresh pulses are transmitted if the timer completes before the next high-level signal to ensure the boot voltage is replenished. This would be the case in a pre-biased startup, where there could be significant time between the boot refresh pulses and the first high-side signal.

5.8 Current Sense Amplifiers and Current Monitoring (IMON)

The ISL73847SEH uses 10MHz (minimum) transconductance amplifiers for each phase to continuously achieve peak current control by sensing the inductor current. Current sensing can be accomplished using a shunt resistor on the output side of the inductor or through inductor DCR sensing. Shunt sensing provides high precision accuracy at the cost of power dissipation, while DCR current sensing has little power dissipation because of indirectly senses the inductor current. Its drawbacks include reduced accuracy across the operating temperature range and the inability to sense when an inductor is saturating; therefore, Renesas recommends using soft saturation inductors.

The ISL73847SEH has an IMON pin that monitors the current through the power supply for telemetry purposes. Connect a resistor from the IMON pin to GND. In this configuration, the IMON pin reflects the average of the inductor ripple current. An additional capacitor in parallel with the resistor can improve averaging. The size of the capacitor needed to average the current depends on the ripple seen on the IMON pin.

5.9 Adjustable Slope Compensation

The ISL73847SEH is a peak current mode controller prone to subharmonic oscillations when the duty cycle exceeds 50%. Adding a compensating ramp equal to the downslope of the inductor current can dampen any subharmonic oscillation within one switching cycle. Renesas recommends using adequate slope compensation if the nominal duty is under but close to 50%, as the duty cycle could cross 50% as the load increases. The slope compensation depends on the SLOPE pin and the FS pin.

If slope compensation is insufficient, the converter can experience subharmonic oscillation that could result in noise emissions at half the switching frequency. However, too much slope compensation can deteriorate the phase margin; therefore, slope compensation must be carefully considered.

5.10 Pulse Skipping

The ISL73847SEH can skip pulses if the feedback indicates excessive minimum pulse width. One scenario where this can arise would be during a load release when operating close to the minimum on-time. Pulse skipping reduces the overshoot during the unloading in a transient step.

5.11 VDD and VCC Range

The ISL73847SEH has an internal LDO that provides the bias for all internal circuitry. The input of the LDO is VDD, which accepts a range of 4.5V up to 19V. VCC is the output of the LDO, which regulates 5V. When VDD is operating in the range of 4.5V to 5.0V, VCC tracks VDD minus the dropout.

5.12 Enable

The ISL73847SEH features a 2-stage enable. When enable is at 1V (gross threshold), the internal circuitry is biased (such as reference voltage, oscillator, and logic) but switching is disabled. When the voltage of EN crosses the fine threshold, switching is enabled, and the IC attempts a boot refresh and soft-start. Because of filtering for Single Event Effects (SEE), the EN logic state (high or low) must persist for at least 80µs for the part to recognize it and respond. The enable pin has a pull-down that disables the part if the pin is not actively driven.

5.13 Initialization and Startup

When the ISL73847SEH first powers up, it goes through several states before boot refresh and soft-start. After VDD has crossed the rising UVLO threshold, the oscillator waits for 128 clock cycles at 500kHz before allowing the digital core to enter its configuration state. The configuration state lasts 886 clock cycles at 500 kHz. When the digital core completes its configuration, it signals the oscillator to switch to the frequency set by the FS pin or SYNC-I. After an additional 128 clock cycles at the new frequency, boot refresh pulses commence, followed by soft-start. Figure 50 and Figure 51 illustrate the start-up sequence.

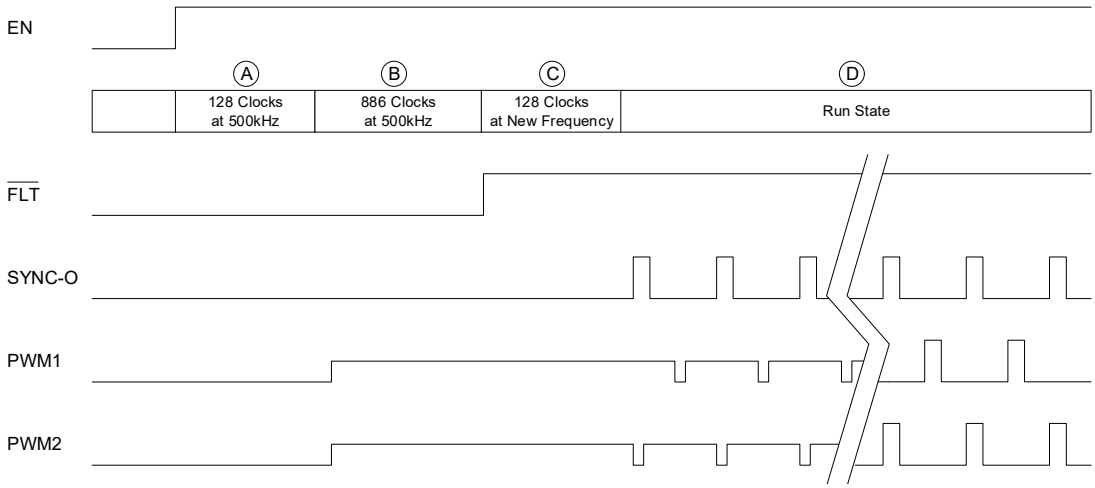


Figure 50. Start-Up Timing Diagram (R_{SYNC-O} = OPEN)

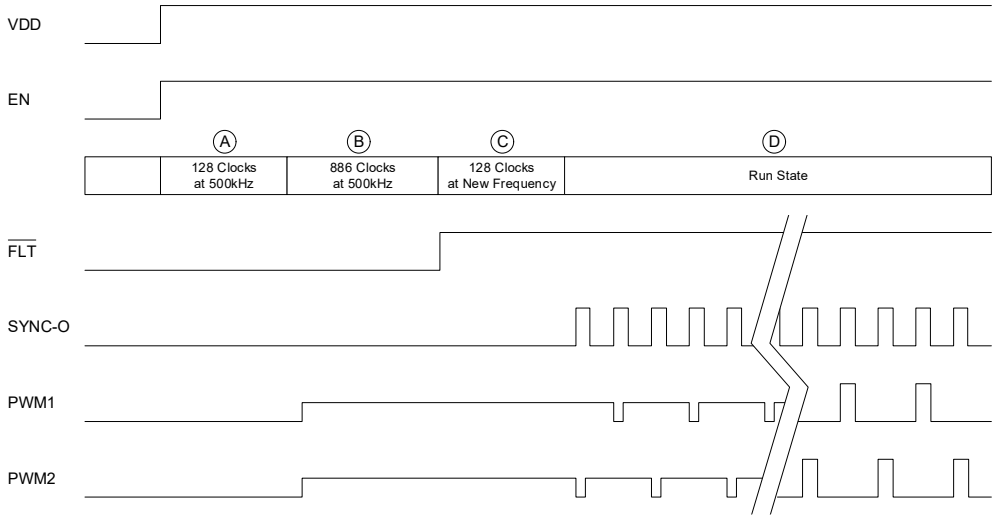


Figure 51. Start-Up Timing Diagram (R_{SYNC-O} = 100kΩ)

During states A and C in Figure 50 and Figure 51, the oscillator blanks the clock signal to the digital core. Therefore, the oscillator has time to stabilize its frequency before entering the configuration state (B) or run state (D).

IMPORTANT: During states A and C, the digital core does not receive a clock; therefore, it cannot detect a rising edge on EN. Instead, the EN signal must persist long enough so the digital core can read it during states B and D. The ISL73847SEH reacts to a falling edge on EN regardless of the controller's state.

5.14 Hiccup

Any time the ISL73847SEH encounters a fault, it enters hiccup mode. During hiccup mode, the controller waits for one soft-start cycle before attempting to start switching again. If the fault has not cleared after the dummy soft-start cycle has completed, the ISL73847SEH waits until it clears and starts the PWM output switching. This would be the case if the fault that tripped was the driver pulling $\overline{FLT}$ low because of an over-temperature fault.

If an output short occurs, the part would hiccup, go through a dummy soft-start cycle, and attempt to start up indefinitely until the output short is removed. In this case, as soon as the part starts switching, it would trip the gross overcurrent threshold and go back to hiccup. When the output short is removed, normal operation resumes after the configuration sequence, which is 886 clock cycles at 500kHz.

5.15 Fault Handling

5.15.1 Cycle-by-Cycle Current Limit

The current flowing through the inductor is monitored through the current-sense inputs using a sense resistor or DCR sensing. When the input reaches the current limit threshold (V_{PCL}), the PWM pulse is terminated to limit the peak current. A single cycle-by-cycle current limit event does not trigger a hiccup, but if there are four current limit events in an eight-clock cycle window, the ISL73847SEH enters a hiccup.

5.15.2 Inductor Peak Overcurrent Protection

If the output current increases after triggering the cycle-by-cycle current limit, the ISL73847SEH has a second overcurrent protection (V_{POC} and V_{NOC}). If triggered, it drives the PWM outputs to mid-level (tri-state the power stage) and enters a hiccup. If the initial fault persists or another fault occurs during the next soft-start, the cycle repeats indefinitely and stays in hiccup. The overcurrent protection protects against both positive and negative overcurrent conditions.

5.15.3 Overvoltage and Undervoltage Fault

The ISL73847SEH has overvoltage and undervoltage protection, which triggers when $V_{(FB, OV)}$ or $V_{(FB, UV)}$ is exceeded. If the $V_{(FB, OV)}$ or $V_{(FB, UV)}$ levels are reached, the part enters a hiccup.

5.15.4 $\overline{FLT}$ Pin

The $\overline{FLT}$ pin (FLT stands for Fault) is a bi-directional communication pin between the ISL73847SEH controller and the ISL73041SEH driver. On the ISL73847SEH, the $\overline{FLT}$ pin is low and is an I/O when the part is not ready (during startup) or encounters a fault. The ISL73041SEH uses this pin to communicate if it is not ready to accept input or encounters a fault on its end. In either case, if the $\overline{FLT}$ pin is pulled low by the ISL73041SEH, the ISL73847SEH sets its PWM outputs to mid-level and enters a hiccup. PWM at mid-level tells the ISL73041SEH to turn off both of its FET outputs. The $\overline{FLT}$ pin is an input while switching (during and after startup).

Note: The FLT Mid Threshold Voltage in the Electrical Characteristic table is the same as the $\overline{FLT}$ Falling Threshold.

5.15.5 Oscillator and Sync Input Fault

If the FS pin is inadvertently shorted to ground, this causes a fault in the controller, and switching would be inhibited.

The ISL73847SEH can synchronize to an external frequency. If the external clock is not present or if the internal clock frequency is not less than 15% of the required external clock frequency, the part reverts to the internal oscillator and continues operation. When the external sync input returns or if the internal clock frequency is less

than 15% of the required external clock frequency, the ISL73847SEH immediately switches back to the external clock, as shown in Figure 52.

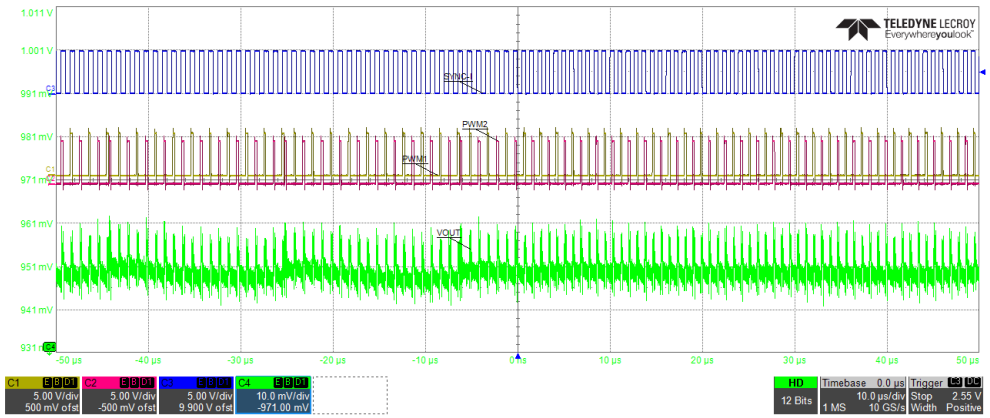


Figure 52. Switching between Internal Oscillator and External Oscillator on SYNC-I (External clock frequency changed from 1MHz to 1.15MHz)

While switching between the internal and external oscillators, there may be a glitch observed on the regulated output. The size of this glitch depends on the frequency difference between the internal and external clock, output capacitance, and output loading.

The internal oscillator must be configured to operate 15% slower than the minimum external frequency applied to the SYNC-I pin to ensure that this fail safe works accordingly,. Setting the internal oscillator to a frequency that is too close to the external sync frequency can result in the clock output alternating between the internal and external clock, resulting in a beat frequency.

If the SYNC-I function is unnecessary, leave the pin floating as it has an internal pull-down. If whatever is driving the SYNC-I pin gets stuck in either a logic high or low, and as long as there are no transitions, the ISL73847SEH reverts to the internal oscillator.

6. Applications Information

6.1 PWM Output Switching Frequency Selection

The PWM output switching frequency is half the frequency of the internal oscillator. This is done to obtain a precise 180° phase shift between phases. The switching frequency is determined based on the requirements of the regulator size, power dissipation, and conversion ratio, where minimum controllable on/off times should be considered. Increasing the switching frequency reduces the solution size but, at the same time, increases switching losses. A balance must be reached between these parameters to decide the optimal switching frequency.

When the switching frequency is determined, the FS resistor (frequency setting resistor) can be determined by using Equation 3. Renesas recommends using precision resistors to set the oscillator frequency as variations in the resistor increase the oscillator frequency spread.

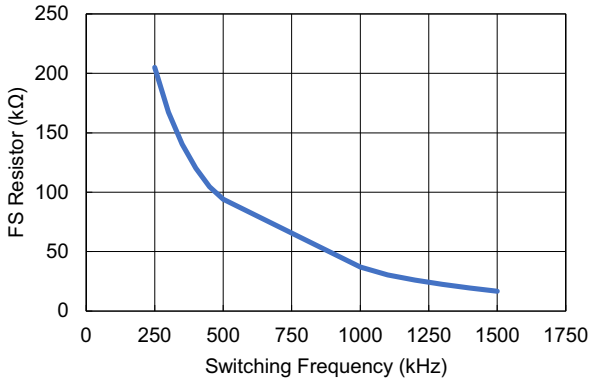


Figure 53. R_{FS} vs Frequency

The oscillator frequency is determined by a resistor to ground on the FS pin where R_{FS} is in kiloohms (kΩ) for a desired switching frequency f_{SW} in kilohertz (kHz).

(EQ. 3) $$R_{FS}[k\Omega] = \frac{56497}{f_{SW}[kHz]} - 20.96$$

IMPORTANT: Equation 3 approximates the real data presented in Figure 53. The data used for Figure 53 is typical, and there is some variation because of temperature and variation. This variation is shown in the electrical specifications table by providing four fixed resistors and the frequency and tolerance achieved with those resistors.

6.2 Output Voltage Setting

Use Equation 4 to calculate the required regulated output voltage. For greater voltage accuracy, Renesas recommends using 0.1% feedback resistors.

(EQ. 4) $$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)$$

- V_{OUT} is the required regulated output voltage.
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.6V (typical).
- R_1 is the bottom resistor in the feedback divider.
- R_2 is the top resistor in the feedback divider.

6.3 Resistor Current Sensing and Monitoring Setting

The ISL73847SEH can sense current through a shunt resistor or DCR sensing. Use Equation 5 to determine the required shunt resistance or minimum DCR of the inductor. Depending on what PV_{IN}, V_{OUT}, and $I_{OUT(MAX)}$ are, DCR sensing might not be practical. For example, in a high current and low output voltage application, getting an inductor that meets both the minimum DCR requirement and the saturation current capability might not be possible. In this case, shunt sensing is the only option.

(EQ. 5) $$R_{SEN} = \frac{V_{SEN} \times n}{I_{OUT(MAX)}}$$

- R_{SEN} is the sense resistor or DCR of the inductor.
- n is the number of phases (for the ISL73847SEH this is either 1 or 2).

- $I_{OUT(MAX)}$ is the max DC output current for all phases.
- V_{SEN} is the target current-sense amplifier input voltage during steady-state operation, which is 50mV (typical).

It is necessary to add RC filters for the sense resistor and DCR sensing. In the case of the sense resistor, it is to compensate for the parasitic inductance. Use Equation 6 to calculate the RC filter if the resistance and parasitic inductance of the sense resistor are known. For DCR sensing, the RC filter has to be properly selected such that the voltage across the cap is proportional to the current through the inductor.

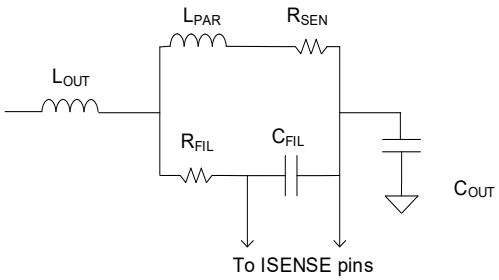


Figure 54. R_{SEN} Parasitic Inductance Compensation RC Circuit

(EQ. 6) $$\frac{L_{PAR}}{R_{SEN}} = R_{FIL} \times C_{FIL}$$

- R_{FIL} is the resistance of the resistor in the RC filter.
- C_{FIL} is the capacitance of the capacitor in the RC filter.
- R_{SEN} is the sense resistor from Equation 5.
- L_{PAR} is the parasitic inductance of R_{SEN}.

The ISL73847SEH continuously monitors the inductor current of each phase. The IMON pin outputs a current proportional to the summation of current from both phases.

(EQ. 7) $$I_{MON} = \sum_{n=1}^{2} R_{SEN} \times I_{Ln} \times g_{m(CSA, IMON)}$$

- I_{MON} is the current out of the IMON pin.
- R_{SEN} is the sense resistor calculated from Equation 5.
- I_{Ln} is the inductor current for a given phase, where n is the phase number.
- $g_{m(CSA, IMON)}$ is the transconductance from the input of the current sense amp to the IMON pin, which is 0.39µA/mV (typical).

6.4 DCR Current Sensing

The DCR method of current sensing in a buck converter uses the DC resistance of the inductor winding as the current sense element. This method eliminates the need for a sense resistor and improves efficiency. The inductor DCR does vary based on the temperature coefficient of the selected winding material, such as Cu. However, these variations are not quite as wide as using a MOSFET for $r_{DS(ON)}$ sensing. This method is often used in low-output voltage converters, as any voltage drop on a sense resistor negates the low-output voltage. Keep in mind that DCR sensing is not recommended for current-sharing applications.

If the DCR = R_{SEN}, place an RC filter across the inductor. as shown in Figure 55.

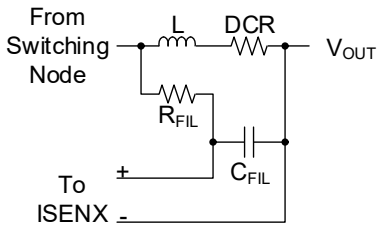


Figure 55. DCR Current Sensing when DCR = R_{SEN}

Calculate the component values using Equation 8:

(EQ. 8) $$\frac{L}{DCR} = R_{FIL} \times C_{FIL}$$

- L is the output inductor value.
- DCR is the DC resistance of inductor winding.
- R_{FIL} is the resistor value selected for DCR sensing and filtering.
- C_{FIL} is the capacitor value selected for DCR sensing and filtering.

If DCR < R_{SEN}, a resistor can be added to get the required R_{SEN}, as shown in Figure 56.

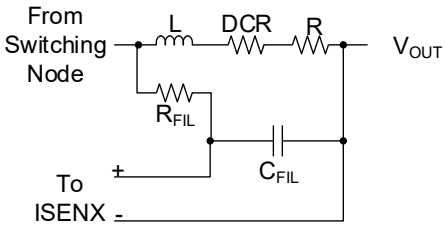


Figure 56. DCR Current Sensing when DCR < R_{SEN}

Calculate the component values using Equation 9. For example, if R_{SEN} is 2mΩ and the chosen inductor has a DCR of 1mΩ, a 25mV current sense signal is produced instead of a 50mV signal. To fix this, add R = 1mΩ in series with the inductor to get a R_{SEN} = 2mΩ.

(EQ. 9) $$\frac{L}{DCR + R} = R_{FIL} \times C_{FIL}$$

- L is the output inductor value.
- DCR is the DC resistance of inductor winding.
- R is the added resistor in series with the inductor.
- R_{FIL} is the resistor value selected for DCR sensing and filtering.

C_{FIL} is the capacitor value selected for DCR sensing and filtering.

If DCR > R_{SEN}, a voltage divider must be added to the current sense filter to obtain the required R_{SEN}, as shown in Figure 57.

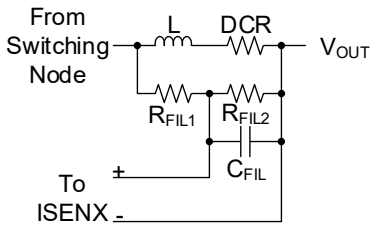


Figure 57. DCR Current Sensing when DCR > R_{SEN}

Calculate the component values using Equation 10. For example, if R_{SEN} is 2mΩ and the chosen inductor has a DCR of 3mΩ, a 75mV current sense signal is produced instead of a 50mV signal. To fix this, use an R_{FIL1} = 1kΩ and R_{FIL2} = 2kΩ divider to reduce the 75mV current sense signal to 50mV.

(EQ. 10) $$\frac{L}{DCR} = \frac{R_{FIL1} \times R_{FIL2}}{R_{FIL1} + R_{FIL2}} \times C_{FIL}$$

- L is the output inductor value.
- DCR is the DC resistance of inductor winding.
- R_{FIL1} and R_{FIL2} are the resistor values selected for DCR sensing and filtering.
- C_{FIL} is the capacitor value selected for DCR sensing and filtering.

6.5 Inductor Selection

To select the proper inductance value, determine the input voltage, output voltage, switching frequency, and inductor ripple current. Renesas recommends ensuring the inductor ripple current is 30%.

(EQ. 11) $$I_{OUT} = n \times I_{PHASE}$$

- n is the number of phases (for the ISL73847SEH this is either 1 or 2).
- I_{PHASE} is the phase current.

Designing with less ripple current reduces the output voltage ripple but comes at the expense of slower transient response. Therefore, the amount of acceptable ripple would need to be decided on a per-application basis.

Use Equation 12 to calculate a good first-pass estimate for the inductor size.

(EQ. 12) $$L_{REC} = \frac{(V_{IN} - V_{OUT}) \times D \times n}{k \times f_{SW} \times I_{OUT}}$$

- L_{REC} is the recommended inductance.
- V_{IN} is the input voltage to the power supply.
- V_{OUT} is the output voltage of the power supply.
- D is the duty cycle; for a buck converter, it is (V_{OUT}/V_{IN}).
- k is the inductor ripple to DC current ratio (k = 0.3 is recommended).
- n is the number of phases (for the ISL73847SEH this is either 1 or 2).
- f_{SW} is the switching frequency of the power supply.
- I_{OUT} is the output current of the regulator.

6.6 Slope Compensation

Use Equation 13 to calculate the slope compensation resistor:

(EQ. 13) $$R_{SLOPE} = \frac{R_{SEN} \times R_{FS} \times V_{OUT}}{k \times L_{SEL}}$$

$$25k\Omega \leq R_{SLOPE} \leq 100k\Omega$$

- R_{SLOPE} is the slope compensation resistor.
- R_{SEN} is the value of the current sensing resistor.
- R_{FS} is the value of the resistor that sets the switching frequency.
- V_{OUT} is the output voltage of the power supply.
- k is a constant, 25kV/s.
- L_{SEL} is the user-selected output inductance.

The R_{SLOPE} value must stay within 25kΩ to 100kΩ for proper operation of the internal circuitry. If R_{SLOPE} is less than 25kΩ, L_{SEL} must be decreased; If R_{SLOPE} is greater than 100kΩ, L_{SEL} must be increased.

6.7 Error Amplifier Compensation and Output Capacitance

To calculate the output capacitor and compensation values, the transient response ΔV_{OUT} and transient current step ΔI_{OUT} must be known. With these two known values, use Equation 14 to calculate the equivalent load-line output impedance R_{LL}.

(EQ. 14) $$R_{LL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

As an example, if a regulator needs to meet a 5% transient specification for V_{OUT} = 1V and ΔI_{OUT} = 50A, ΔV_{OUT} is 50mV (1V×5%), which would make R_{LL} = 50mV/50A = 1mΩ.

The error amplifier is a transconductance amplifier that makes it much easier to compensate by placing a series resistor and capacitor on the output of the amplifier (COMP pin). Use Equation 15 to determine the compensation resistor (R_{COMP}).

(EQ. 15) $$R_{COMP} = \frac{V_{OUT} \times R_{SEN} \times A_{CSA}}{n \times V_{REF} \times g_{m(EA)} \times R_{LL}}$$

- R_{COMP} is the COMP pin resistor.
- R_{SEN} is the sense resistor or minimum DCR of the inductor.
- A_{CSA} is the gain of the current sense amplifier, which is 8mV/mV (typical).
- n is the number of phases (for the ISL73847SEH this is either 1 or 2).
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.6V (typical).
- $g_{m(EA)}$ is the transconductance of the error amplifier, which is 3.57mA/V or 3.57mS (typical).
- R_{LL} is the equivalent load-line output impedance calculated with Equation 14.

The output capacitance determines the unity gain frequency f_T. Renesas recommends setting the unity gain frequency a decade below the switching frequency ($f_T = f_{SW}/10$). After selecting real output capacitors, rearrange Equation 16 to solve for f_T and recalculate the actual unity gain frequency (f_T).

(EQ. 16) $$C_{OUT(MIN)} = \frac{n \times R_{COMP} \times g_{m(EA)} \times V_{REF}}{2\pi \times f_T \times A_{CSA} \times R_{SEN} \times V_{OUT}}$$

- $C_{OUT(MIN)}$ is the minimum output capacitance needed for the required unity gain frequency of the regulator.
- R_{COMP} is the COMP pin resistor calculated in Equation 15.
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.6V (typical).
- V_{OUT} is the output voltage of the power supply.
- f_T is the unity gain frequency of the regulator, typically $f_T = f_{SW}/10$.
- R_{SEN} is the sense resistor or minimum DCR of the inductor.
- A_{CSA} is the gain of the current sense amplifier, which is 8mV/mV (typical).

Equations for R_{COMP} and $C_{OUT(MIN)}$ are derived for an ideal case where the output capacitance has no parasitic ESR and ESL. The actual equivalent output capacitance has some parasitic ESR and ESL that impact the transient response. Use Equation 17 to approximate the total transient response.

(EQ. 17) $$\Delta V_{OUT(TOTAL)} = \Delta V_{OUT} + \Delta V_{ESR} + \Delta V_{ESL}$$

- ΔV_{OUT} is the value in Equation 14 used for calculating R_{LL}.
- ΔV_{ESR} is the output voltage deviation due to the equivalent parasitic ESR, calculated in Equation 18.

(EQ. 18) $$\Delta V_{ESR} = \Delta I_{OUT} \times ESR$$

- ΔV_{ESL} is the output voltage deviation due to the equivalent parasitic ESL, calculated in Equation 19, where di/dt is the slew rate of the transient step.

(EQ. 19) $$\Delta V_{ESL} = ESL \times di/dt$$

Note: Equation 17 is a rough estimate because these three components that affect the transient response never have maximum values simultaneously. Therefore, it should be clear that the ideal ΔV_{OUT} calculated in Equation 14 must be reduced to account for parasitic ESR and ESL in the output capacitors. For example, for a design goal of 5% total transient response, if both ΔV_{ESR} and ΔV_{ESL} are causing 1% V_{OUT} disturbance each, the real ΔV_{OUT} used in Equation 14 should be 3% (5%-2%).

C_{COMP} sets the zero frequency of the error amplifier. To maximize the phase margin of the regulator, Renesas recommends setting the zero formed by R_{COMP} and C_{COMP} a decade smaller than the actual unity gain frequency of the regulator calculated with actual output capacitance ($f_Z = f_T/10$). Use Equation 20 to calculate the C_{COMP} value.

(EQ. 20) $$C_{COMP} = \frac{1}{2\pi \times f_Z \times R_{COMP}}$$

- C_{COMP} is the compensation capacitance.
- R_{COMP} is the COMP pin resistor calculated in Equation 15.
- f_Z is the zero frequency set by R_{COMP} and C_{COMP}, based on the actual f_T calculated from the actual output capacitance.

6.8 Pole Capacitor

A pole capacitor must be added in parallel with R_{COMP} and C_{COMP} to cancel out the zero created by the equivalent ESR and C_{OUT}. To calculate C_{POLE} use Equation 21.

(EQ. 21) $$C_{POLE} = \frac{C_{OUT} \times ESR}{R_{COMP}}$$

6.9 Droop Regulation Setting

Droop regulation changes the DC regulation set point inversely to the output load current, improving the transient response. Place a resistor between the DROOP and VREF pins to use droop regulation. If droop regulation is unnecessary, short the DROOP and VREF pins together. Figure 58 shows the transient response with droop resistor = 0Ω, and Figure 59 shows the transient response with droop resistor = 604Ω. With droop regulation, the transient response is reduced by 40%, which could allow a reduction in output capacitance if there is margin in ΔV_{OUT}.

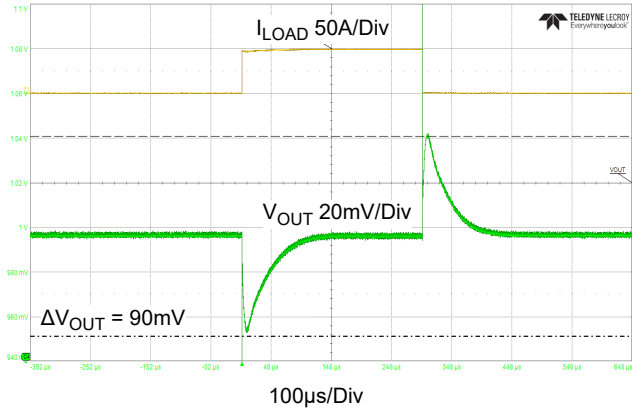


Figure 58. Transient Response without Droop Regulation

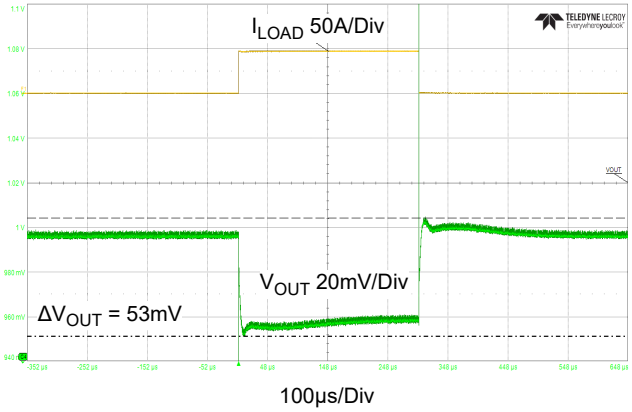


Figure 59. Transient Response with Droop Regulation

As the output loading increases, the current into the DROOP pin increases and generates a voltage across the resistor between the DROOP and VREF pins. This lowers the reference voltage presented to the error amplifier, effectively lowering the regulation point. The extent of the droop variation can be tuned by carefully selecting the droop resistor.

When using droop regulation, it is important to set the light load regulation point at the highest acceptable voltage using Equation 4. Then, calculate the percent deviation of the regulated voltage needed to achieve the lowest acceptable voltage at the maximum DC loading. When the percentage deviation ($DRP_{percent}$) is determined, use Equation 22 to calculate the resistance between VREF and DROOP.

(EQ. 22) $$R_{DROOP} = \frac{DRP_{percent} \times V_{REF}}{I_{DROOP} \times n}$$

- R_{DROOP} is the resistance between the VREF and DROOP pins.
- $DRP_{percent}$ is the required droop of VOUT at full load. For example, DRPpercent = 0.05 for 5% VOUT droop.
- V_{REF} is the internal voltage reference, which is 0.6V (typical).
- I_{DROOP} is the current into the DROOP pin (also known as the ERROR_DRP in the EC Table), which is 19.9µA (typical).
- n is the number of phases (for the ISL73847SEH this is either 1 or 2).

Because I_{DROOP} follows the inductor current, average the signal to get the DC load current. Use Equation 23 to calculate the value of the capacitance:

(EQ. 23) $$C_{DROOP} = \frac{R_{COMP} \times C_{COMP}}{R_{DROOP}}$$

- C_{DROOP} is the droop capacitance.
- R_{DROOP} is the resistance between the VREF and DROOP pins.

- R_{COMP} is the resistor in the series RC on the COMP pin from Equation 15.
- C_{COMP} is the capacitor in the series RC on the COMP pin.

6.10 Soft-Start Capacitor Selection

The ISL73847SEH has an adjustable soft-start to help control the inrush current during startup. A capacitor to ground on the SS pin controls the startup dynamics of the power supply. Use Equation 24 to calculate the capacitance given the required soft-start time.

(EQ. 24) $$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}}$$

- C_{SS} is the soft-start capacitance.
- t_{SS} is the required soft-start time.
- V_{REF} is the reference voltage, which is 0.6V (typical).
- I_{SS} is the current sourced out of the SS pin, which is 10µA (typical).

The output should be in regulation when the soft-start capacitor reaches the band gap voltage of 0.6V. However, the ISL73847SEH waits until soft-start reaches 0.9V before allowing PGOOD to reflect the output state.

6.11 Layout

6.11.1 Layout Guidelines

The following are recommendations for the best performance on the ISL73847SEH:

- Place the VDD bulk and high-frequency capacitor as close as possible to the VDD pin.
- Place the feedback resistors as close as possible to the VFB+ and VFB- pins to minimize parasitic capacitance.
- Ensure that all feedback traces are routed away from noisy switching nodes.
- Place the RSENSE RC filter as close to the ISENX+ and ISENX- pins as possible.
- Place C_{COMP}, R_{COMP}, and C_{POLE} as close as possible to the COMP pin.
- SS, DROOP, and VREF capacitors should be referenced to VFB-.
- Ensure to have a good ground plane.
- Place bulk and high-frequency PVIN capacitors close to the ISL70020SEH FETS drain (Not drawn).
- Minimize the current loop area between the PVIN bulk capacitors and GND and phase node connections
- Connect the feedback traces to the load for point-of-load (POL) regulation.
- Ensure that the traces carrying high load currents are wide enough.

6.11.2 Layout Example

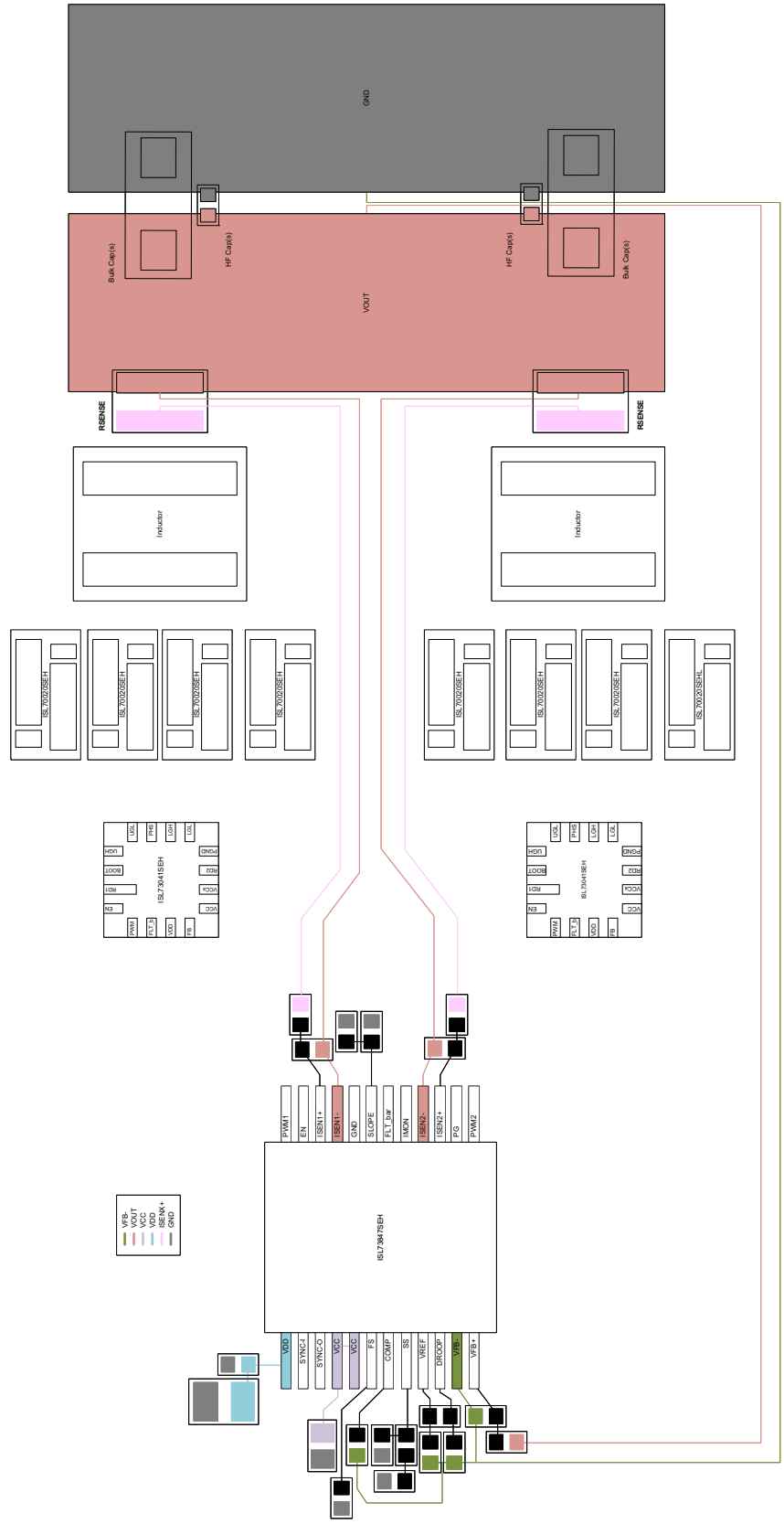


Figure 60. Layout Recommendations

7. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimension	3710µm (146 mils) × 7110µm (280 mils) Thickness: 483µm ±25µm (19 mils ±1 mil)
Interface Materials	
Passivation	Type: Silicon Dioxide and silicon nitride Thickness: 24.5kÅ
Top Metallization	Type: Top metal/Bond Pad Composition 99.5% Al, 0.5%Cu
Backside Finish	Silicon
Process	0.25µm BiCMOS
Assembly Information	
Substrate Potential	Internal connection to GND
Additional Information	
Worst Case Current Density	31.36mA/µm
Transistor Count	268182
Weight of Packaged Device	1.39 grams
Lid Characteristics	Finish: Gold, Potential: Tied to Pin 20

7.1 Metallization Mask Layout

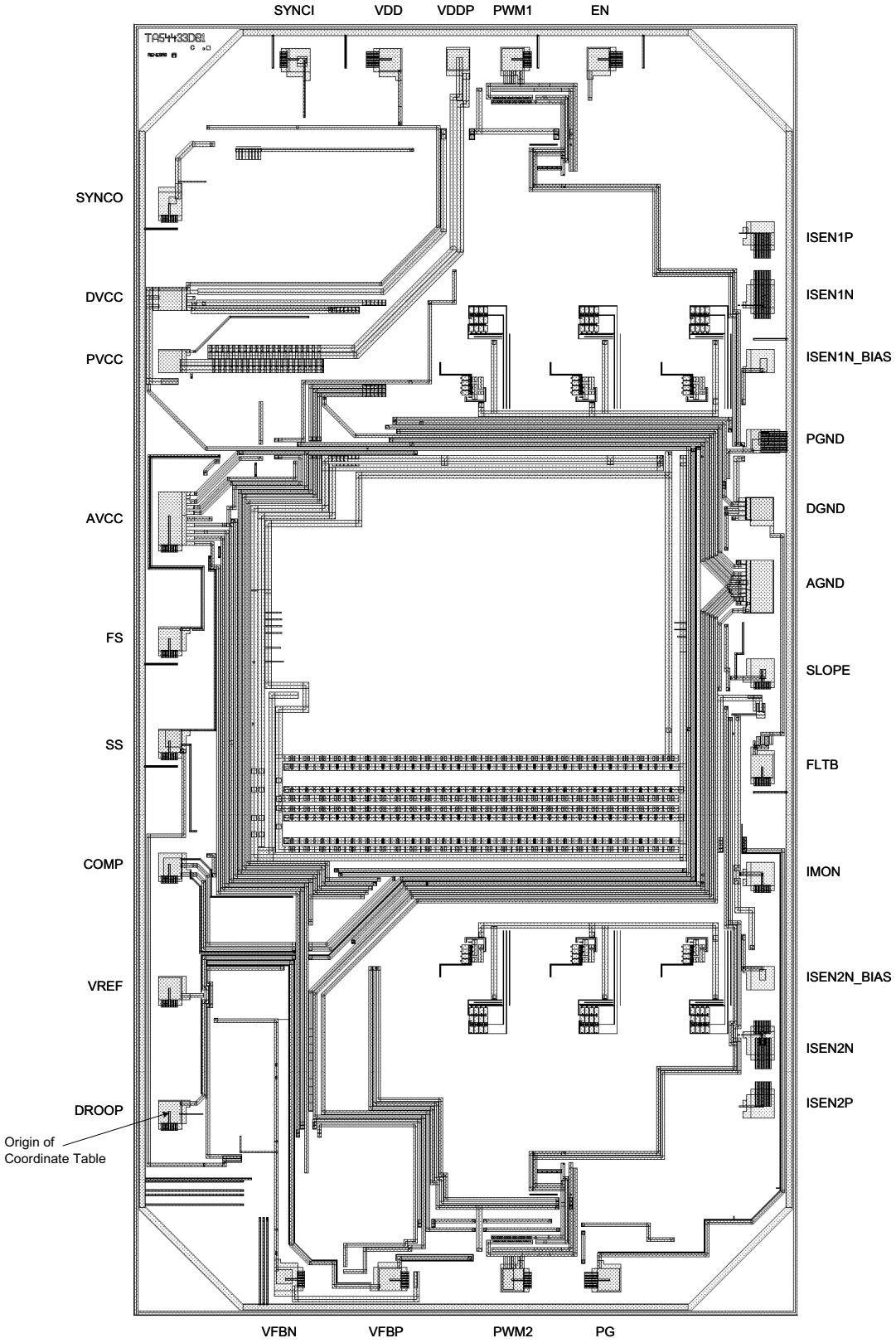


Table 3. Layout X-Y Coordinates (Centroid of Bond Pad)

Pad Name	Pad Number	Pin Number	X-Coordinate (um)	Y-Coordinate (um)	Pad Size X (um)	Pad Size Y (um)	Bond Wire Diameter (0.001”)
VDDP	1	1	1559	5706	117	117	1.25
VDD	2	1	1195	5699	117	117	1.25
SYNCI	3	2	695	5699	117	117	1.25
SYNCO	4	3	0	4924	117	117	1.25
DVCC	5	4	0	4407	117	117	1.25
PVCC	6	5	0	4070	117	117	1.25
AVCC	7	5	0	3216	117	280	1.25
FS	8	6	0	2565	117	117	1.25
SS	9	7	0	2010	117	117	1.25
COMP	10	8	0	1340	117	117	1.25
VREF	11	9	0	670	117	117	1.25
DROOP	12	10	0	0	117	117	1.25
VFBN	13	11	627	-905	117	117	1.25
VFBP	14	12	1191	-905	117	117	1.25
PWM2	15	13	1855	-912	117	117	1.25
PG	16	14	2379	-912	117	117	1.25
ISEN2P	17	15	3211	31	117	117	1.25
ISEN2N	18	16	3211	373	117	117	1.25
ISEN2N_BIAS	19	16	3211	726	117	117	1.25
IMON	20	17	3211	1290	117	117	1.25
$\overline{\text{FLT}}$	21	18	3211	1871	117	117	1.25
SLOPE	22	19	3211	2392	117	117	1.25
AGND	23	20	3211	2848	117	280	1.25
DGND	24	20	3211	3270	117	117	1.25
PGND	25	20	3211	3635	117	117	1.25
ISEN1N_BIAS	27	21	3211	4070	117	117	1.25
ISEN1N	26	21	3211	4421	117	117	1.25
ISEN1P	28	22	3211	4763	117	117	1.25
EN	29	23	2322	5706	117	117	1.25
PWM1	30	24	1855	5706	117	117	1.25

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number[1]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
ISL73847SEHMF	LDR to 75krad(Si)	24 Ld CDFP Packaged Device (QML-V Level Screening)	K24.A	Tray	-55 to +125°C
ISL73847SEHMX[2]	LDR to 75krad(Si)	Bare Die (QML-V Level Screening)	N/A	-	-55 to +125°C
ISL73847SEHF/PROTO[3]	N/A	24 Ld CDFP Packaged Device (For Evaluation Purposes)	K24.A	Tray	-55 to +125°C
ISL73847SEHX/SAMPLE[2][3]	N/A	Bare Die (For Evaluation Purposes)	N/A	-	-55 to +125°C
ISL73847SEHEV2Z[4]	Evaluation Board (For Evaluation Purposes)				

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications. The die is sourced from wafer lots that have been qualified for Group C and Group E per MIL-PRF-38535 (Refer to *R34TB0001: Renesas Radiation Hardened Hermetic Screening and QCI Flow* for more information).
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in this datasheet. The /SAMPLE parts do not receive 100% screening across temperature to the electrical limits. These part types do not come with a Certificate of Conformance.
4. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

10. Revision History

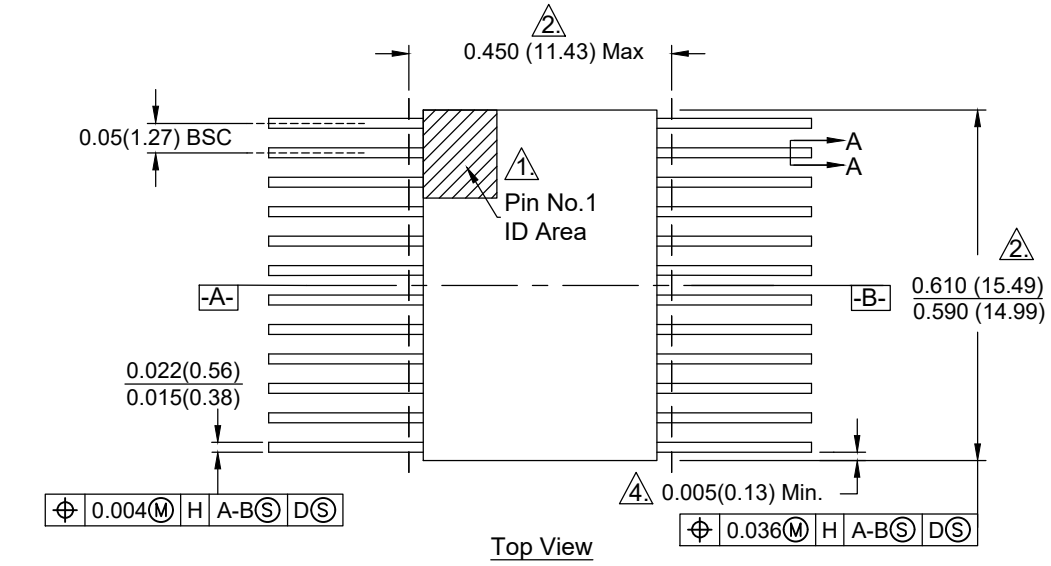
Rev.	Date	Description
2.04	Aug 8, 2025	Updated Page 1 information. Added the Multi-Phase Operation section. Updated the POD to the latest revision, changes are as follows: -Placed into latest format. -Improved dimensional ranges on Package body Length and Width, Package thickness, Package bottom pedestal Width, and lead Length. -Removed references to a lead tab as a pin 1 index corner ID option, since no packages using this outline use a tab on lead 1.
2.03	Nov 14, 2024	Updated Figures 3, 4, and 7. Updated SYNC-I to PWM2 Delay typical from 20ns to 260ns. Updated SYNC-O to PWM2 Delay typical from 150ns to 20ns.
2.02	Jul 24, 2024	Updated Figures 51 and 52 and related text.

Rev.	Date	Description
2.01	Mar 13, 2024	Updated Features section. Updated Figure 5. Updated Pin Descriptions. Updated the maximum spec for ISENSx and VCC (second one) in the abs max section. Updated the ISENx Common Mode Range to 19V. Added Note 2 in the abs max section. Updated minimum spec for PWM Output Switching Frequency in the Recommended Operating Conditions. Updated Current Share between Phase 1 & 2 specification. Updated Figures 20 - 27 and Figures 37 - 43 titles. Minor text updates throughout document. Updated Peak Current Mode Control section. Updated Figure 49. Updated sections 6.1 through 6.9 by updating/removing equations and text throughout.
2.00	Apr 20, 2023	Updated $\overline{FLT}$ Drive current maximum spec from 60mA to 75mA. Updated Droop current -55°C maximum spec from 22µA to 23.5µA. Changed the $g_{m(EA)}$ values on page 32 and 33 from 0.001S to 0.00357S.
1.02	Feb 15, 2023	Added new bullets in the Features section. Updated VCC pin descriptions. Updated Figures 3, 4, and 5. Updated Droop Regulation and Droop Regulation Setting sections. Updated Equations 1, 15, and 17. Updated Note 2 and the package description in the ordering information table.
1.01	Dec 15, 2022	Updated Pin Descriptions table. Updated Absolute Maximum Ratings section adding row 3 and fixing typo in the parameter column for first row.
1.00	Nov 21, 2022	Initial Release

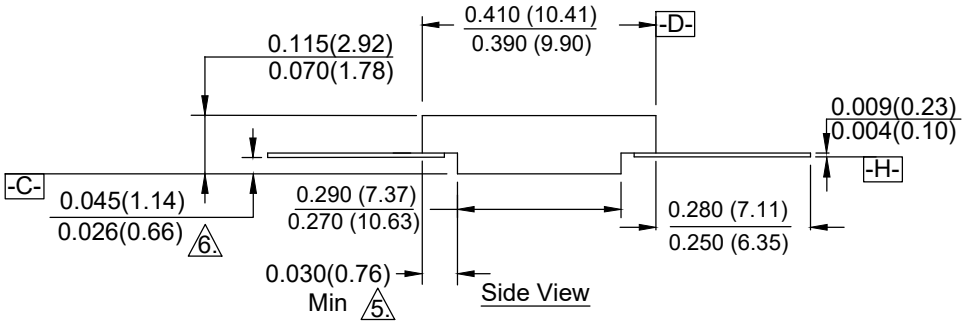
Package Outline Drawing

24 Lead Ceramic Metal Seal Flatpack

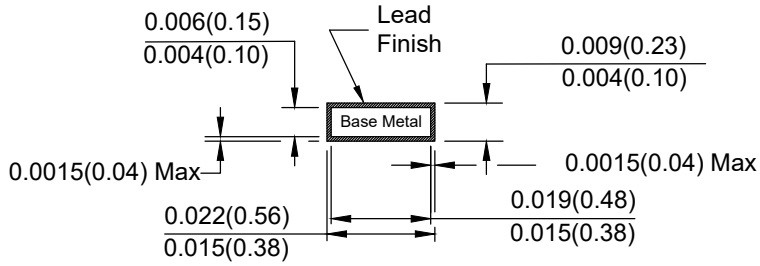
POD No: K24.A, Revision No: 01, Date Created: May12, 2025



Top View



Side View



Section A-A 3.

Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The maximum limits of lead dimensions (SECTION A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. This Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: INCH(mm). Controlling dimension: INCH.
9. Meets MIL-STD-1835 CDFP4-F24 (F-6A, Configuration B).

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