ISL73148SEH

Radiation Hardened 8-Channel 14-Bit 900/480ksps SAR ADC

The ISL73148SEH is a radiation hardened 8-channel high precision 14-bit, 900/480ksps SAR Analog-to-Digital Converter (ADC). The ADC core is preceded by eight analog input channels followed by a buffered 8-to-1 multiplexer and a PGA (Programmable Gain Amplifier). The device features a peak SNR of 82dBFS when operating at 900ksps. With the PGA enabled, sampling rates up to 480ksps are supported. The PGA can be bypassed so that the sample rate increases to 900ksps.

The product features 900/480ksps throughput with no data latency. The device also features excellent linearity and dynamic accuracy. The ISL73148SEH offers a high-speed SPI-compatible serial interface that supports logic ranging from 2.2V to 3.6V using a separate digital I/O supply pin.

The ISL73148SEH offers a separate low power mode (LPM) pin that reduces power dissipation at lower sample rates. The analog input signal range is determined by an external reference with a supported input range of 2.4V to 2.6V.

The ISL73148SEH operates across the military temperature range from -55°C to +125°C and is available in a 28 Ld hermetically sealed Ceramic Dual Flat-Pack (CDFP) package.

Applications

- Precision signal processing in satellite payloads
- Satellite telemetry systems
- Satellite propulsion and orbit control
- Attitude control of satellites
- High-end industrial and down-hole drilling

Features

- Qualified to Renesas Rad Hard QML-V Equivalent Screening and QCI Flow (R34TB0001EU)
- All screening and QCI is in accordance with MIL-PRF-38535L Class-V
- 8 Buffered analog input channels with multiplexer
- Bypassable PGA with selectable gain ($1 \le G \le 16$)
- Pseudo-differential bipolar and unipolar operation
- Channel scan sequencer
- Full throughput rate with no data latency
- Excellent linearity: ±0.5 LSB DNL, ±1.5 LSB INL
- Low noise: 83dBFS (PGA bypassed), 77dBFS SNR (PGA Gain = 2)
- 5V AV_{CC} supply and 2.5V/3.3V DV_{CC} supply
- Analog input impedance: >1GΩ, 3pF
- Wide 50MHz -3dB input bandwidth
- Low power mode operation at lower sample rates
- High speed SPI-compatible serial I/O
- Full military temperature range operation
  - T_A = -55°C to +125°C
- TID Rad Hard Assurance (RHA) testing
  - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE hardness (see SEE report for details)
  - No DSEE for AV_{CC} = 6.4V, DV_{CC} = 4.6V, and V_{REF} = 3.6V at 86MeV•cm^2/mg
  - SEFI <2.5µm^2 at 86MeV•cm^2/mg

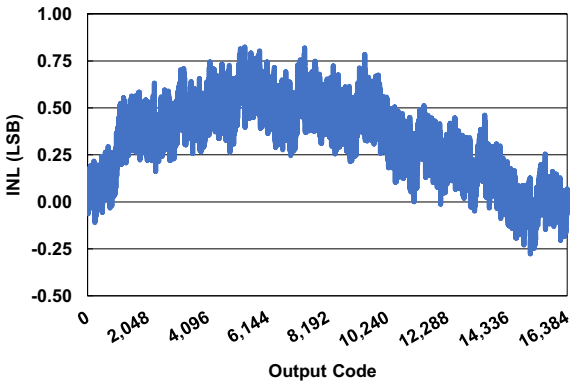


Figure 1. INL vs Output Code

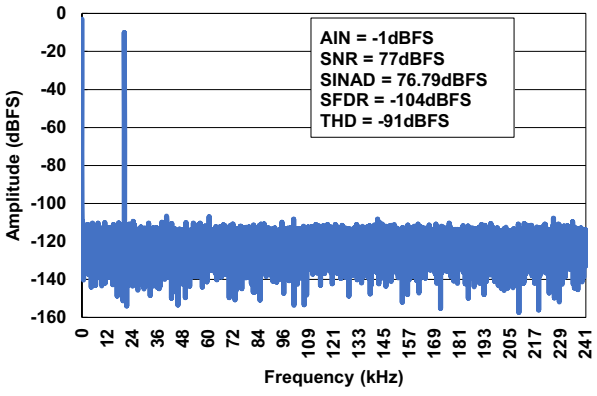


Figure 2. FFT - 20.3kHz

Contents

1. Overview

1.1 Typical Application Schematic

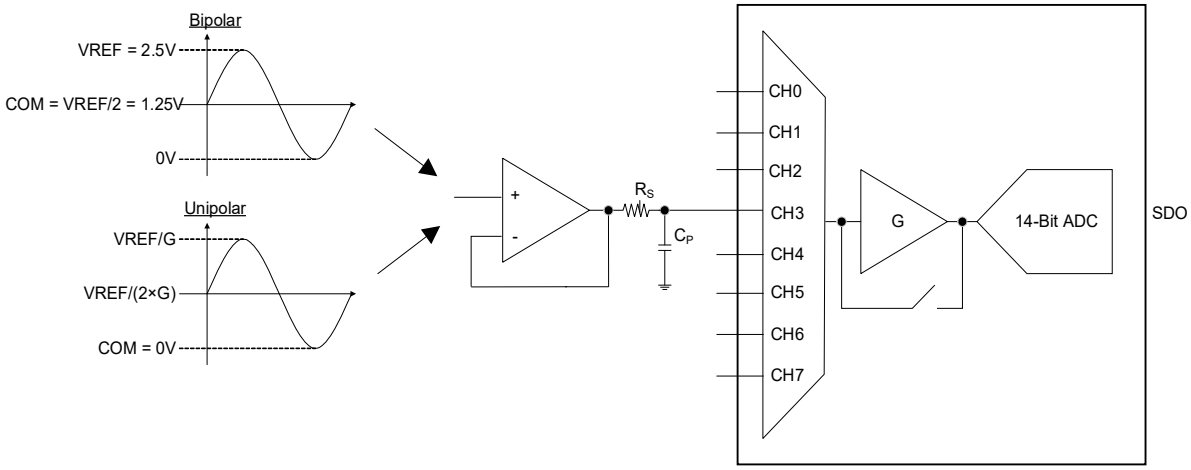


Figure 3. Typical Application Example Circuit

1.2 Functional Block Diagram

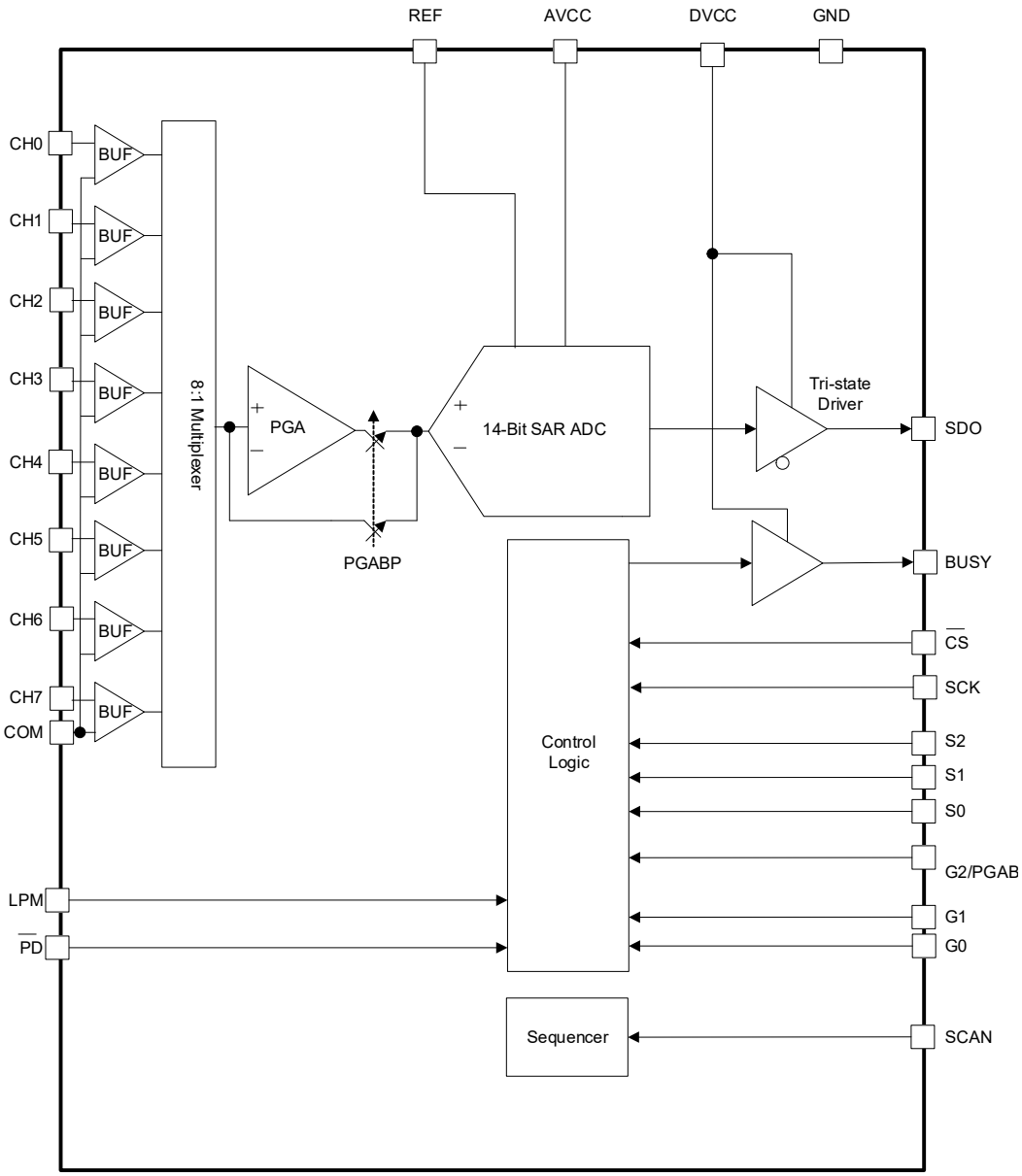
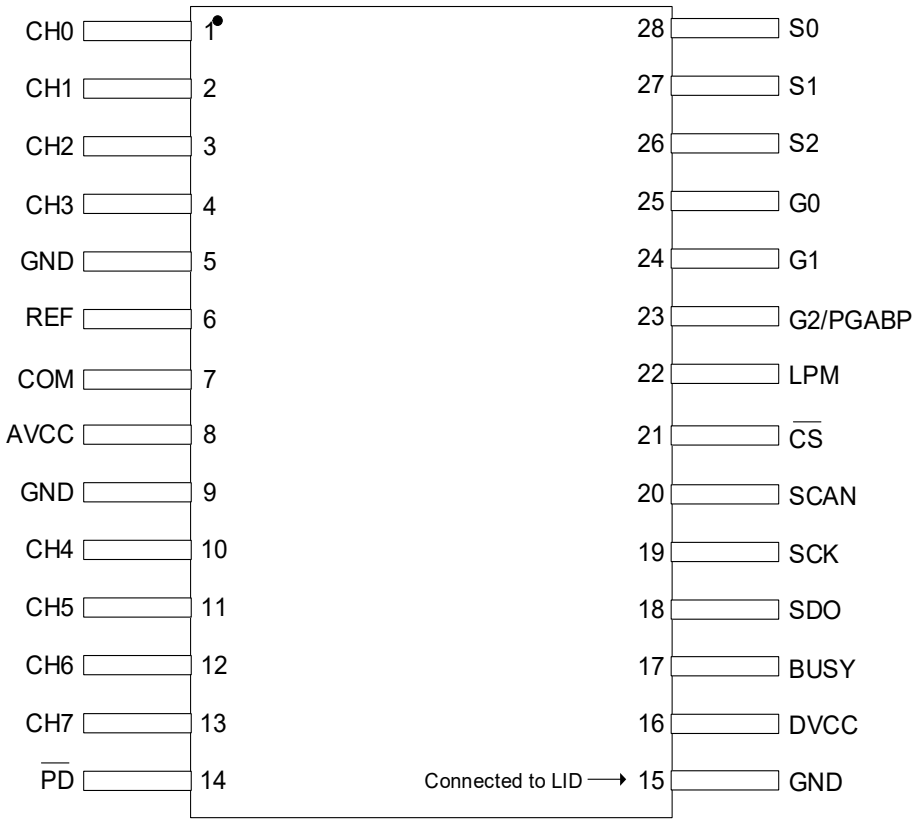


Figure 4. ISL73148SEH Block Diagram

2. Pin Information

2.1 Pin Configuration



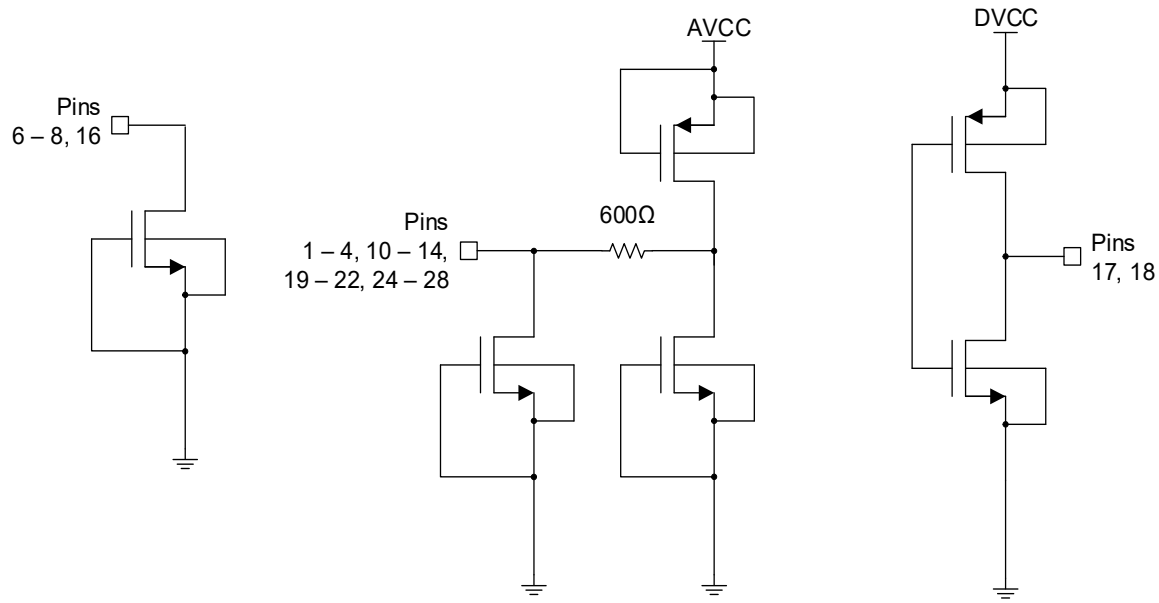
Top View

2.2 Pin Descriptions

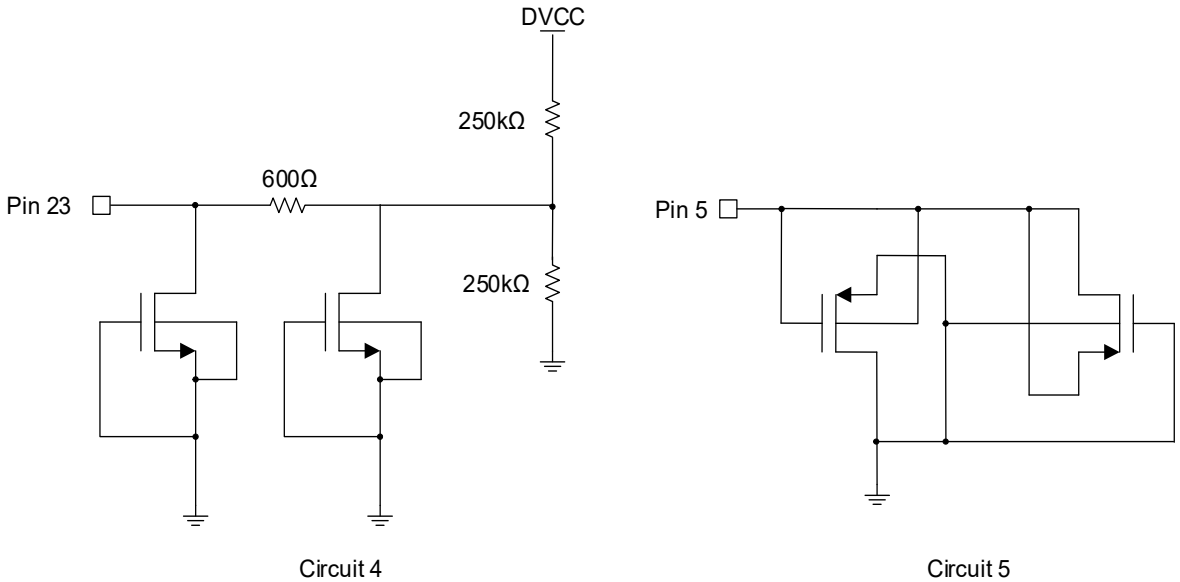
Pin Number	Pin Name	ESD Circuit	Description
5, 9, 15	GND	-	Analog and digital supply ground. Tie directly to the PCB ground plane (GND). Pin 15 is electrically tied to the package lid.
8	AVCC	1	Analog supply. The supply range is 4.5V to 5.5V. Bypass this pin to GND with a 10µF ceramic capacitor.
6	REF	1	Reference Input. The input range of REF is 2.4V to 2.6V. The voltage at the REF pin (V_{REF}) defines the input range of each Analog Input Channel as 0V to V_{REF}. Bypass REF to GND with a 10µF ceramic capacitor.
1, 2, 3, 4, 10, 11, 12, 13	CH0, CH1, CH2, CH3, CH4, CH5, CH6, CH7	2	Analog input channels. CH0 to CH7 are eight single-ended analog input channels. Each input channel pin may be driven within the voltage range from 0V to V_{REF}.
7	COM	1	Common input. This is the reference voltage for all single-ended analog input channels. Connect to GND for unipolar (unsigned) conversions. For bipolar (signed) conversions, the COM pin will output a voltage equal to $V_{REF}/2$ and requires bypassing to GND with a 0.1µF ceramic capacitor. This pin is referenced to VREF. This pin is a device configuration pin and should not be switched dynamically during operation.

Pin Number	Pin Name	ESD Circuit	Description
14	$\overline{PD}$	2	Power-down low input. When this pin is a logic low, the ADC enters power-down mode. If this occurs during a conversion, the conversion is halted, and the SDO pin is placed in Hi-Z. Logic levels are determined by DV_{CC}. This pin has an internal 500kΩ pull-up resistor to DV_{CC}.
16	DVCC	1	Digital I/O supply. The voltage range on this pin is 2.2V to 3.6V. DV_{CC} is nominally set to the same supply voltage as the host interface (2.5V or 3.3V). Bypass DVCC to GND with a 0.1µF capacitor.
17	BUSY	3	Busy output. A logic high indicates a conversion is in progress. The BUSY indicator returns low following the completion of a conversion. Logic levels are determined by DV_{CC}.
18	SDO	3	Serial data output. The current conversion result is serially shifted out on this pin on the rising edges of SCK, MSB first to LSB last. The data stream is composed of 14 bits of conversion data followed by the channel select and gain select bits corresponding to the conversion result. When the COM pin is floated and bypassed to ground with a 0.1µF ceramic capacitor the data format will be in bipolar (signed) format. When the COM pin is grounded the data format is unipolar (unsigned). Logic Levels are determined by DV_{CC}.
19	SCK	2	Serial data clock input. When $\overline{CS}$ is low and the BUSY indicator is low, the conversion result is shifted out on SDO on the rising edges of SCK, Most Significant Bit (MSB) first to Least Significant Bit (LSB) last. Logic levels are determined by DV_{CC}. SCK should be held low when it is not being asserted.
20	SCAN	2	Channel scan input. When this input is logic high, the internal sequencer controls the channel selected. CH0 is the first channel selected following the rising edge of SCAN. Each subsequent channel is selected on each new rising edge of $\overline{CS}$. Logic levels are determined by DV_{CC}.
21	$\overline{CS}$	2	Convert Start Low input. A falling edge on this input completes the sampling process and starts a new conversion. The conversion is timed using an internal oscillator. The device automatically powers down following the conversion process. The logic state of the $\overline{CS}$ pin controls the state of the SDO pin. A logic high on the $\overline{CS}$ pin disables the SDO pin driver and the SDO pin impedance is Hi-Z. A logic low on the $\overline{CS}$ pin enables the SDO driver (unless $\overline{PD}$ is low) and allows data to be read out following a conversion. This pin should be held low at power-up and when in power-down or when the device is inactive.
22	LPM	2	Low power mode input. When this input is logic high, the acquisition time is directly controlled by the $\overline{CS}$ pin logic state held high. The ADC is automatically powered down between conversions to reduce power consumption for lower sample rates. This pin is a device configuration pin and should not be switched dynamically during operation.
23, 24, 25	G2/PGABP, G1, G0	2 (Pin 23 uses ESD circuit 4)	Gain selection logic inputs. These three pins program the gain of the PGA. The G2, G1, and G0 logic inputs are latched internally on the rising edge of $\overline{CS}$. The G2/PGABP pin should be left floating and bypassed to GND with a 100pF capacitor to bypass the PGA. When the PGA is bypassed, the maximum throughput rate is increased to approximately 900ksps. When using the G2/PGABP pin to bypass the PGA the pin should not be switched dynamically during operation and should be driven to a static value to set the configuration of the PGA. When using the G2/PGABP pin to configure gain settings, it is safe to switch the pin dynamically during operation as long as timing requirements are met. Logic levels are determined by DV_{CC}.
26, 27, 28	S2, S1, S0	2	Channel selection logic inputs. These three pins select the input channel passed through the input multiplexer to the PGA (or ADC if the PGA is bypassed). The S2, S1, and S0 logic inputs are latched internally on the rising edge of $\overline{CS}$. Logic levels are determined by DV_{CC}.

Pin Number	Pin Name	ESD Circuit	Description
LID	N/A	N/A	Package Lid is internally connected to GND through Pin 15.



Circuit 1 Circuit 2 Circuit 3



Circuit 4 Circuit 5

Equivalent Input Circuits

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Min	Max	Unit
Supply Voltage (AV_{CC}, DV_{CC})	-0.3	6.4	V
Supply Voltage (AV_{CC})[1]	-0.3	6.3	V
Supply Voltage (DV_{CC})[1]	-0.3	4.6	V
REF	-0.3	3.6	V
REF[1]	-0.3	3.6	V
CH0-CH7	-0.3	AV_{CC} + 0.3	V
CH0-CH7 Input Current[2]	-3	3	mA
Digital Input Voltage ($\overline{PD}$, $\overline{CS}$, SCK, S2, S1, S0, G2, G1, G0, LPM, SCAN)	-0.3	DV_{CC} + 0.3	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2.5	kV
Charged Device Model (Tested per JS-002-2018)	-	750	V

1. Tested in a heavy ion environment at LET = 86MeV•cm^2/mg at 125°C.
2. When an input voltage transient exceeds maximum operating conditions (voltage at the channel input pins less than GND or greater than AVCC), limit the input current to less than ±3mA.

3.2 Recommended Operating Conditions

Parameter	Min	Max	Unit
Temperature	-55	+125	°C
Analog Supply Voltage, A_{VCC}	4.5	5.5	V
Digital Supply Voltage, D_{VCC}	2.2	3.6	V
Reference Input Voltage, V_{REF}	2.4	2.6	V
Reference Input Ground (RGND)[1]	0	0	V
Analog Input Voltage, A_{IN}	0	V_{REF}	V

1. Reference input ground (RGND) must be tied directly to GND plane.

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
CDFP Package K28.A	25	3.5

1. θ_{JA} is measured in free air with the component on high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

3.4 Electrical Specifications

3.4.1 Normal Operating Mode

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, all channels, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Converter Characteristics						
Resolution	-	-	**14**	-	-	bits
No Missing Codes	-	-	**14**	-	-	bits
Transition Noise		RMS noise, 14-bit LSB	-	0.5	-	LSB_{RMS}
Integral Non-Linearity	INL	Measured with full-scale input signal.[3]	**-1.2**	-0.3/+0.8	**2.0**	LSB
Differential Non-Linearity	DNL	Measured with full-scale input signal.**[3]**	**-0.6**	±0.3	**0.6**	LSB
Zero-Scale Error	VOFF	Measured with input set to V_{REF}/2.	**-26.5**	±5	**23**	LSB
		PGA bypassed. Measured with input set to V_{REF}/2.	**-13**	±5	**13**	LSB
Zero-Scale Error Drift	VOFFD	Measured with input set to V_{REF}/2.	-	±0.03	-	LSB/°C
		PGA bypassed. Measured with input set to V_{REF}/2.	-	±0.015	-	LSB/°C
Zero-Scale Error Match	VOFFM	Measured with input set to V_{REF}/2.	-6	±3	6	LSB
		PGA bypassed. Measured with input set to V_{REF}/2.	-16.5	-8/+6	14	LSB
Positive Full-Scale Error	+FSE	Measured with input connected to VREF.	**-33**	±5	**26**	LSB
		PGA bypassed. Measured with input connected to VREF.	**-13.5**	-2/+3	**19.5**	LSB
Positive Full-Scale Error Drift	+FSED	Measured with input connected to VREF.	-	±0.03	-	LSB°C
		PGA bypassed. Measured with input connected to VREF.	-	±0.01	-	LSB/°C
Positive Full-Scale Error Match	+FSEM	Measured with input connected to VREF.	-8	±1.5	8	LSB
		PGA bypassed. Measured with input connected to VREF.	-16.5	-7/+6	14	LSB
Negative Full-Scale Error	-FSE	Measured with input connected to GND.	**-33**	±5	**26**	LSB
		PGA bypassed. Measured with input connected to GND.	**-23.5**	±1	**10.5**	LSB
Negative Full-Scale Error Drift	-FSED	Measured with input connected to GND.	-	±0.03	-	LSB/°C
		PGA bypassed. Measured with input connected to GND.	-	±0.01	-	LSB/°C
Negative Full-Scale Error Match	-FSEM	Measured with input connected to GND.	-8	±2	8	LSB
		PGA bypassed. Measured with input connected to GND.	-16.5	-7/+6	14	LSB

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, all channels, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Dynamic Accuracy						
Signal to Noise Ratio	SNR	PGA Bypassed, f_{SAMP} = 900.901ksps, Ain = -7dBFS	**80**	83	-	dBFS
		PGA Gain = 2	**75**	77	-	dBFS
		PGA Gain = 16	**58.5**	61.2	-	dBFS
Signal to Noise + Distortion Ratio	SINAD	PGA Bypassed, f_{SAMP} = 900.901ksps, Ain = -7dBFS	**79**	82.5	-	dBFS
		PGA Gain = 2	**74**	76.6	-	dBFS
		PGA Gain = 16	**57.5**	61.2	-	dBFS
Effective Number of Bits	ENOB	PGA Bypassed, f_{SAMP} = 900.901ksps, Ain = -7dBFS	**12.8**	13.4	-	bits
		PGA Gain = 2	**11.8**	12.4	-	bits
		PGA Gain = 16	**9.1**	9.9	-	bits
Total Harmonic Distortion	THD	PGA Bypassed, f_{SAMP} = 900.901ksps, Ain = -7dBFS	**85**	92	-	dBFS
		PGA Gain = 2	**83**	89	-	dBFS
		PGA Gain = 16	**80**	90	-	dBFS
Spurious Free Dynamic Range	SFDR	PGA Bypassed, f_{SAMP} = 900.901ksps, Ain = -7dBFS	**90**	95	-	dBFS
		PGA Gain = 2	**90**	95	-	dBFS
		PGA Gain = 16	-	93	-	dBFS
Channel-to-Channel Isolation		F_{IN} = 20.3kHz, PGA gain = 1, full-scale signal applied to one channel, other channels connected to GND	-	-100	-	dB
Input Bandwidth		Source impedance = 50Ω, -3dB point	-	50	-	MHz
Aperture Delay	t_{AD}	$\overline{CS}$ falling edge to sample edge	-	2.5	-	ns
Aperture Jitter	$t_{AJITTER}$	-	-	5	-	ps_{RMS}
Power Supply Characteristics (AVCC, DVCC)						
Analog Supply Voltage	AV_{CC}	-	**4.5**	-	**5.5**	V
Analog Supply Current - Active	I_{AVCC}	Active, PGA enabled, f_{SAMP} = 483.092ksps	-	17.6	**20.5**	mA
		Active, PGA bypassed, f_{SAMP} = 900ksps	-	18.1	**23**	mA
Analog Supply Current - Static	I_{Static}	PGA enabled. $\overline{CS}$ held Low	-	10.6	**13**	mA
		PGA bypassed. $\overline{CS}$ held Low	-	7.3	**9**	mA
Analog Supply Current - Sleep	I_{SLAVCC}	$\overline{PD}$ held Low	-	20	-	µA
Digital Supply Voltage	DV_{CC}	-	**2.2**	-	**3.6**	V
Digital Supply Current - Active	I_{DVCC}	PGA enabled. f_{SCK} = 50MHz	-	340	**600**	µA
		PGA bypassed. f_{SCK} = 50MHz	-	495	**700**	µA

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, all channels, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Digital Supply Current - Static	I_{STDVCC}	PGA enabled. $\overline{CS}$ held Low	-	90	**110**	µA
		PGA bypassed. $\overline{CS}$ held Low	-	64	**80**	µA
Digital Supply Current - Sleep	I_{SLDVCC}	$\overline{PD}$ held Low	-	6	-	µA
P_D	P_{ACTIVE}	PGA enabled, f_{SAMP} = 483.092ksps	-	89	**104**	mW
		PGA bypassed, f_{SAMP} = 900.901ksps	-	92	**117**	mW
	P_{STATIC}	PGA enabled, $\overline{CS}$ held Low	-	55	**65**	mW
		PGA bypassed, $\overline{CS}$ held Low	-	38	**45**	mW
	P_{SLEEP}	$\overline{PD}$ held Low	-	115	-	µW

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed. Values derived from +25°C median data.
3. Characterized on all channels, production tested on Channel 0 only.

3.4.2 Low Power Mode

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 2.5V, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, all channels, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Converter Characteristics						
Resolution	-	-	**14**	-	-	bits
No Missing Codes	-	-	**14**	-	-	bits
Transition Noise		RMS noise, 14-bit LSB	-	0.3	-	LSB_{RMS}
Integral Non-Linearity	INL	Measured with full scale input signal.[3]	**-1.2**	-0.3/+0.8	**2.0**	LSB
Differential Non-Linearity	DNL	Measured with full scale input signal.[3]	**-0.6**	±0.3	**0.6**	LSB
Zero-Scale Error	VOFF	Measured with input set to V_{REF}/2.	**-29**	±5	**17**	LSB
		PGA bypassed. Measured with input set to V_{REF}/2.	**-13**	±5	**13**	LSB
Zero-Scale Error Drift	VOFFD	Measured with input set to V_{REF}/2.	-	±0.03	-	LSB/°C
		PGA bypassed. Measured with input set to V_{REF}/2.	-	±0.01	-	LSB/°C
Zero-Scale Error Match	VOFFM	Measured with input set to V_{REF}/2.	-6.5	±3	6.5	LSB
		PGA bypassed. Measured with input set to V_{REF}/2.	-16.5	-8/+6	14	LSB
Positive Full-Scale Error	+FSE	Measured with input connected to VREF.	**-34**	±5	**22.5**	LSB
		PGA bypassed. Measured with input connected to VREF.	**-13.5**	±1	**18.5**	LSB

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 2.5V, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, all channels, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Positive Full-Scale Error Drift	+FSED	Measured with input connected to VREF.	-	±0.01	-	LSB/°C
		PGA bypassed. Measured with input connected to VREF.	-	±0.01	-	LSB/°C
Positive Full-Scale Error Match	+FSEM	Measured with input connected to VREF.	-8.5	±1.5	8.5	LSB
		PGA bypassed. Measured with input connected to VREF.	-16	-7/+6	14	LSB
Negative Full-Scale Error	-FSE	Measured with input connected to GND.	**-40**	-9/+1	**18**	LSB
		PGA bypassed. Measured with input connected to GND.	**-22.5**	±1	**11**	LSB
Negative Full-Scale Error Drift	-FSED	Measured with input connected to GND.	-	±0.03	-	LSB/°C
		PGA bypassed. Measured with input connected to GND.	-	±0.01	-	LSB/°C
Negative Full-Scale Error Match	-FSEM	Measured with input connected to GND.	-8.5	±1.5	8.5	LSB
		PGA bypassed. Measured with input connected to GND.	-16	-7/+6	14	LSB
Dynamic Accuracy						
Signal to Noise Ratio	SNR	PGA Bypassed, f_{SAMP} = 683.932ksps, Ain = -7dBFS	**80**	83	-	dBFS
		PGA Gain = 2	**75**	77	-	dBFS
		PGA Gain = 16	**58.0**	61.1	-	dBFS
Signal to Noise + Distortion Ratio	SINAD	PGA Bypassed, f_{SAMP} = 684.932ksps, Ain = -7dBFS	**79**	82.5	-	dBFS
		PGA Gain = 2	**74**	76.6	-	dBFS
		PGA Gain = 16	**57.0**	61.2	-	dBFS
Effective Number of Bits	ENOB	PGA Bypassed, f_{SAMP} = 684.932ksps, Ain = -7dBFS	**12.8**	13.4	-	bits
		PGA Gain = 2	**11.8**	12.4	-	bits
		PGA Gain = 16	**9.1**	9.9	-	bits
Total Harmonic Distortion	THD	PGA Bypassed, f_{SAMP} = 684.932ksps, Ain = -7dBFS	**85**	92	-	dBFS
		PGA Gain = 2	**83**	89	-	dBFS
		PGA Gain = 16	**80**	90	-	dBFS
Spurious Free Dynamic Range	SFDR	PGA Bypassed, f_{SAMP} = 684.932ksps, Ain = -7dBFS	**90**	95	-	dBFS
		PGA Gain = 2	**90**	95	-	dBFS
		PGA Gain = 16	-	93	-	dBFS
Channel-to-Channel Isolation	-	F_{IN} = 20.3kHz, PGA gain = 1, full-scale signal applied to one channel, other channels connected to GND	-	-100	-	dB

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 2.5V, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, all channels, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Input Bandwidth	-	Source impedance = 50Ω, -3dB point	-	50	-	MHz
Aperture Delay	t_{AD}	$\overline{CS}$ falling edge to sample edge	-	2.5	-	ns
Aperture Jitter	$t_{AJITTER}$	-	-	5	-	ps_{RMS}
Power Supply Characteristics (AVCC, DVCC)						
Analog Supply Voltage	AV_{CC}	-	**4.5**	-	**5.5**	V
Analog Supply Current - Active	I_{AVCC}	Active, PGA enabled, f_{SAMP} = 413.223ksps	-	14.3	**16.9**	mA
		Active, PGA bypassed, f_{SAMP} = 670ksps	-	15	**17.5**	mA
Analog Supply Current - Static	I_{Static}	PGA enabled. $\overline{CS}$ held Low	-	6	**7.5**	mA
		PGA bypassed. $\overline{CS}$ held Low	-	6	**7.5**	mA
Analog Supply Current - Sleep	I_{SLAVCC}	$\overline{PD}$ held Low	-	20	-	µA
Digital Supply Voltage	DV_{CC}	-	**2.2**	-	**3.6**	V
Digital Supply Current - Active	I_{DVCC}	PGA enabled. f_{SCK} = 50MHz	-	360	**600**	µA
		PGA bypassed. f_{SCK} = 50MHz	-	490	**700**	µA
Digital Supply Current - Static	I_{STDVCC}	PGA enabled. $\overline{CS}$ held Low	-	110	**130**	µA
		PGA bypassed. $\overline{CS}$ held Low	-	80	**110**	µA
Digital Supply Current - Sleep	I_{SLDVCC}	$\overline{PD}$ held Low	-	6	-	µA
P_D	P_{ACTIVE}	PGA enabled, f_{SAMP} = 413.223ksps	-	72.5	**86**	mW
		PGA bypassed, f_{SAMP} = 684.932ksps	-	76.25	**89**	mW
	P_{STATIC}	PGA enabled, $\overline{CS}$ held Low	-	30	**38**	mW
		PGA bypassed, $\overline{CS}$ held Low	-	30	**38**	mW
	P_{SLEEP}	$\overline{PD}$ held Low	-	115	-	µW

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed. Values derived from +25°C median data.
3. Characterized on all channels, production tested on Channel 0 only.

3.4.3 Channel Input Specifications

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, T_A = 25°C, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Channel Input Characteristics (CH0 to CH7)						
Input Voltage Range		Unipolar, COM pin grounded	**-0.1**	-	**V_{REF}/GAIN + 0.1**	V
		Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**V_{REF}/2 - (V_{REF}/2)/GAIN**	-	**V_{REF}/2 + (V_{REF}/2)/GAIN**	V

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, T_A = 25°C, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Input Differential Range (CH0:CH7 to COM)	-	Unipolar, COM pin grounded	**0**	-	**V_{REF}/GAIN**	V
		Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**(-V_{REF}/2)/GAIN**	-	**(V_{REF}/2)/GAIN**	V
Input Leakage Current	IA_{IN}	-	**-1**	-	**1**	µA
Input Capacitance	C_{IN}	-	-	3	-	pF
Input Resistance	R_{IN}	-	-	1	-	GΩ
PGA Gain Accuracy	-	Gain = 1, G2:G0 = '000', Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-0.3**	-0.15	**0.4**	%
		Gain = 2, G2:G0 = '001' Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-0.3**	-0.02	**0.4**	%
		Gain = 3, G2:G0 = '010' Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-0.3**	-0.02	**0.4**	%
		Gain = 4, G2:G0 = '011' Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-0.3**	-0.01	**0.4**	%
		Gain = 6, G2:G0 = '100' Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-0.8**	-0.08	**0.35**	%
		Gain = 8, G2:G0 = '101' Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-0.8**	-0.17	**0.35**	%
		Gain = 12, G2:G0 = '110' Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-1**	-0.32	**0.2**	%
		Gain = 16, G2:G0 = '111' Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor	**-1**	-0.46	**0.2**	%

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed. Values derived from +25°C median data.

3.4.4 I/O Specifications

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, T_A = 25°C, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Digital Inputs and Outputs ($\overline{PD}$, $\overline{CS}$, SCK, BUSY, SDO, LPM, S2, S1, S0, G2/PGABP, G1, G0, SCAN)						
High Level Input	V_{IH}	DV_{CC} = 2.2V to 3.6V	**0.8×DV_{CC}**	-	-	V
Low Level Input	V_{IL}	DV_{CC} = 2.2V to 3.6V	-	-	**0.2×DV_{CC}**	V
Input Current ($\overline{CS}$, SCK, S2, S1, S0, G1, G0, SCAN)	I_{IN}	V_{IN} = 0V to DV_{CC}	**-1**	-	**1**	µA
Input Capacitance	C_{IN}	-	-	5	-	pF
High Level Output	V_{OH}	DV_{CC} - Output, I_O = -500µA	**DV_{CC} - 0.2**	-	-	V
Low Level Output	V_{OL}	I_O = 500µA	-	-	**0.2**	V
Output Source Current	I_{SRC}	V_{OUT} = 0V to DV_{CC}	-	-10	-	mA
Output Sink Current	I_{SNK}	V_{OUT} = 0V to DV_{CC}	-	10	-	mA
Hi-Z Output Leakage Current	I_{OZ}	V_{OUT} = 0V to DV_{CC}	**-1**	-	**1**	µA
$\overline{PD}$ Input Resistance	R_{INPDL}	Internal pull-up resistance to D_{VCC}	**400**	500	**600**	kΩ
LPM Input Resistance	R_{INLPM}	Internal pull-down resistance to GND	**400**	500	**600**	kΩ
G2/PGABP Input Resistance	R_{ING2BP}	Internal resistor divider between DV_{CC} and GND	**180**	250	**320**	kΩ
COM Pin Characteristics						
COM Input Voltage	V_{ICOM}	Unipolar.	**-0.1**	0	**0.1**	V
COM Output Voltage	V_{OCOM}	Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor.	V_{REF}/2 - 0.002	V_{REF}/2	V_{REF}/2 + 0.002	V
COM Input Resistance	R_{INCOM}	COM pin bypassed to ground with 0.1µF ceramic capacitor	-	100	-	Ω
COM Input Resistance	R_{INCOM}	COM pin driven to GND	**80**	100	**120**	kΩ
Reference Input Characteristics (REF)						
REF Input Voltage Range	V_{REF}	-	**2.4**	2.5	**2.6**	V
REF Input Current	I_{REF}	-	-	300	**400**	µA

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed. Values derived from +25°C median data.

3.4.5 Operation Burn-In Deltas

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, f_{SAMP} = 483.092ksps (Normal Mode) and 395ksps (Low Power Mode), A_{IN} = -1dBFS; T_A = +25°C, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V (Normal Mode) and LPM = 2.5V (Low Power Mode), S2, S1, and S0 = 0V (Channel 0 selected); unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Integral Non-Linearity	INL	Measured with full scale input signal	-0.6	0.6	LSB
Signal to Noise Ratio	SNR	F_{IN} = 20.3kHz	-1	1	dBFS
Effective Number of Bits	ENOB	F_{IN} = 20.3kHz	-0.2	0.2	bits

3.4.6 Low Dose Rate Post Radiation Characteristics

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, f_{SAMP} = 483.092ksps, A_{IN} = -1dBFS; T_A = +25°C, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2; unless otherwise noted. **This data is post radiation exposure over a total ionizing dose of 75krad(Si) with a low dose rate of <0.01rad(Si)/s. This data is intended to show parameter shifts because of low dose rate radiation.**

Parameter	Symbol	Test Conditions	Min	Max	Unit
COM Output Voltage	V_{OCOM}	Bipolar, COM pin bypassed to ground with 0.1µF ceramic capacitor.	$V_{REF}/2$ - 0.003	$V_{REF}/2$ + 0.003	V
Zero-Scale Error Match	VOFFM	Measured with input set to $V_{REF}/2$. Normal mode; LPM = 0V	-10	10	LSB
		Measured with input set to $V_{REF}/2$. Normal mode; LPM = DV_{CC}	-10	10	LSB
Positive Full-Scale Error Match	+FSEM	Measured with input connected to VREF. Normal mode; LPM = 0V	-11	11	LSB
		Measured with input connected to VREF. Normal mode; LPM = DV_{CC}	-11	11	LSB
Negative Full-Scale Error Match	-FSEM	Measured with input connected to GND. Normal mode; LPM = 0V	-11	11	LSB
		Measured with input connected to GND. Normal mode; LPM = DV_{CC}	-11	11	LSB

3.5 Timing Specifications

3.5.1 Normal Operating Mode

AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min [1]	Typ[2]	Max[1]	Unit
Timing Characteristics						
Maximum Sampling Frequency	f_{SAMP}	PGA Bypassed	-	-	**900.901**	kHz
		PGA Enabled	-	-	**483.092**	kHz
Conversion Time	t_{CONV}	BUSY Output High Time, PGA Bypassed	-	-	**660**	ns
		BUSY Output High Time, PGA Enabled	-	-	**1550**	ns

AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min [1]	Typ[2]	Max[1]	Unit
$\overline{CS}$ High Time	t_{CSH}	-	**150**	-	-	ns
SCK Held Low to $\overline{CS}\downarrow$	t_{QUIET}	-	**150**	-	-	ns
$\overline{CS}\downarrow$ to BUSY↑	t_{BUSYLH}	PGA enabled, C_L = 10pF	-	-	**100**	ns
$\overline{CS}\downarrow$ to BUSY↑	t_{BUSYLH}	PGA bypassed, C_L = 10pF	-	-	**30**	ns
SCK Period	t_{SCK}	-	**20**	-	-	ns
SCK High Time	t_{SCKH}	-	**8**	-	-	ns
SCK Low Time	t_{SCKL}	-	**8**	-	-	ns
SDO Data Valid Delay from BUSY↓	$t_{DBUSYLSDOV}$	C_L = 10pF	-	-	**0**	ns
SDO Data Valid Delay from SCK↑	$t_{DSCKSDOV}$	C_L = 10pF	-	-	**20**	ns
SDO Data Valid Hold Time from SCK↑	t_{HSDOV}	C_L = 10pF	**7**	-	-	ns
SDO Bus Acquisition Time from $\overline{CS}\downarrow$	$t_{DCSLSDOL}$	C_L = 10pF	-	-	**25**	ns
SDO Bus Relinquish Time after $\overline{CS}\uparrow$	$t_{DCSHSDOZ}$	C_L = 10pF	-	-	**25**	ns
G2:0, S2:0 to $\overline{CS}\uparrow$	$t_{SUDIGCSH}$	Setup time for gain and channel select bits.	**5**	-	-	ns
G2:0, S2:0 from $\overline{CS}\uparrow$	$t_{HDIGCSH}$	Hold time for gain and channel select bits	**25**	-	-	ns
SCAN to $\overline{CS}\uparrow$	$t_{SCANCSH}$	Setup time for SCAN input.	**20**	-	-	ns
Wake-Up time from Power-Down Mode	t_{WAKE}	Time to wait after $\overline{PD}\uparrow$ to first sample	-	15	**25**	µs

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed. Values derived from +25°C median data.

3.5.2 Low Power Mode

AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM =2.5V, f_{SAMP} = 395ksps, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s.**

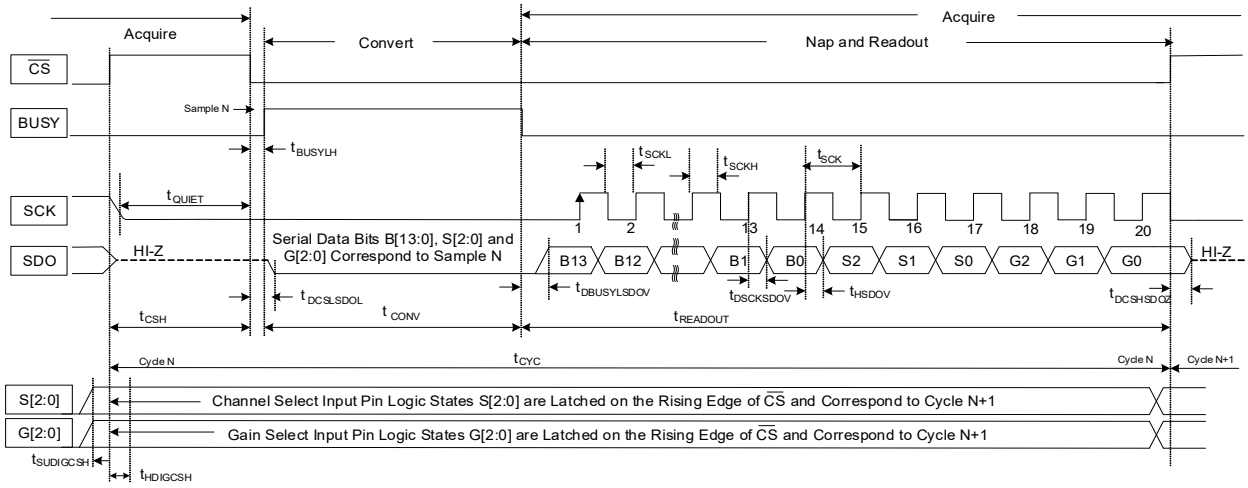
Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Timing Characteristics						
Maximum Sampling Frequency	f_{SAMP}	PGA Bypassed	-	-	**684.932**	kHz
		PGA Enabled	-	-	**413.223**	kHz
Conversion Time	t_{CONV}	BUSY Output High Time, PGA Bypassed	-	-	**660**	ns
		BUSY Output High Time, PGA Enabled	-	-	**1550**	ns
$\overline{CS}$ High Time	t_{CSH}	-	**500**	-	-	ns
SCK Held Low to $\overline{CS}\downarrow$	t_{QUIET}	-	**500**	-	-	ns

AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM =2.5V, f_{SAMP} = 395ksps, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across operating temperature range, -55C to +125C by production testing; over a total ionizing dose of 75krad(Si) at 25C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
$\overline{CS}$↓ to BUSY↑	t_{BUSYLH}	C_L = 10pF, PGA enabled.	-	-	**100**	ns
		C_L = 10pF, PGA bypassed.	-	-	**30**	ns
SCK Period	t_{SCK}	-	**20**	-	-	ns
SCK High Time	t_{SCKH}	-	**8**	-	-	ns
SCK Low Time	t_{SCKL}	-	**8**	-	-	ns
SDO Data Valid Delay from BUSY↓	$t_{DBUSYLSDOV}$	C_L = 10pF	-	-	**0**	ns
SDO Data Valid Delay from SCK↑	$t_{DSCKSDOV}$	C_L = 10pF	-	-	**20**	ns
SDO Data Valid Hold Time from SCK↑	t_{HSDOV}	C_L = 10pF	**7**	-	-	ns
SDO Bus Acquisition Time from $\overline{CS}$↓	$t_{DCSLSDOL}$	C_L = 10pF	-	-	**25**	ns
SDO Bus Relinquish Time after $\overline{CS}$↑	$t_{DCSHSDOZ}$	C_L = 10pF	-	-	**25**	ns
G2:0, S2:0 to $\overline{CS}$↑	$t_{SUDIGCSH}$	Setup time for gain and channel select bits.	**15**	-	-	ns
G2:0, S2:0 from $\overline{CS}$↑	$t_{HDIGCSH}$	Hold time for gain and channel select bits.	**10**	-	-	ns
SCAN to $\overline{CS}$↑	t_{SCAN}	Setup time for SCAN input.	**20**	-	-	ns
Wake-Up time from Power-Down Mode	t_{WAKE}	Time to wait after $\overline{PD}$↑ to first sample[3]	-	15	**25**	µs

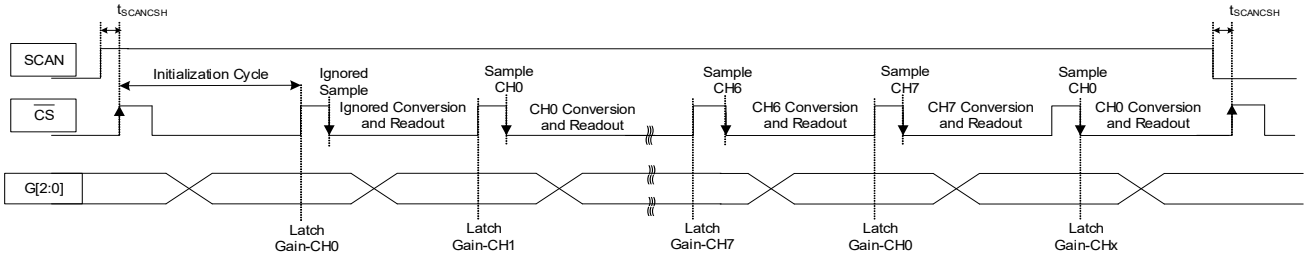
1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed. Values derived from +25°C median data.
3. Production tested in normal mode.

3.6 Timing Diagrams



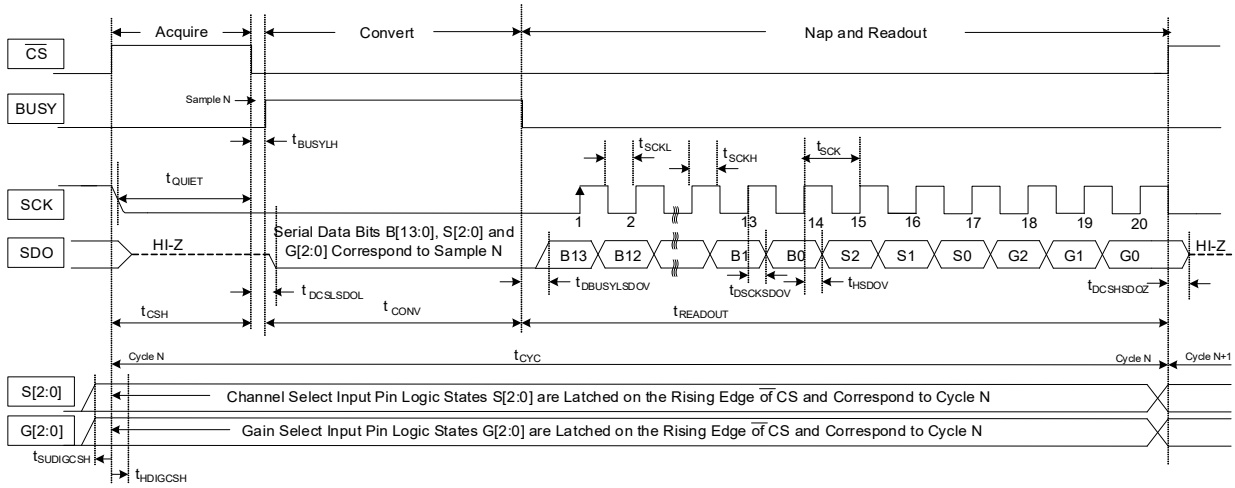
***Bits S2, S1, S0, G2, G1, and G0 are optional and not required. For maximum sample rate do not provide additional clocks for these bits.**

Figure 5. ISL73148SEH Operational Timing Diagram - Normal Operation



Gain Select Bits G[2:0] are Latched on the Rising Edge of $\overline{CS}$ in Cycle N and Correspond to Conversion Cycle N+1

Figure 6. ISL73148SEH SCAN Timing Diagram - Normal Mode



***Bits S2, S1, S0, G2, G1, and G0 are optional and not required. For maximum sample rate do not provide additional clocks for these bits.**

Figure 7. ISL73148SEH Operational Timing Diagram - Low Power Mode

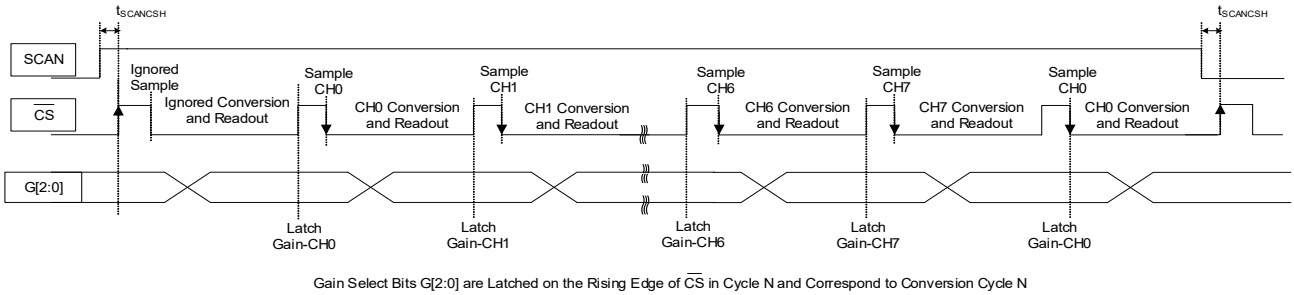


Figure 8. ISL73148SEH SCAN Timing Diagram - Low Power Mode

4. Typical Performance Curves

4.1 Normal Mode

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

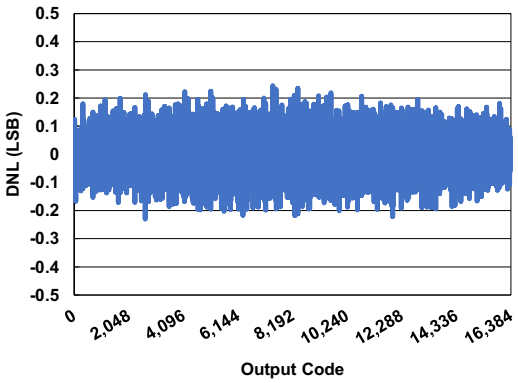


Figure 9. Differential Non-Linearity (DNL)

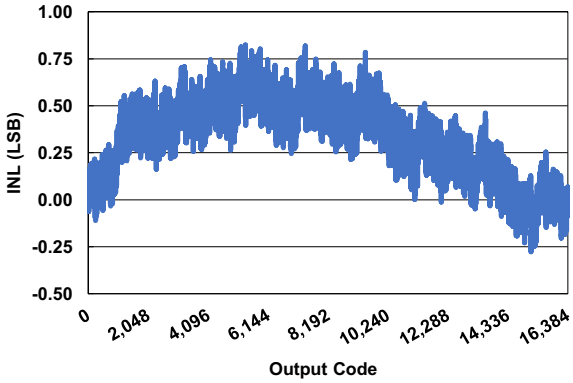


Figure 10. Integral Non-Linearity (INL)

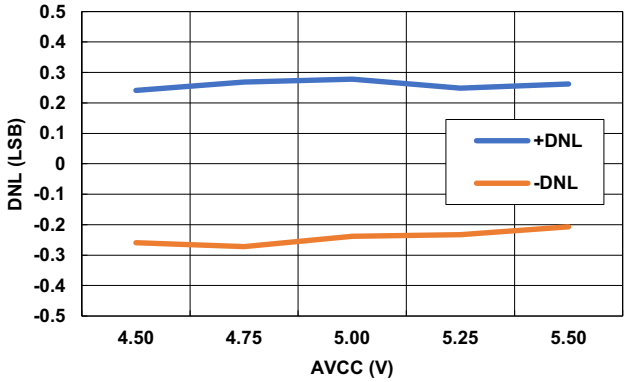


Figure 11. DNL vs AV_{CC}

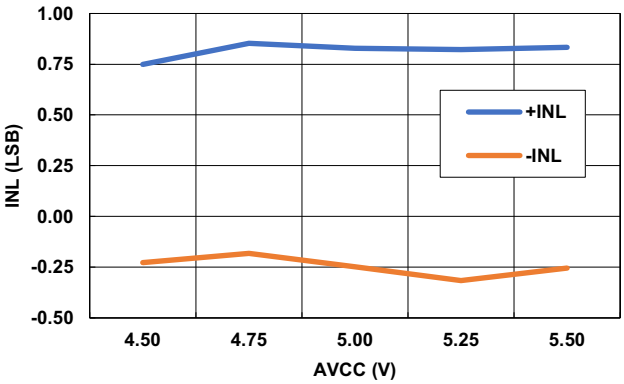


Figure 12. INL vs AV_{CC}

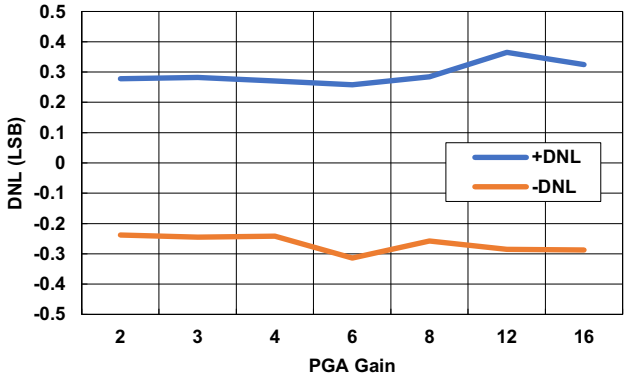


Figure 13. DNL vs PGA Gain

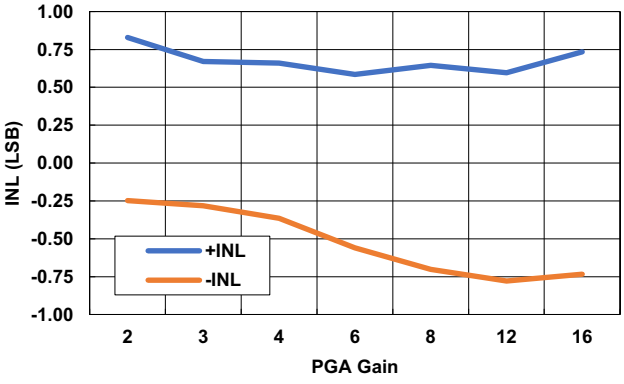


Figure 14. INL vs PGA Gain

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

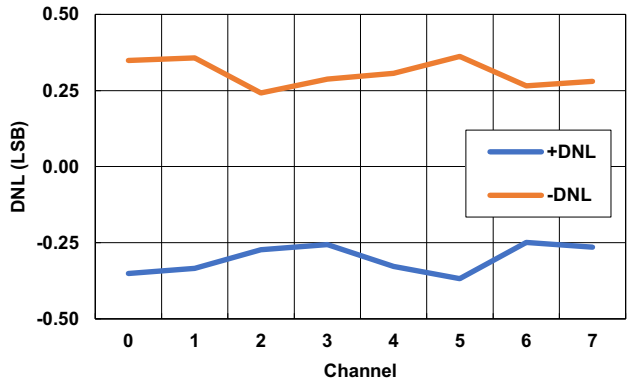


Figure 15. DNL vs Channel

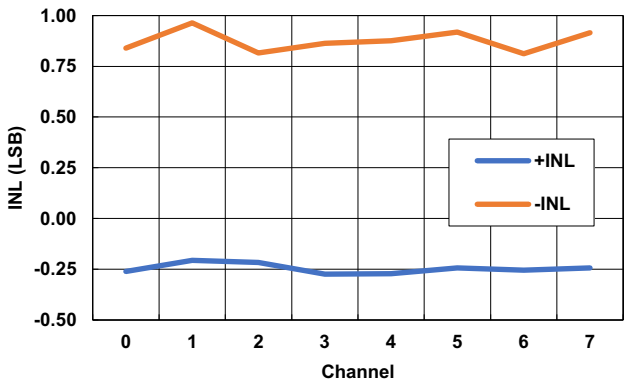


Figure 16. INL vs Channel

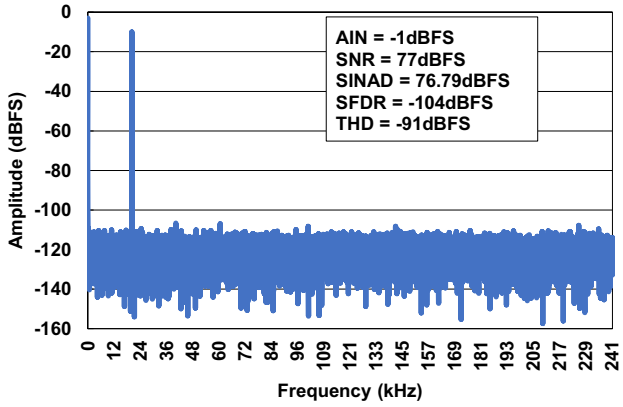


Figure 17. 32k FFT - 20.3kHz

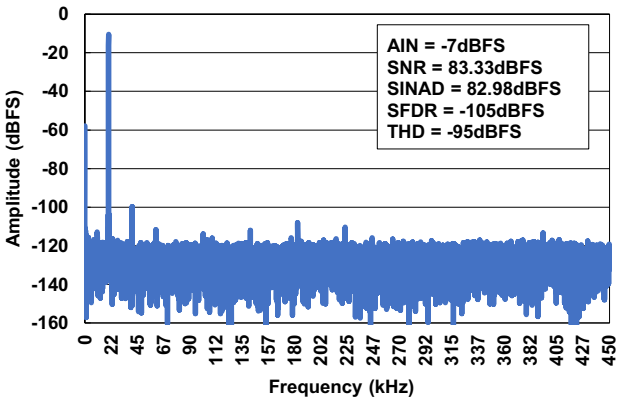


Figure 18. 32k FFT - 20.3kHz, PGA Bypassed

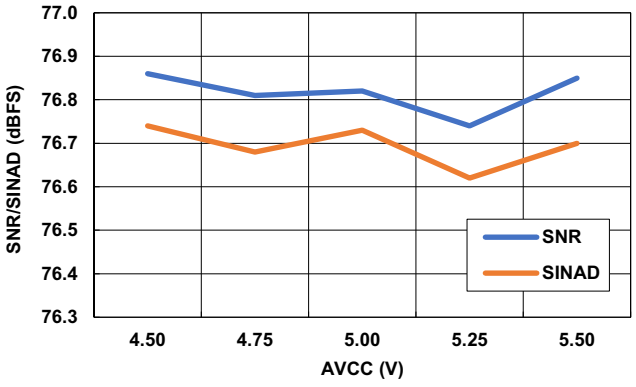


Figure 19. SNR and SINAD vs AV_{CC}

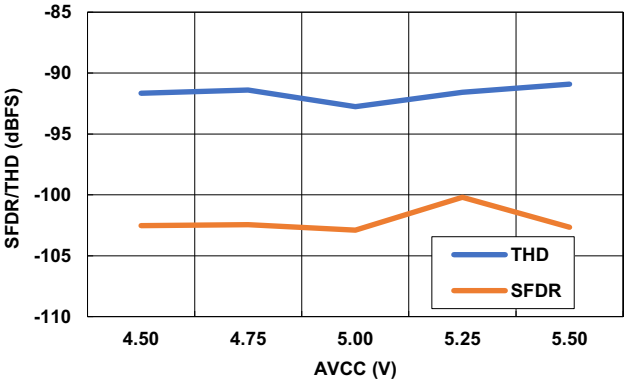


Figure 20. SFDR and THD vs AV_{CC}

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

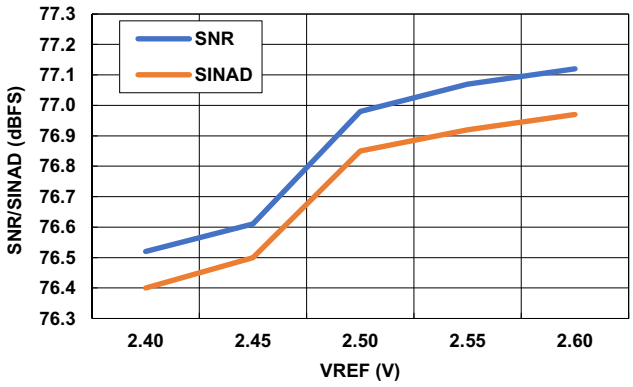


Figure 21. SNR and SINAD vs VREF

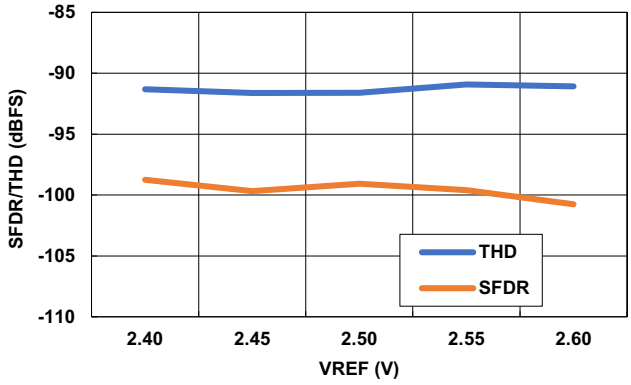


Figure 22. SFDR and THD vs VREF

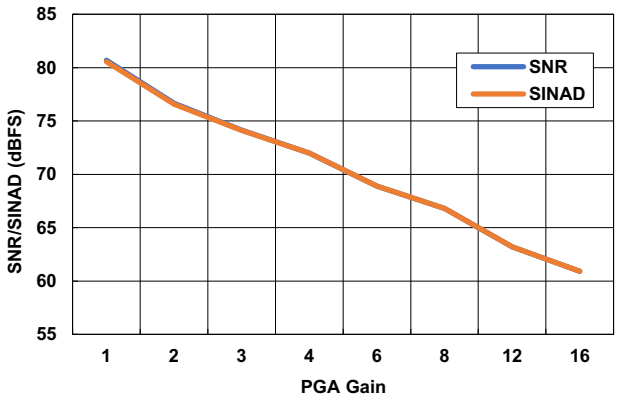


Figure 23. SNR and SINAD vs PGA Gain

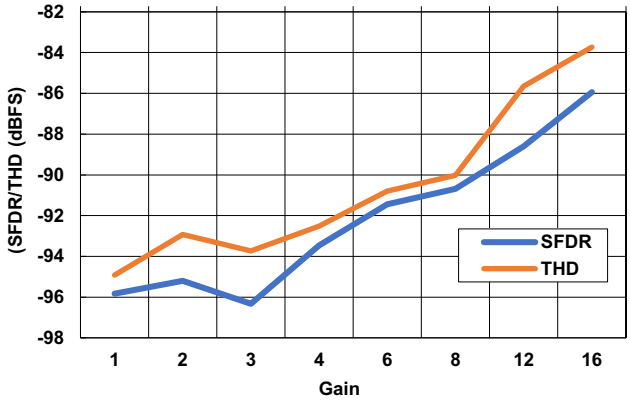


Figure 24. SFDR and THD vs PGA Gain

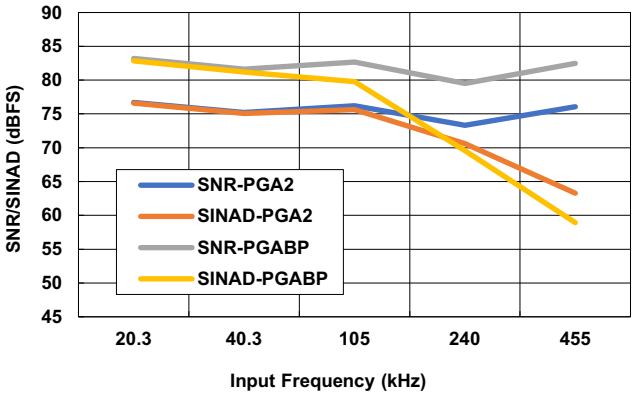


Figure 25. SNR and SINAD vs Frequency

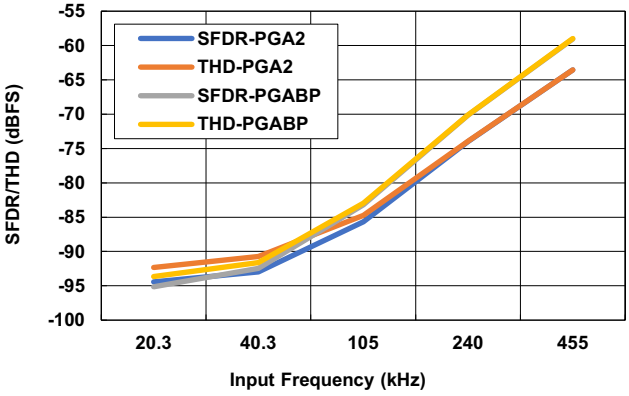


Figure 26. SFDR and THD vs Frequency

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

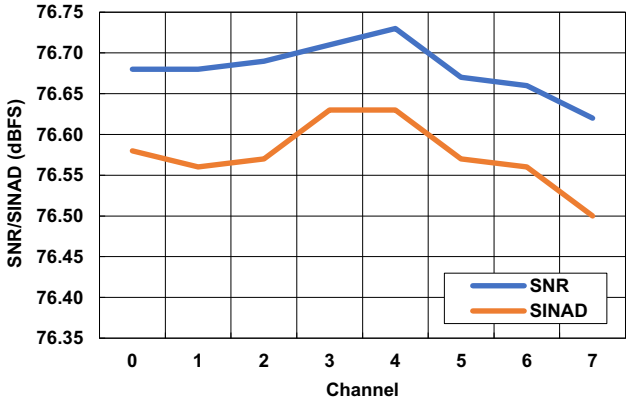


Figure 27. SNR and SINAD vs Channel

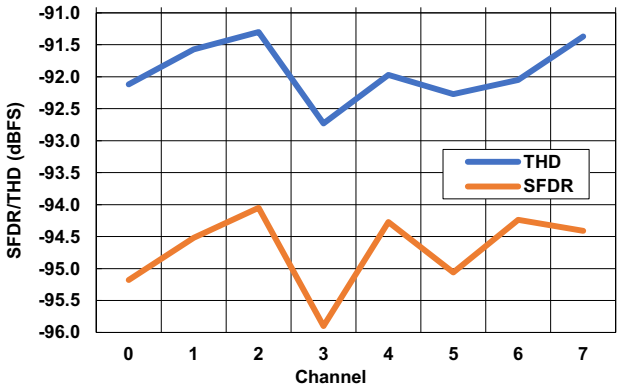


Figure 28. SFDR and THD vs Channel

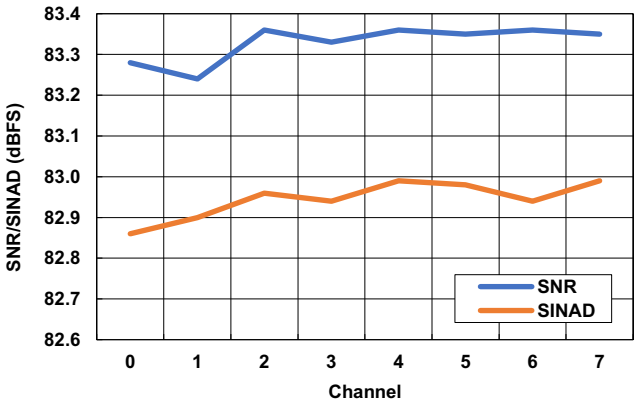


Figure 29. SNR and SINAD vs Channel - PGA Bypassed

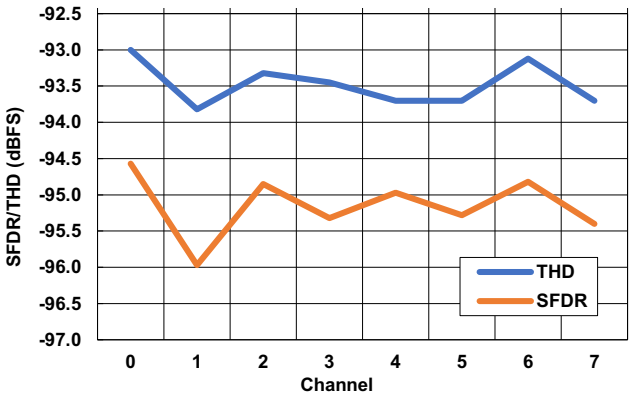


Figure 30. SFDR and THD vs Channel - PGA Bypassed

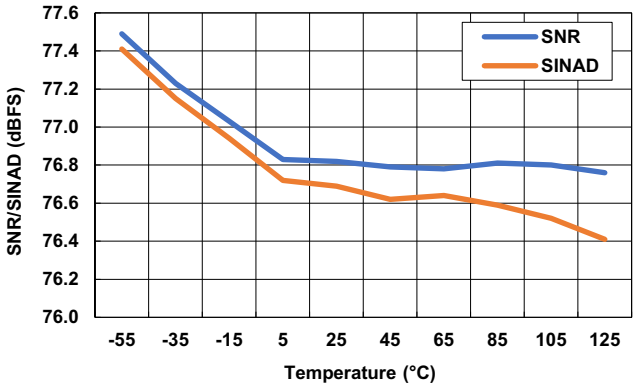


Figure 31. SNR and SINAD vs Temperature

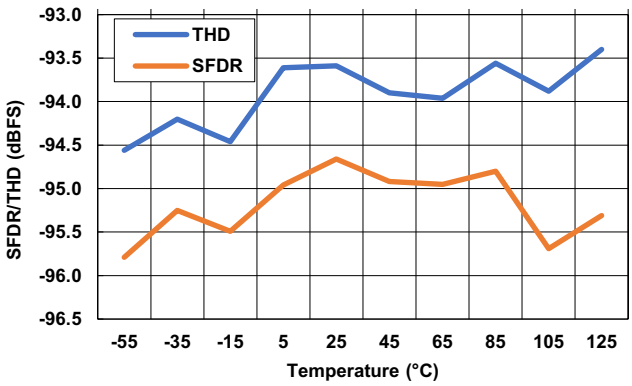


Figure 32. SFDR and THD vs Temperature

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

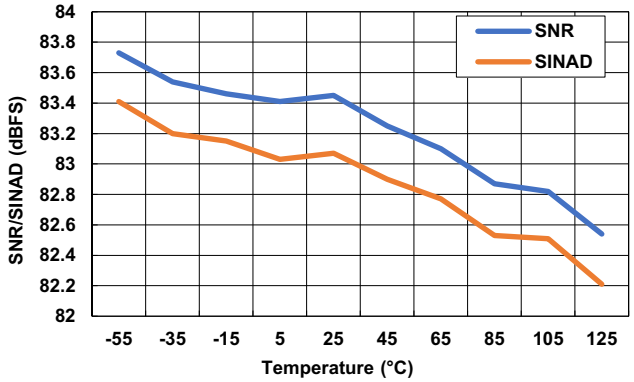


Figure 33. SNR and SINAD vs Temperature - PGA Bypassed

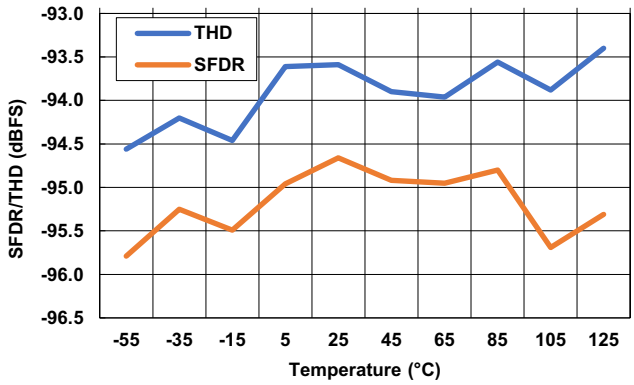


Figure 34. SFDR and THD vs Temperature - PGA Bypassed

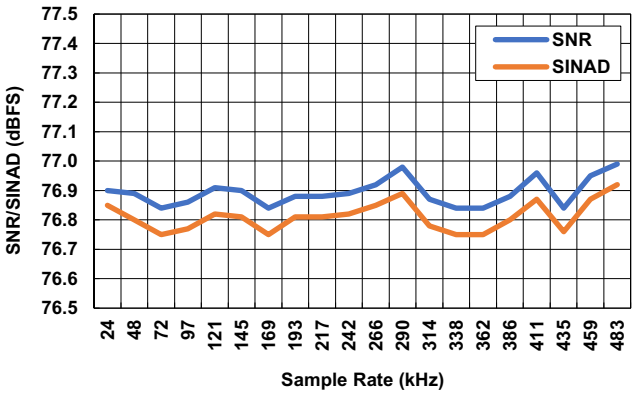


Figure 35. SNR and SINAD vs Sample Rate

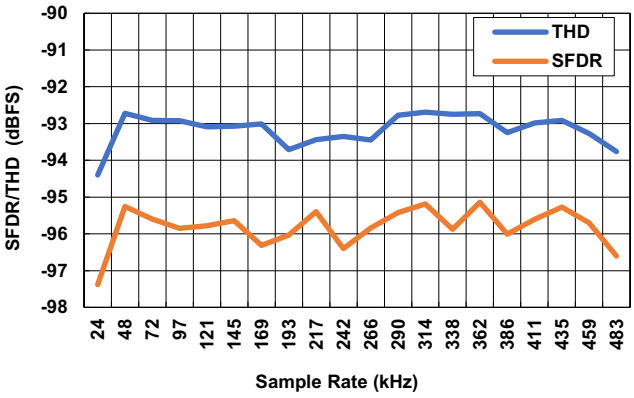


Figure 36. SFDR and THD vs Sample Rate

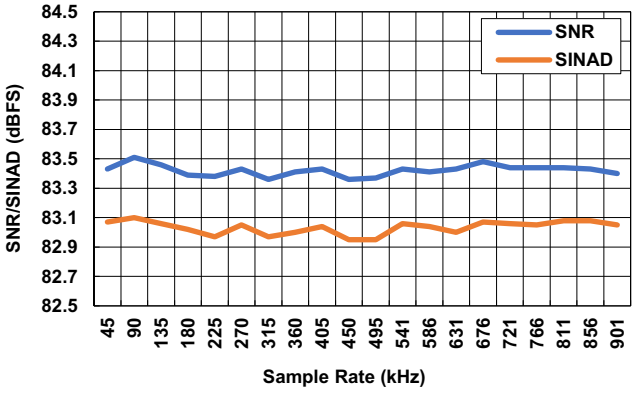


Figure 37. SNR and SINAD vs Sample Rate - PGA Bypassed

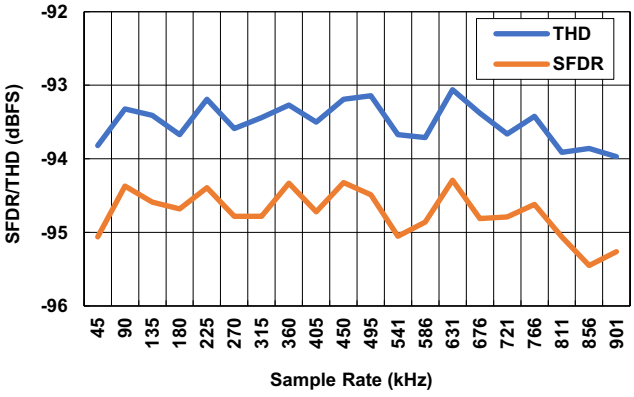


Figure 38. SFDR and THD vs Sample Rate - PGA Bypassed

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

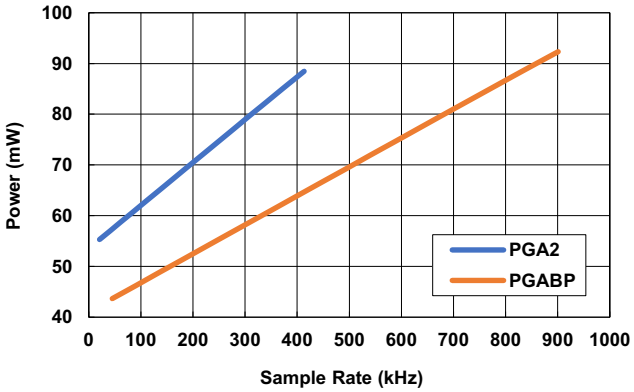


Figure 39. Power vs Sample Rate

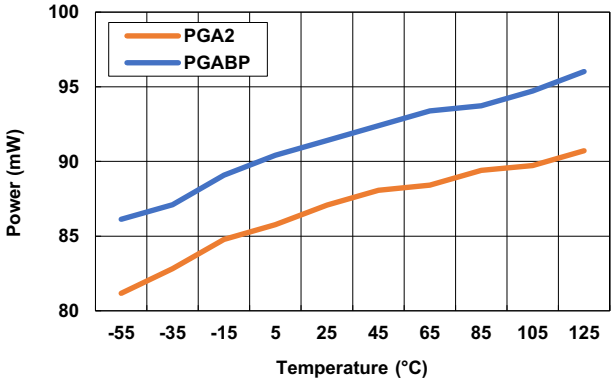


Figure 40. Power vs Temperature

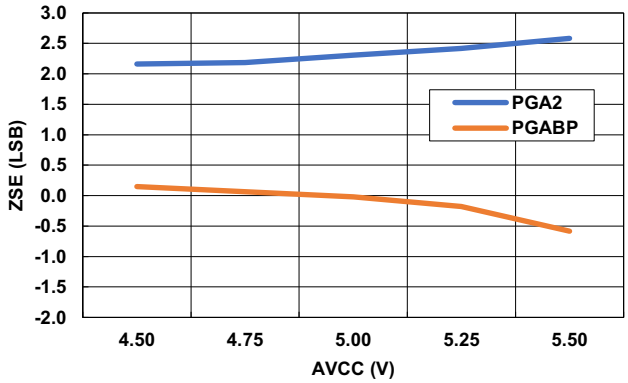


Figure 41. Zero-Scale Error vs AV_{CC}

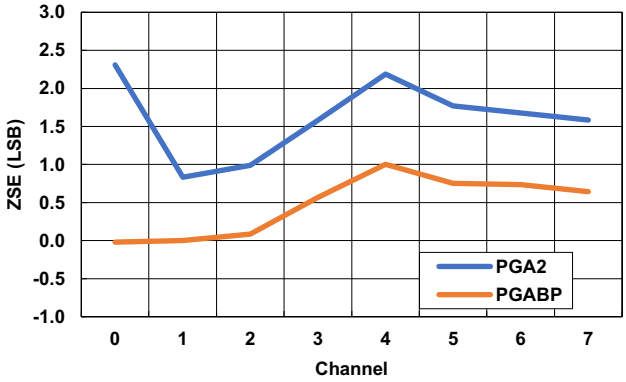


Figure 42. Zero-Scale Error vs Channel

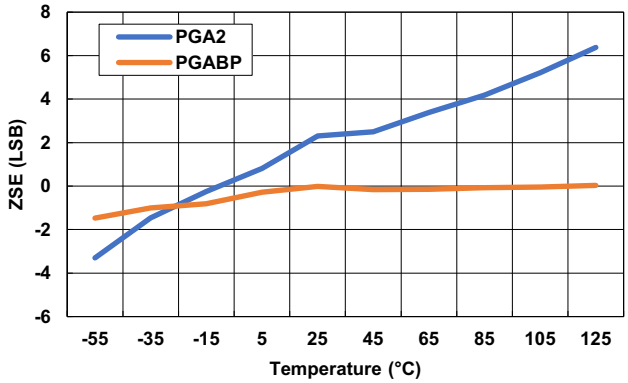


Figure 43. Zero-Scale Error vs Temperature

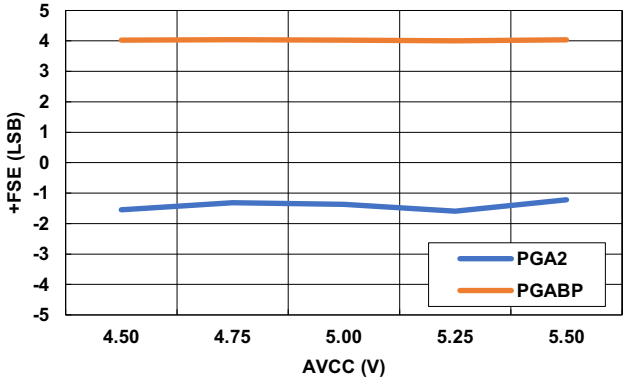


Figure 44. +Full-Scale Error vs AV_{CC}

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

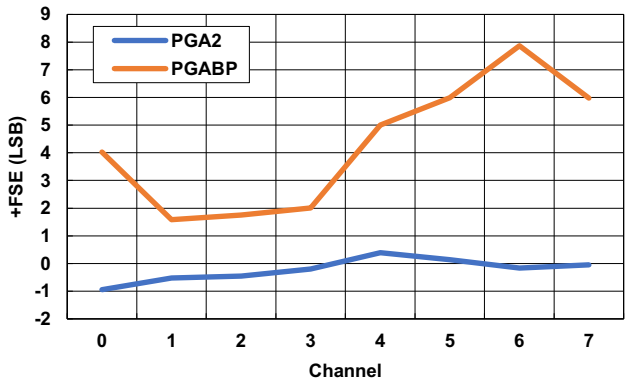


Figure 45. +Full-Scale Error vs Channel

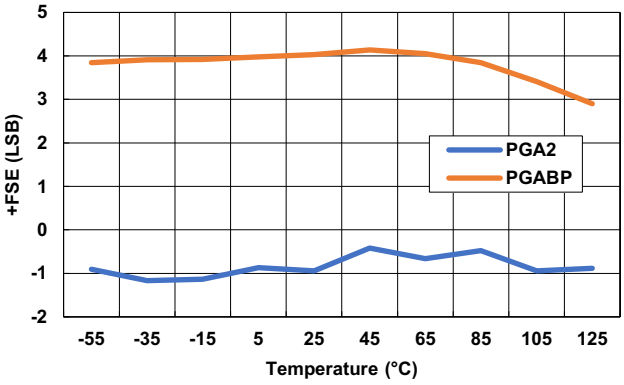


Figure 46. +Full-Scale Error vs Temperature

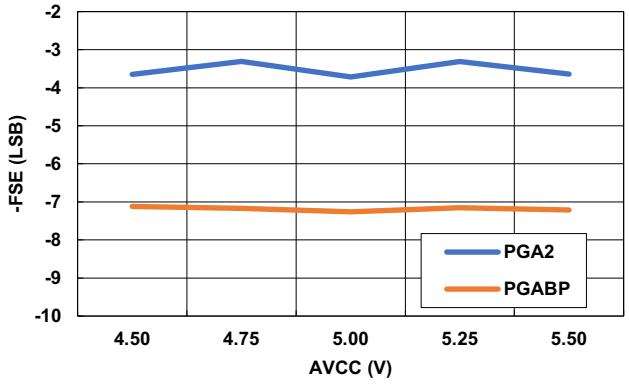


Figure 47. -Full-Scale Error vs AV_{CC}

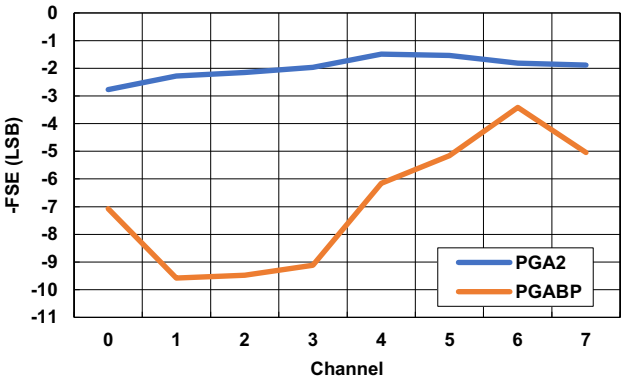


Figure 48. -Full-Scale Error vs Channel

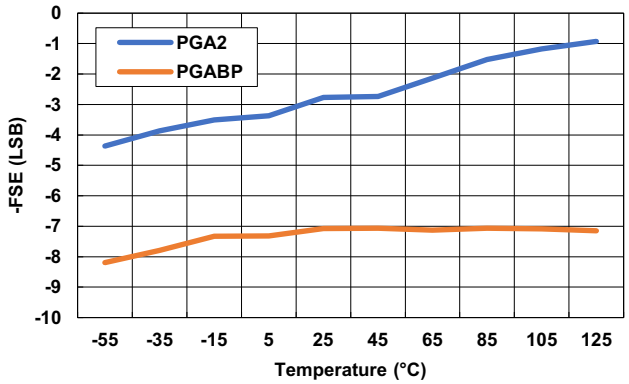


Figure 49. -Full-Scale Error vs Temperature

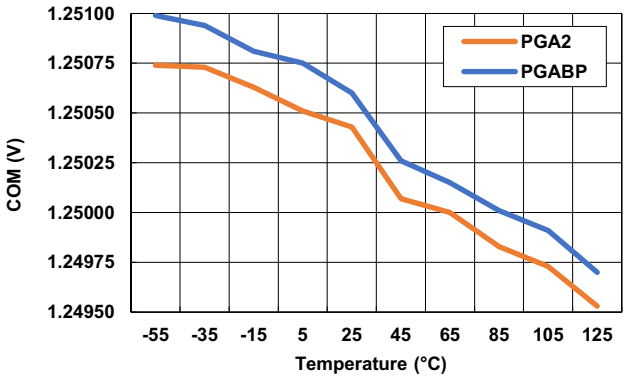


Figure 50. COM Output Voltage vs Temperature

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

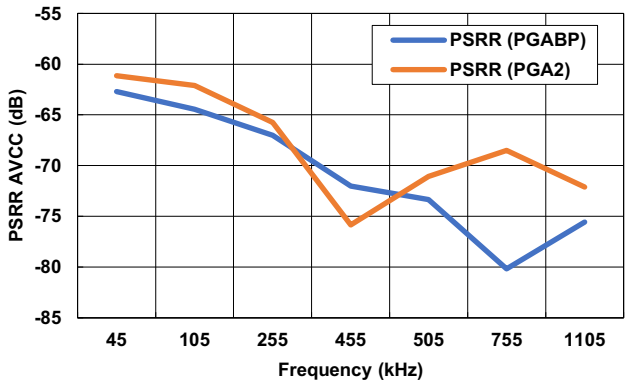


Figure 51. PSRR vs Frequency - AV_{CC}

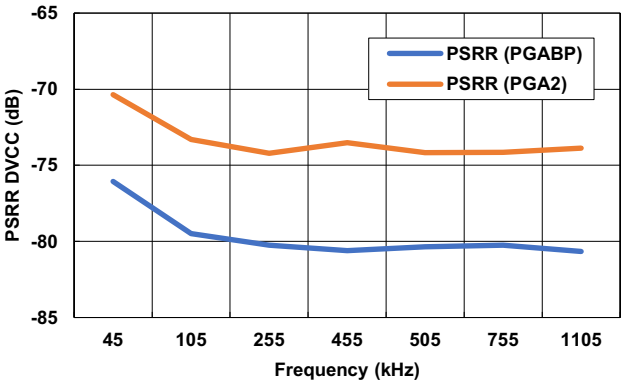


Figure 52. PSRR vs Frequency - DV_{CC}

4.2 Low Power Mode

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

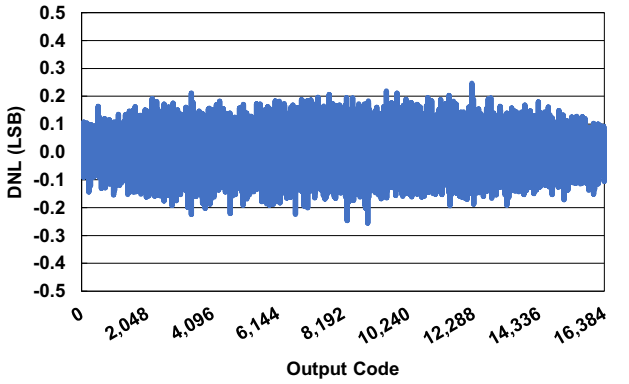


Figure 53. Differential Non-Linearity (DNL)

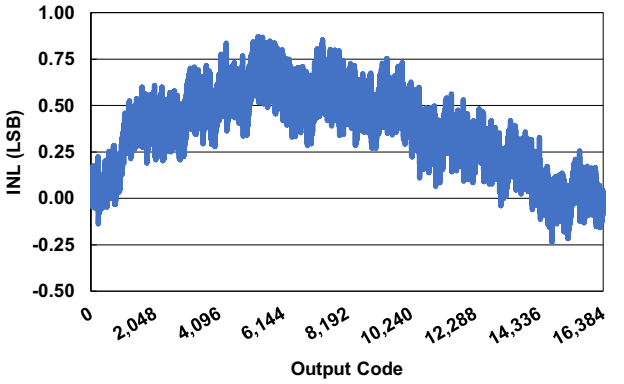


Figure 54. Integral Non-Linearity (INL)

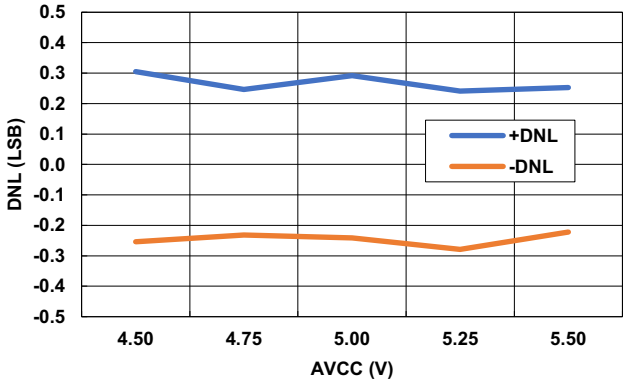


Figure 55. DNL vs AV_{CC}

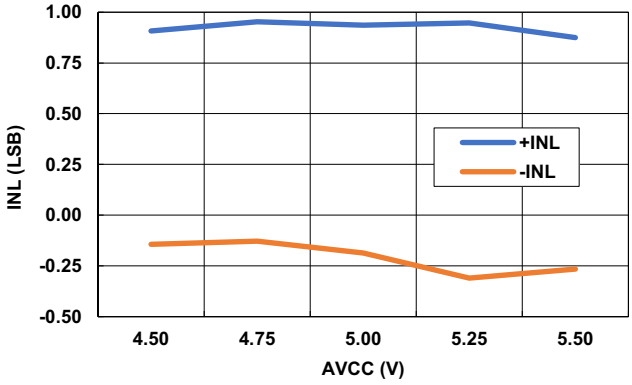


Figure 56. INL vs AV_{CC}

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

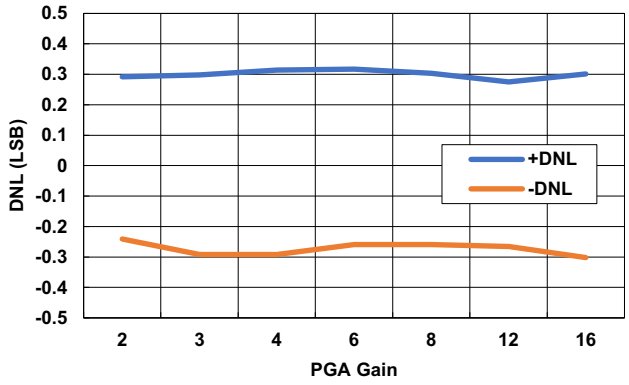


Figure 57. DNL vs PGA Gain

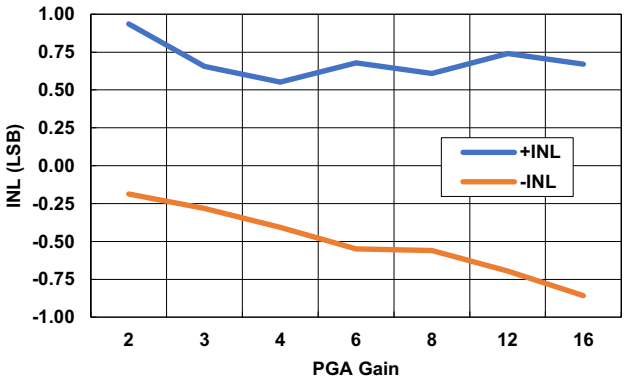


Figure 58. INL vs PGA Gain

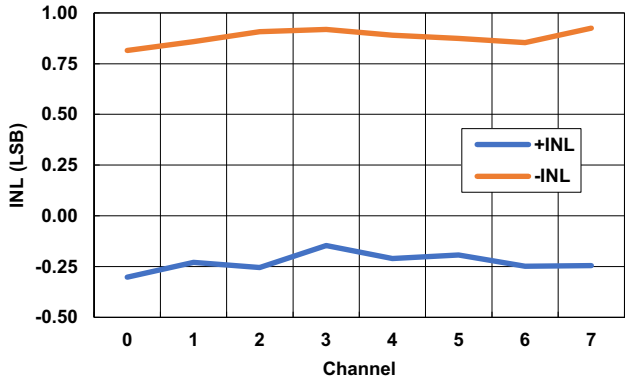


Figure 59. DNL vs Channel

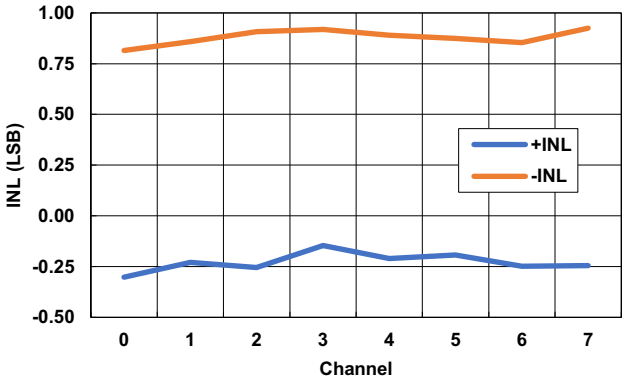


Figure 60. INL vs Channel

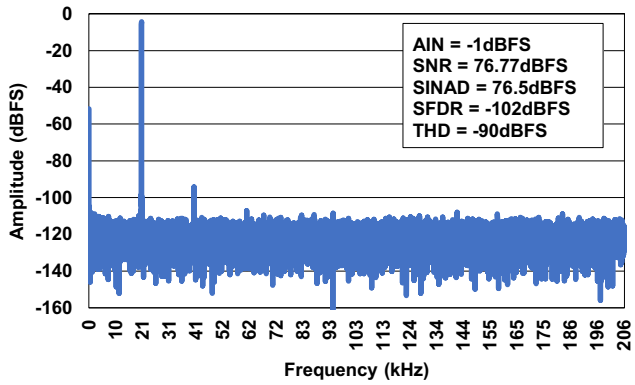


Figure 61. 32k FFT - 20.3kHz

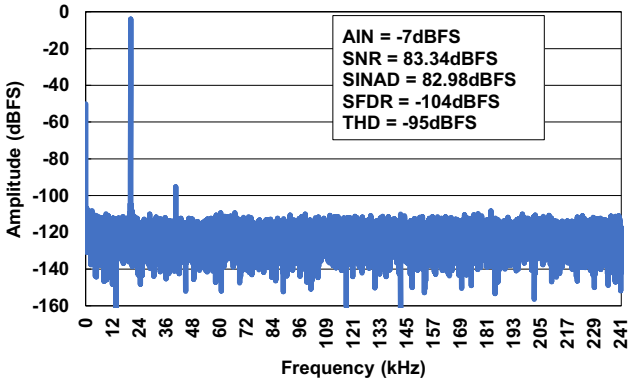


Figure 62. 32k FFT - 20.3kHz, PGA Bypassed

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

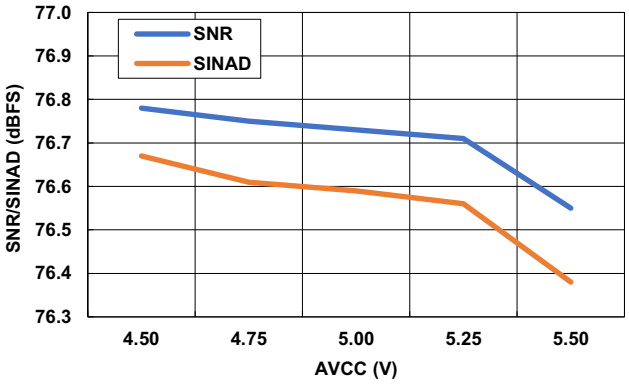


Figure 63. SNR and SINAD vs AV_{CC}

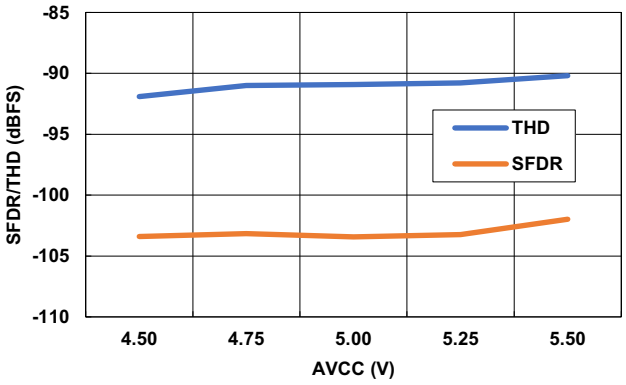


Figure 64. SFDR and THD vs AV_{CC}

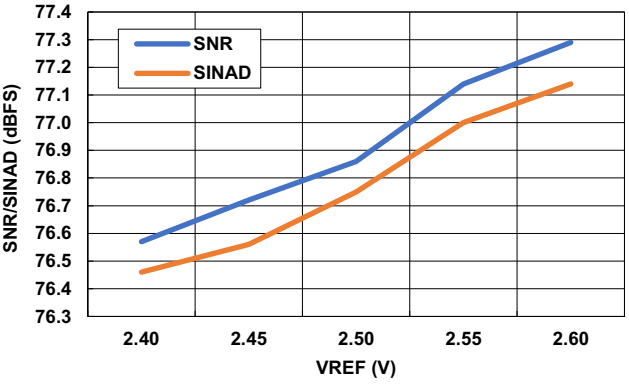


Figure 65. SNR and SINAD vs VREF

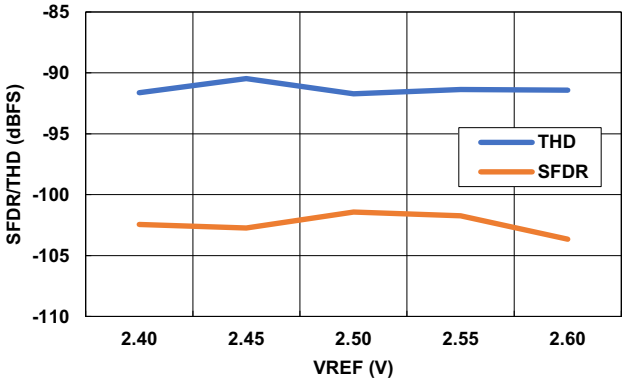


Figure 66. SFDR and THD vs VREF

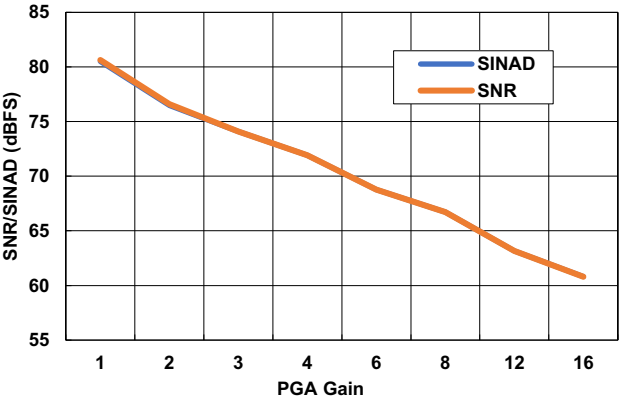


Figure 67. SNR and SINAD vs PGA Gain

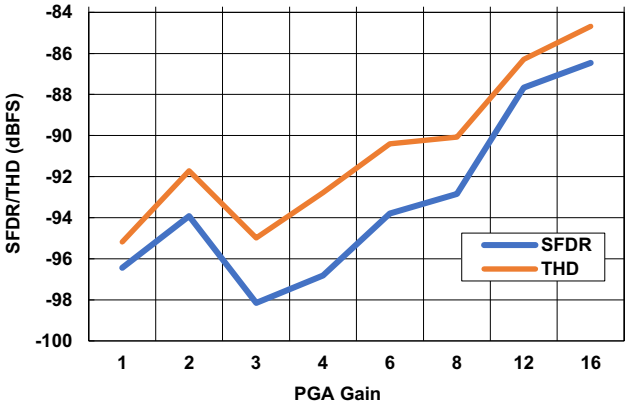


Figure 68. SFDR and THD vs PGA Gain

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

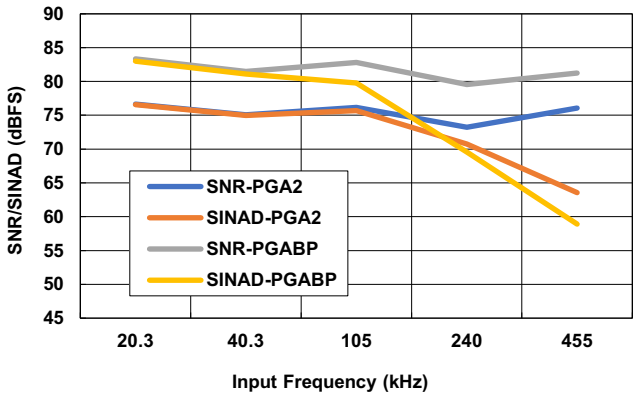


Figure 69. SNR and SINAD vs Frequency

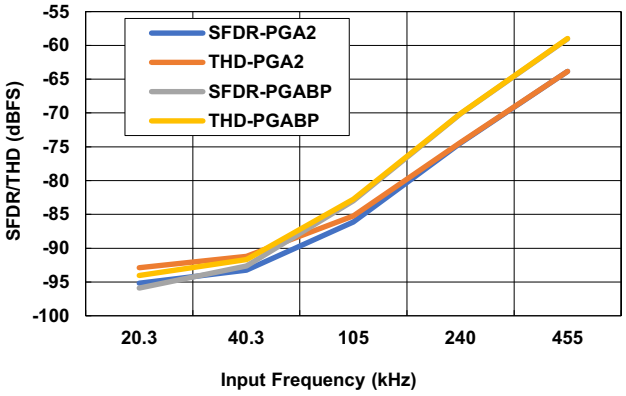


Figure 70. SFDR and THD vs Frequency

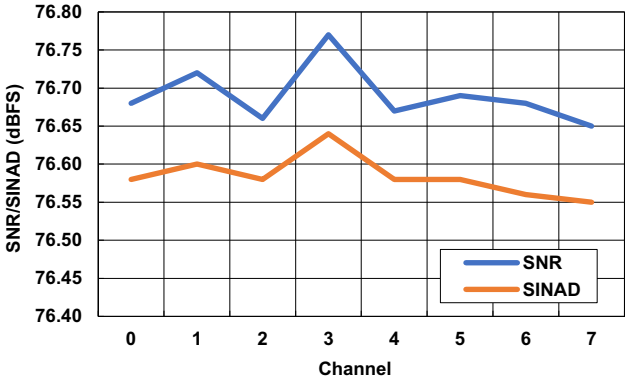


Figure 71. SNR and SINAD vs Channel

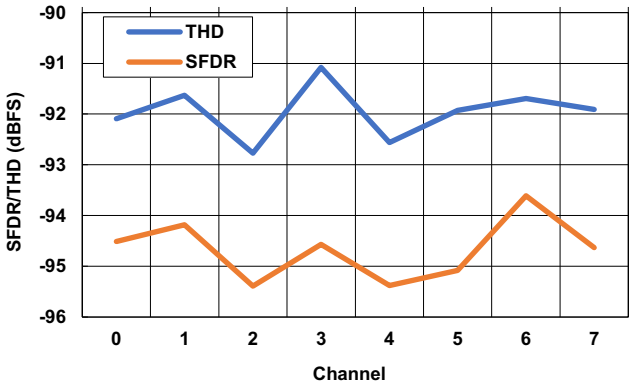


Figure 72. SFDR and THD vs Channel

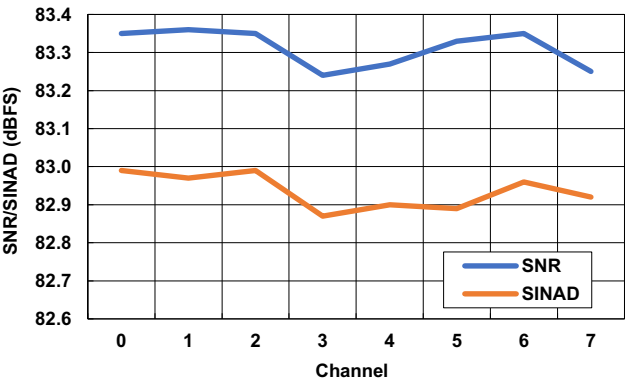


Figure 73. SNR and SINAD vs Channel - PGA Bypassed

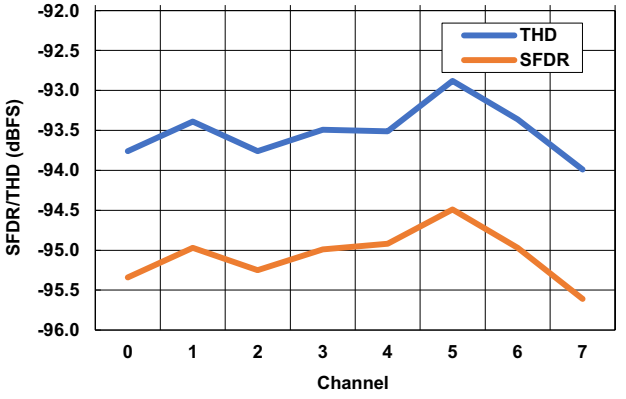


Figure 74. SFDR and THD vs Channel - PGA Bypassed

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

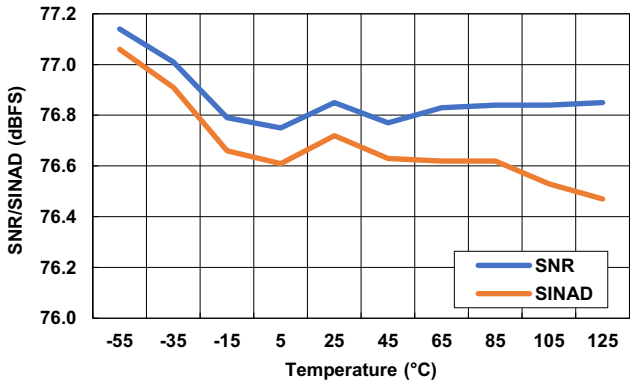


Figure 75. SNR and SINAD vs Temperature

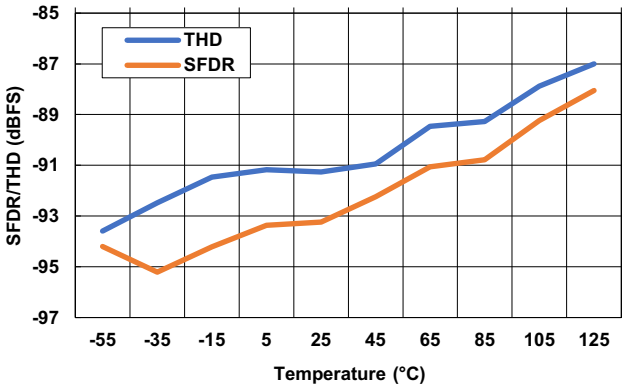


Figure 76. SFDR and THD vs Temperature

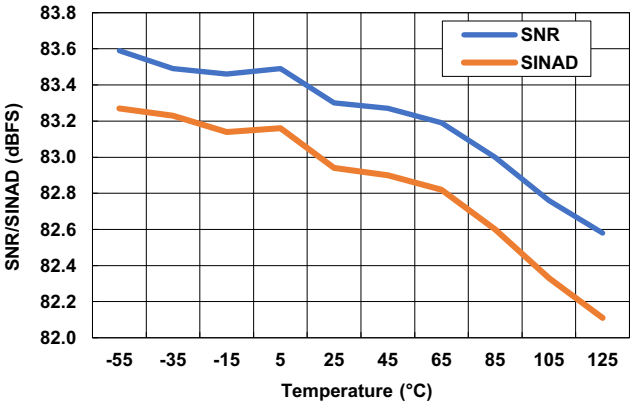


Figure 77. SNR and SINAD vs Temperature - PGA Bypassed

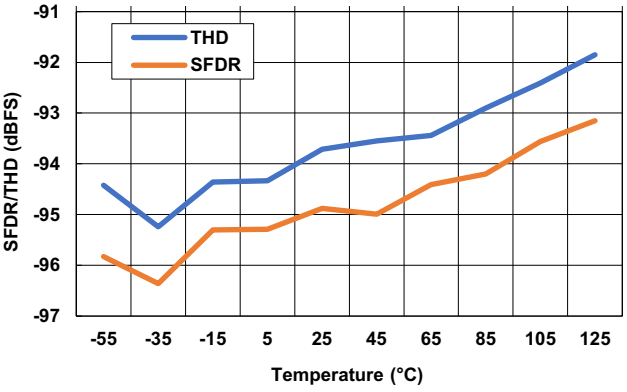


Figure 78. SFDR and THD vs Temperature - PGA Bypassed

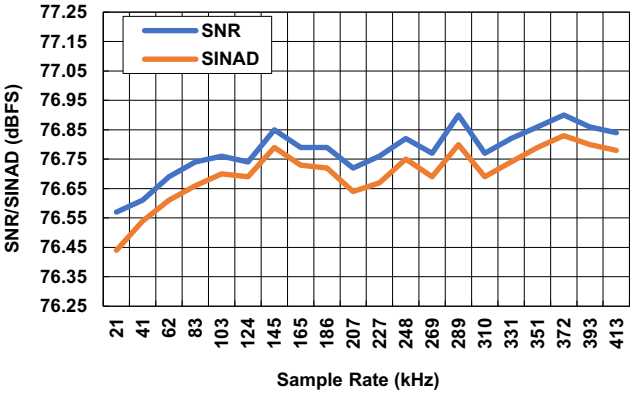


Figure 79. SNR and SINAD vs Sample Rate

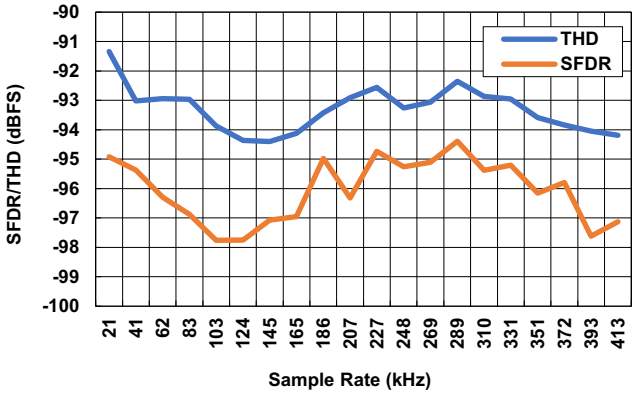


Figure 80. SFDR and THD vs Sample Rate

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

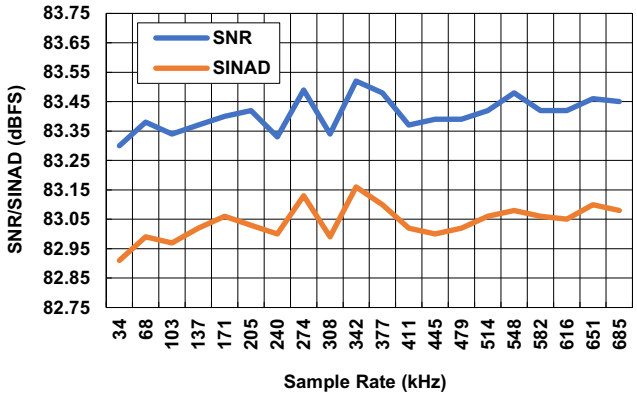


Figure 81. SNR and SINAD vs Sample Rate - PGA Bypassed

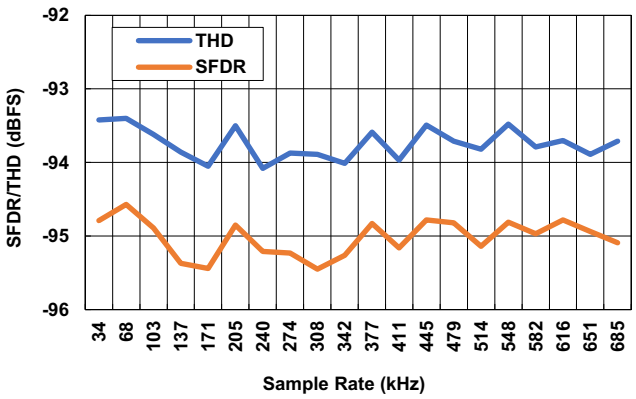


Figure 82. SFDR and THD vs Sample Rate - PGA Bypassed

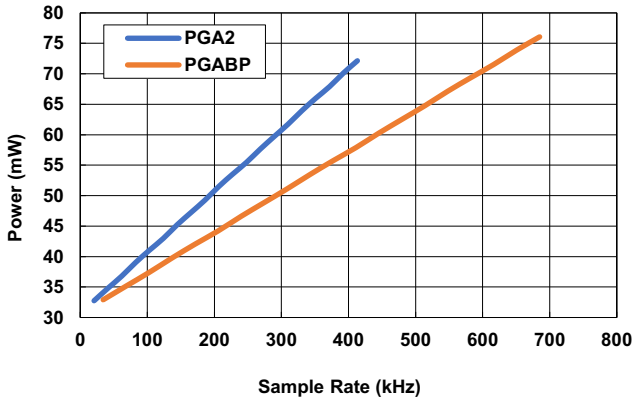


Figure 83. Power vs Sample Rate

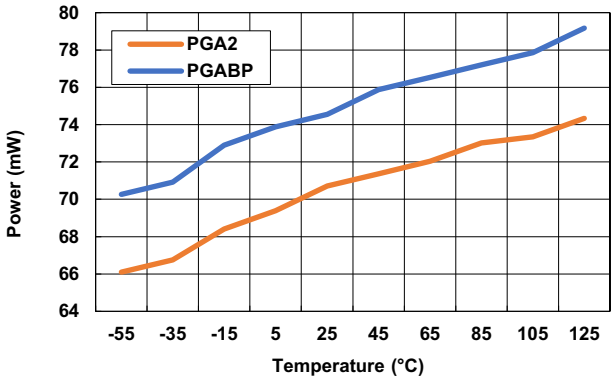


Figure 84. Power vs Temperature

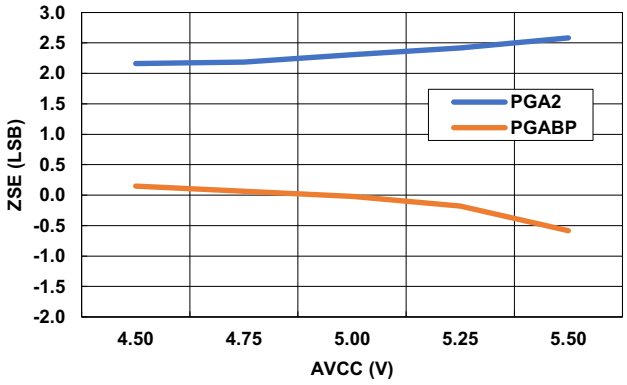


Figure 85. Zero-Scale Error vs AV_{CC}

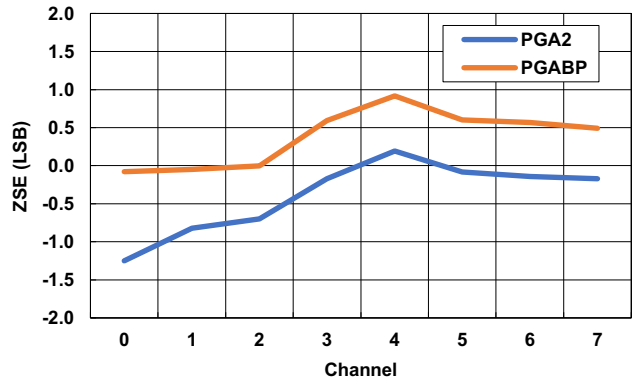


Figure 86. Zero-Scale Error vs Channel

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

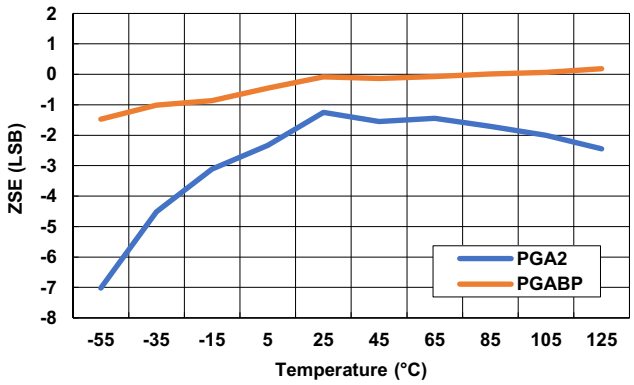


Figure 87. ZSE vs Temperature

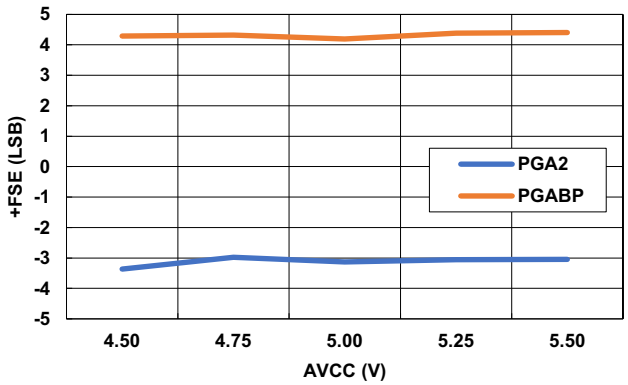


Figure 88. +FSE vs AV_{CC}

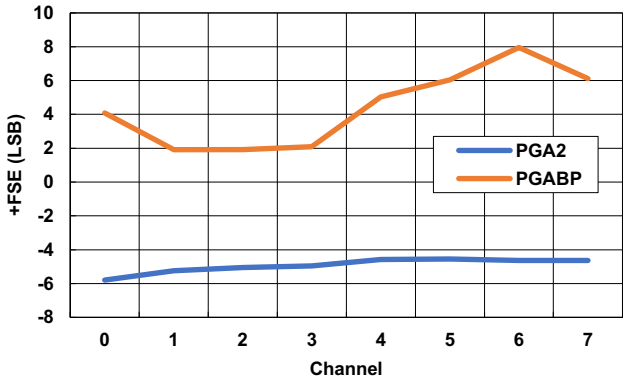


Figure 89. +FSE vs Channel

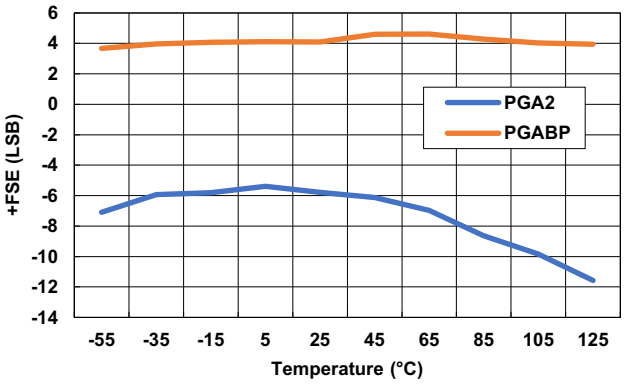


Figure 90. +FSE vs Temperature

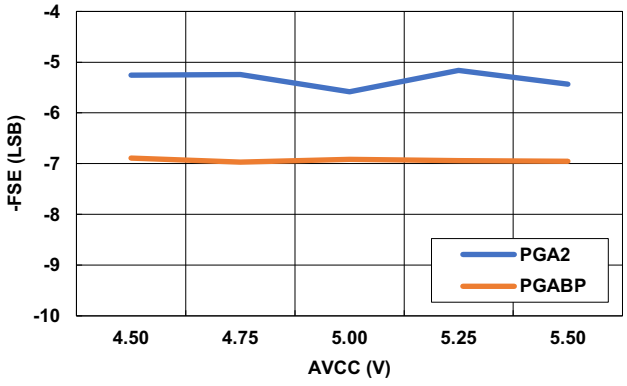


Figure 91. -FSE vs AV_{CC}

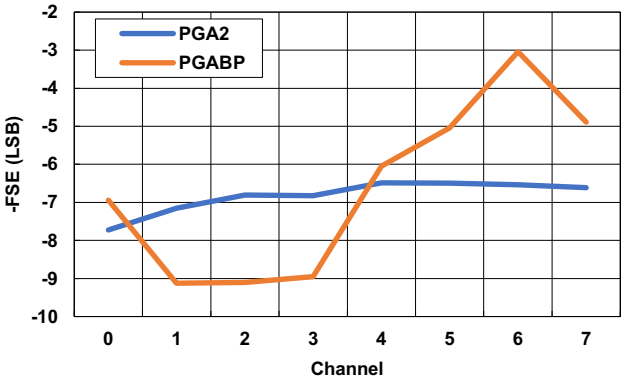


Figure 92. -FSE vs Channel

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin bypassed to ground with 0.1µF ceramic capacitor, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

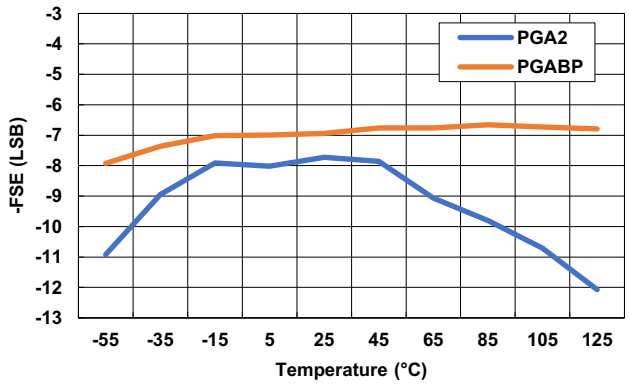


Figure 93. -FSE vs Temperature

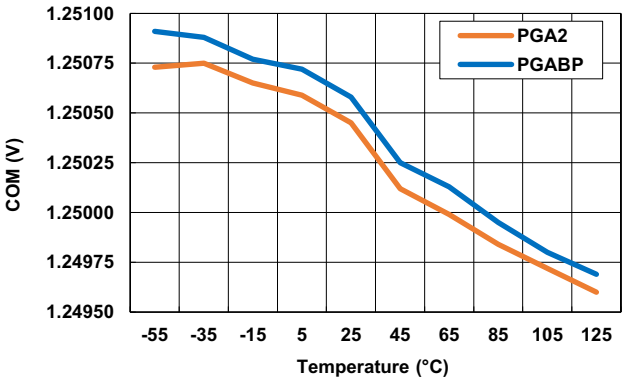


Figure 94. COM Output Voltage vs Temperature

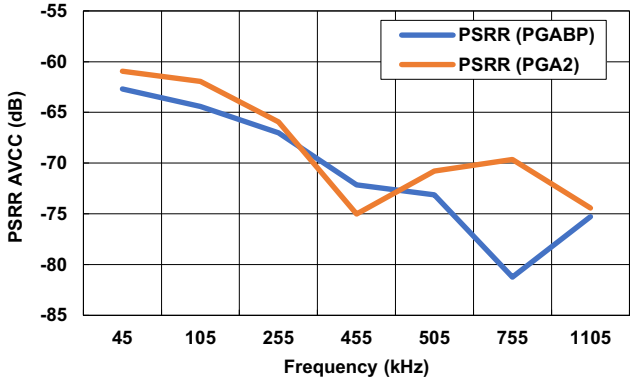


Figure 95. PSRR vs Frequency - AV_{CC}

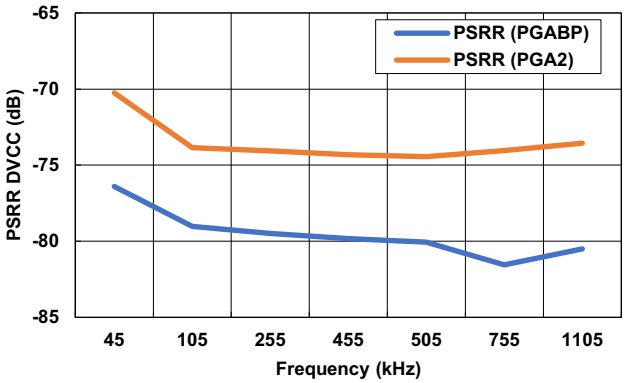


Figure 96. PSRR vs Frequency - DV_{CC}

4.3 Unipolar Data Format - Normal Mode

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin connect to GND, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

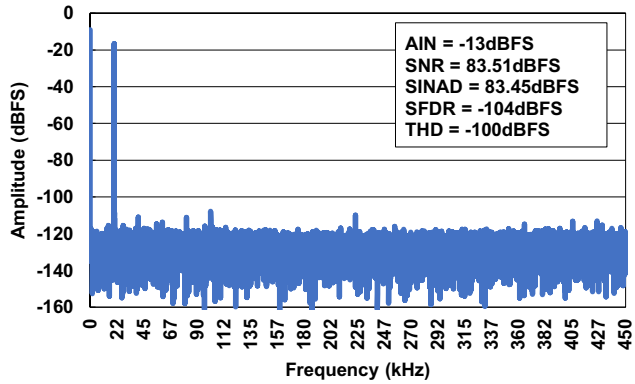


Figure 97. 32k FFT - 20.3kHz, PGA Gain = 2

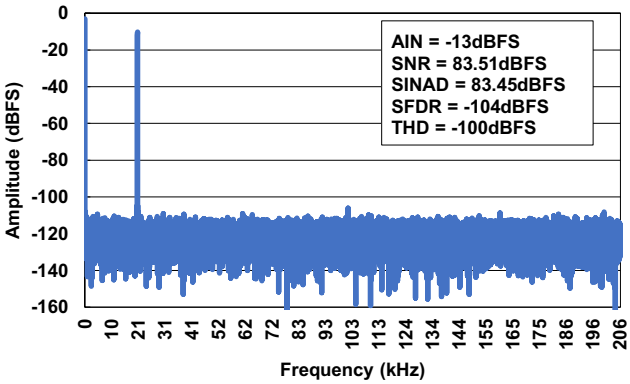


Figure 98. 32k FFT - 20.3kHz, PGA Bypassed

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin connect to GND, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

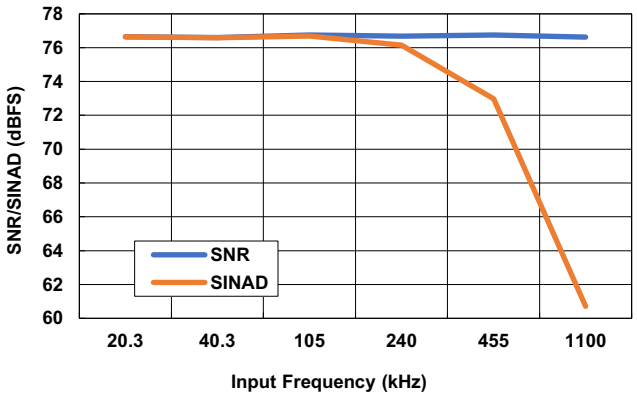


Figure 99. SNR and SINAD vs Frequency

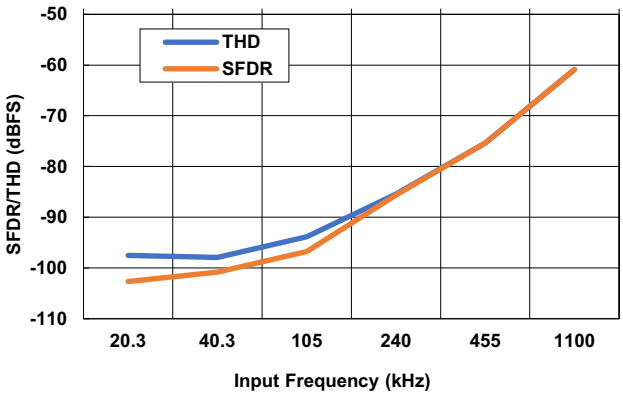


Figure 100. SFDR and THD vs Frequency

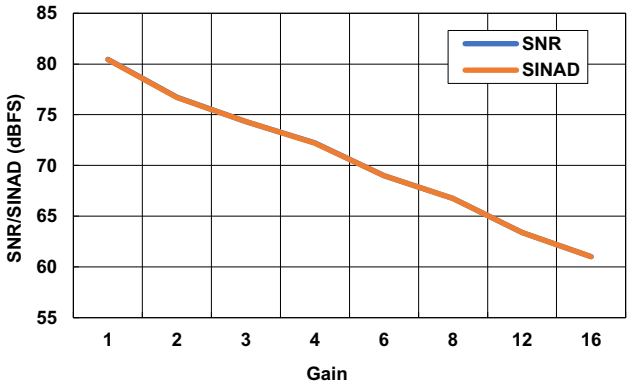


Figure 101. SNR and SINAD vs PGA Gain

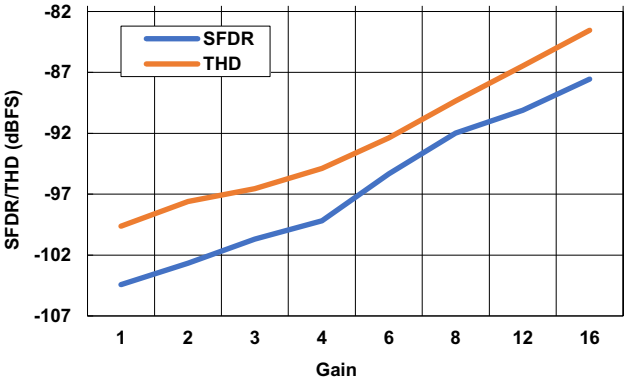


Figure 102. SFDR and THD vs PGA Gain

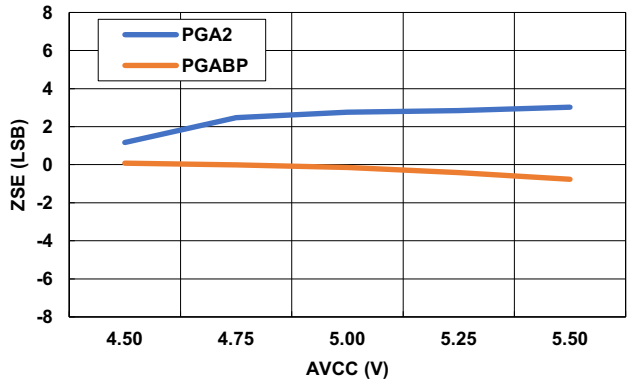


Figure 103. Zero-Scale Error vs AV_{CC}

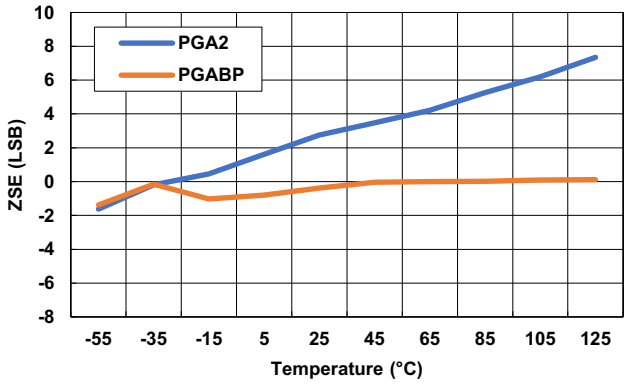


Figure 104. Zero-Scale Error vs Temperature

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin connect to GND, PGA Gain = 2, LPM = 0V, f_{SAMP} = 483.092ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

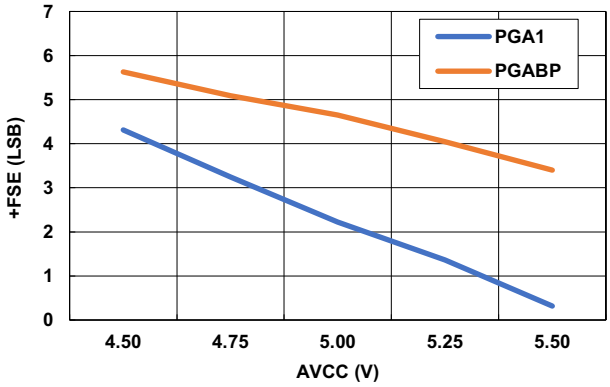


Figure 105. +Full-Scale Error vs AV_{CC}

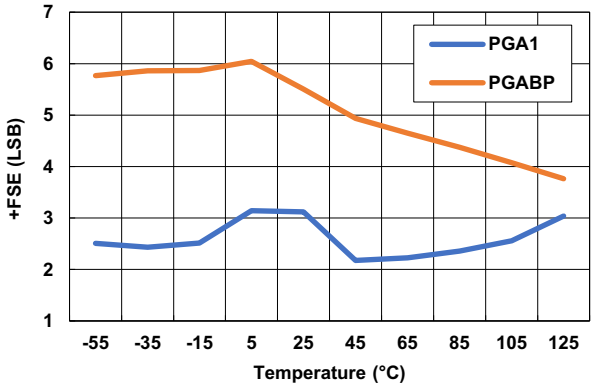


Figure 106. +Full-Scale Error vs Temperature

4.4 Unipolar Data Format - Low Power Mode

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin connect to GND, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

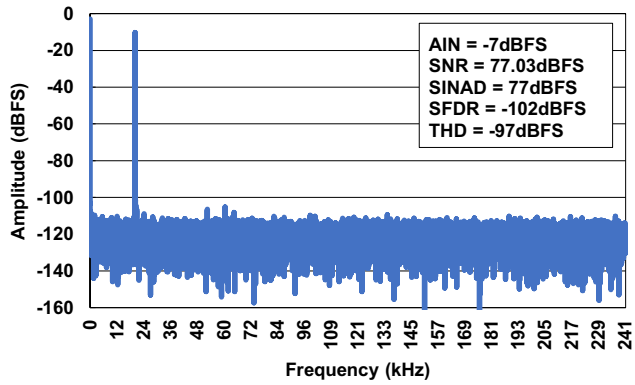


Figure 107. 32k FFT - 20.3kHz, PGA Gain = 2

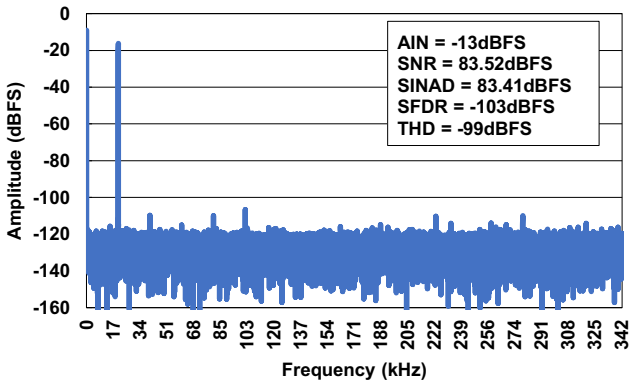


Figure 108. 32k FFT - 20.3kHz, PGA Bypassed

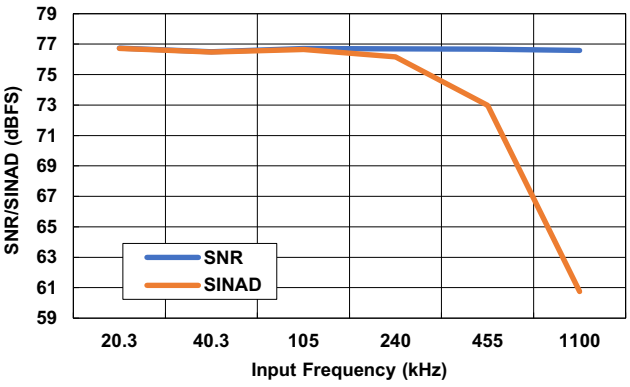


Figure 109. SNR and SINAD vs Frequency

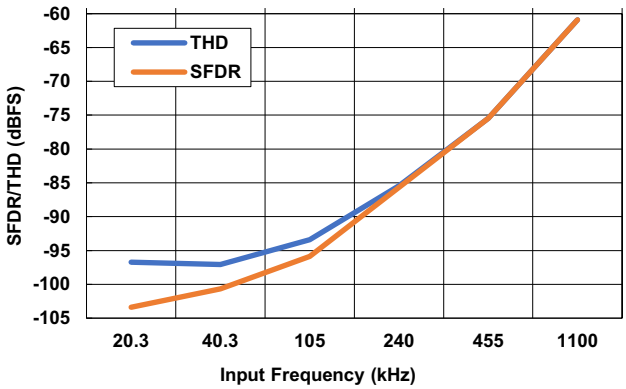


Figure 110. SFDR and THD vs Frequency

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, COM pin connect to GND, PGA Gain = 2, LPM = DV_{CC}, f_{SAMP} = 413.223ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C. (Cont.)

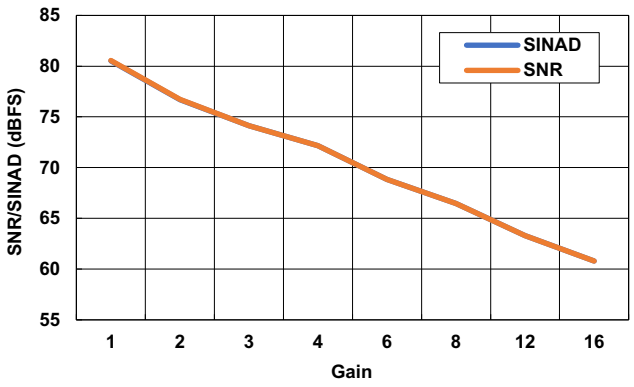


Figure 111. SNR and SINAD vs PGA Gain

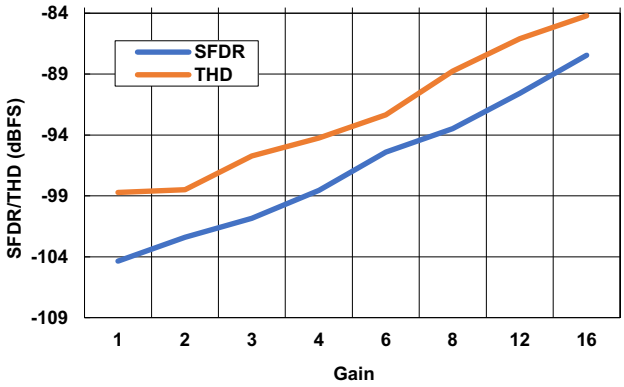


Figure 112. SFDR and THD vs PGA Gain

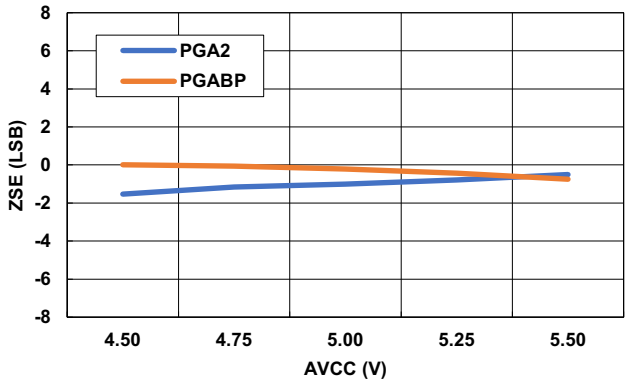


Figure 113. Zero-Scale Error vs AV_{CC}

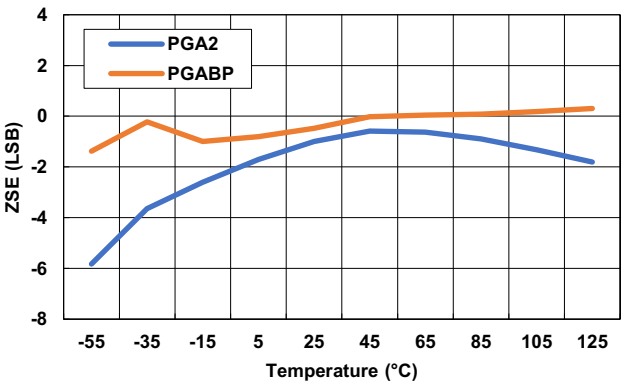


Figure 114. Zero-Scale Error vs Temperature

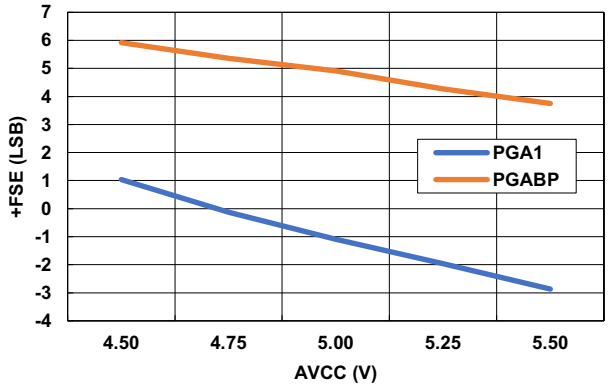


Figure 115. +Full-Scale Error vs AV_{CC}

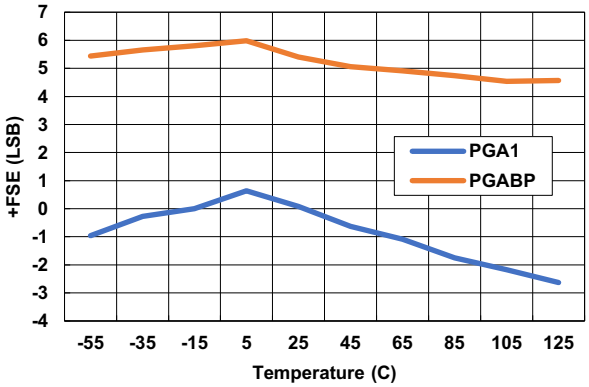


Figure 116. +Full-Scale Error vs Temperature

5. Applications Information

5.1 Overview

The ISL73148SEH is a radiation hardened, high precision, low noise, 8-channel 14-bit Successive Approximation Register (SAR) ADC. The ADC core is preceded by eight independently buffered analog input channels followed by an 8-to-1 multiplexer and a Programmable Gain Amplifier (PGA). The PGA features a bypass mode and 8-pin selectable gain settings: 1, 2, 3, 4, 6, 8, 12, and 16. Both channel and gain selections are controlled using pin-driven digital inputs.

The device operates from an analog supply voltage range of 4.5V to 5.5V, a digital supply voltage range of 2.2V to 3.6V, and has a dedicated reference input (REF). The device may be operated in unipolar or bipolar mode depending on the connection of the COM input. When the COM input is floated and bypassed to GND with a 0.1µF capacitor, it outputs a voltage equal to $V_{REF}/2$, and the analog input range is from $-V_{REF}/2$ to $V_{REF}/2$. When the COM input is grounded, the device operates in unipolar mode, where the analog input range is from 0V to V_{REF}/Gain, where Gain is the PGA gain setting.

The ISL73148SEH supports sample rates up to 900ksps with the PGA bypassed and up to approximately 480ksps with the PGA enabled, allowing system optimization based on the type of analog signal being sampled. The ISL73148SEH with PGA gain = 2 achieves excellent dynamic performance (77dB SNR, 90dB THD) and linearity (INL ±1.5LSB, DNL ±0.5LSB) while still maintaining a low power consumption of 89mW. A low power mode is available that reduces the power consumption of the ISL73148SEH by approximately 25% at maximum sampling rates, and greater than 50% at slower sampling rates. Additionally, the device offers a Sleep mode that minimizes power consumption to <50µW during idle operation.

The ISL73148SEH offers a high-speed serial interface with an independent digital supply (DV_{CC}) range of 2.2V to 3.6V, making it ideal to interface with 2.5V or 3.3V systems. The conversion data is output on the SDO pin with no latency. The ISL73148SEH supports up to a 50MHz serial data read clock on the SCK input.

The analog input voltage (A_{IN}) is sampled from the selected input channel on the falling edge of $\overline{CS}$. The input range of the ISL73148SEH is determined by the REF pin voltage and the PGA gain setting. The ISL73148SEH supports excellent THD and SFDR sampling input signal frequencies up to and beyond Nyquist (such as f_{IN} ≥ 450kHz with f_{SAMP} = 900ksps).

5.2 Serial Interface and BUSY

The ISL73148SEH uses a 3-wire serial port interface to communicate with other devices such as microcontrollers and other external circuitry. A falling edge on $\overline{CS}$ initiates conversion in the ISL73148SEH. Renesas requires holding $\overline{CS}$ high for at least 150ns before initiating the conversion when in normal operation and at least 500ns when operating in lower power mode. The conversion is timed by an internal oscillator. During the conversion process, the BUSY signal is asserted high. When the conversion is complete, BUSY is de-asserted. Renesas requires holding SCK low during t_{CONV}. When BUSY is de-asserted, the MSB is immediately available on the SDO pin. Each subsequent rising edge of SCK serially outputs data on SDO from the MSB-1 to the LSB. The input logic level of $\overline{CS}$ and SCK is determined by the DV_{CC} supply voltage that operates across a range of 2.2V up to 3.6V. Similarly, the output voltage level of BUSY is also determined by the DV_{CC} supply voltage.

5.3 Operational Phases and Timing

The conversion result MSB is available for serial readout at the SDO pin immediately following a completed conversion. The BUSY indicator flag is high during conversion, and transitions to low following completion of the conversion. When the BUSY indicator flag goes LOW after a conversion, the MSB of the conversion result (B13) is immediately available at the SDO pin. Subsequent rising edges of SCK shift bits MSB-1 (B12) through the LSB (B0) to SDO for readout. Optionally, the channel and gain selection for the current sample can be clocked out on the SDO pin after the LSB of the ADC data. This requires up to an additional six rising edges of SCK. The channel and gain selection bits are clocked out in order from MSB to LSB with the channel select bits output first (S2, S1,

S0) and the gain bits output last (G2, G1, G0). If less than six rising edges of SCK are provided after the 14 rising edges for the ADC data, the ISL73148SEH outputs only the amount of channel and gain bits equal to the number of rising edges of SCK provided. For example, if three rising edges of SCK are provided after the 14 rising edges for the ADC data, the ISL73148SEH only outputs the channel selection bits S2, S1, and S0; the gain selection bits are not outputted on SDO in this case. The output voltage level of SDO is determined by the DV_{CC} supply voltage, which may operate across a range of 2.2V to 3.6V.

The ISL73148SEH can be configured to operate in normal operation or low power mode. The operational timing of the device changes between these two modes. In both modes, the channel and gain selection bits can optionally be clocked out with the ADC data after each sample word. If these bits are clocked out, the sample period of the ISL73148SEH must be extended to accommodate the clocking of the additional bits.

The following are the three phases of operation in the ISL73148SEH that are shown in Figure 117 and Figure 118.

- Acquisition
- Conversion
- Readout

The Acquisition phase begins immediately following the completion of the conversion. During $\overline{CS}$ high, the SDO pin is held in high impedance (high-Z). The falling edge of $\overline{CS}$ defines the sampling instant of the ISL73148SEH, initiates a conversion, and also enables the SDO output to a low state. The conversion cycle is internally timed through an internal oscillator and takes an ensured maximum time of t_{CONV} to complete. Following conversion, several internal blocks are powered down to reduce power consumption. This phase of power-down is referred to as NAP mode. The ISL73148SEH stays in NAP mode until the next rising edge of $\overline{CS}$ where the ISL73148SEH is fully powered up.

The first sample outputs in normal mode immediately after supplying power to the device or exiting power-down mode is invalid. This is because of power reduction methods that place portions of the internal circuitry of the ISL73148SEH into sleep mode and the short duration of the $\overline{CS}$ pulse in normal mode. When a $\overline{CS}$ pulse is applied to the device, these portions of the internal circuitry are powered up and a valid sample can be acquired on the falling edge of the next subsequent $\overline{CS}$ pulse. If the first sample after power-up needs to be valid, the ISL73148SEH should be operated in low power mode.

5.3.1 Normal Operation Mode Timing

Figure 117 shows the basic timing of the ISL73148SEH in a conversion cycle during normal operation. When deriving timing, it is imperative to use the appropriate maximum and minimum specifications.

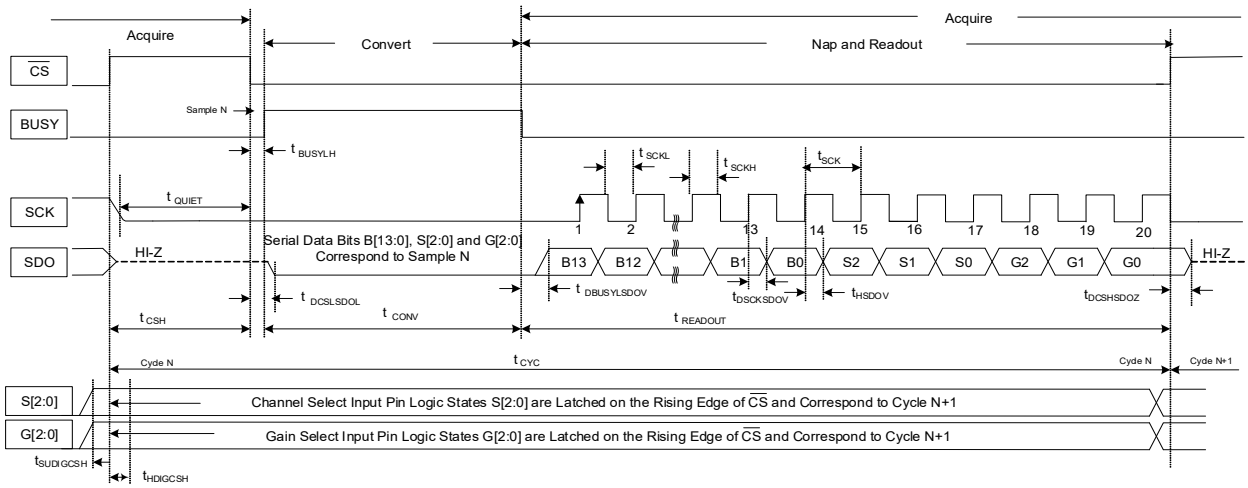


Figure 117. ISL73148SEH Timing Diagram - Normal Operation

The following is an example of timing calculation in an application operating the ISL73148SEH at 483.092ksps for the case where the channel and gain select bits are not clocked out on SDO with the ADC data and the ISL73148SEH is configured in normal operation with the PGA enabled. The $\overline{CS}$ input must be held high for 150ns (t_{CSH}). The time between the falling edge of $\overline{CS}$ and the rising edge of BUSY is a maximum of 100ns (t_{BUSYLH}) with the PGA enabled and 30ns with the PGA bypassed. The conversion time (t_{CONV}) is a maximum of 1550ns. To clock the data out of the ADC, there must be 14 rising edges of SCK ($t_{READOUT}$). To achieve the maximum sample rate, the 14th SCK falling edge must be coincident with the rising edge of $\overline{CS}$ for the subsequent sample. Using the maximum SCK frequency of 50MHz yields a readout time of:

$$t_{READOUT} = 13 \times 20ns + 10ns = 270ns$$

Note: The 14th SCK edge is coincident with the rising edge of $\overline{CS}$ so there is only a 1/2 period for the 14th SCK. The cycle time is calculated using Equation 1:

(EQ. 1) $$t_{CYC} = t_{CSH} + t_{BUSYLH} + t_{CONV} + t_{READOUT}$$

Using the timing parameters previously discussed, the sampling period and sampling rate is calculated as follows:

$$t_{CYC} = 150ns + 100ns + 1550ns + 270ns = 2070ns$$

$$f_{SAMP} = \frac{1}{2070ns} = 483.092ksps$$

When the channel and gain selection bits are clocked out on SDO along with the data, additional time must be alloted, therefore, resulting in a reduction in the sample rate of the ISL73148SEH. The six additional bits require an additional 6 SCK clock cycles to be read out on SDO. In this case, the 20th SCK falling edge must be coincident with the rising edge of $\overline{CS}$ for the subsequent sample. Using the maximum SCK frequency of 50MHz yields a read out time of:

$$t_{READOUT} = 19 \times 20ns + 10ns = 390ns$$

To accommodate the additional 120ns required to clock out the six additional bits for channel and gain information, the sample rate of the ISL73148SEH must be reduced. In other words, the sample period must be increased to accommodate time for clocking out these additional bits. The minimum sample period and corresponding maximum sample rate when clocking out the channel and gain selection bits is as follows:

$$t_{CYC} = 150ns + 100ns + 1550 + 390ns = 2190ns$$

$$f_{SAMP} = \frac{1}{2190ns} = 456.621ksps$$

The PGA can be bypassed to achieve the maximum possible sample rate in normal mode. N**ote:** In PGA bypass mode, t_{BUSYLH} = 30ns and t_{CONV} = 660ns. The timing and sample rate are calculated as follows:

$$t_{CYC} = t_{CSH} + t_{BUSYLH} + t_{CONV} + t_{READOUT} = 150ns + 30ns + 660ns + 270ns = 1110ns$$

$$f_{SAMP} = \frac{1}{1110ns} = 900.901ksps$$

Table 1 provides the minimum sample period for various configurations of PGA state and bits read out on SDO. **Note:** The channel and gain bits can always be clocked out with the data. If these bits are clocked out, the sample period must be increased to accommodate the additional clock cycles required. Channel bits are clocked out first, from MSB to LSB, followed by the gain bits also from MSB to LSB.

Table 1. Minimum Sample Periods in Normal Mode

PGA	Channel Bits	Gain Bits	Sample Period (µs)
Disabled	No	No	1.11
Disabled	Yes	No	1.17
Enabled	No	No	2.07
Enabled	Yes	Yes	2.19

5.3.2 Low Power Mode Timing

The ISL73148SEH may also be operated in low power mode to reduce total power dissipation or to allow an accurate first sample following initial power-up or on exiting power-down. When operating in lower power mode, the timing requirements are different than normal operation. In low power mode, the acquisition time is directly controlled by the $\overline{CS}$ input. The logic high pulse width on the $\overline{CS}$ input defines the acquisition time. The direct control of the acquisition time by $\overline{CS}$ permits significant power savings especially at lower sampling rates where power dissipation may be less than 50% of that in normal mode. Because the acquisition time is directly controlled by the pulse width of $\overline{CS}$, the minimum pulse width of $\overline{CS}$ in low power mode is 500ns. This is significantly higher than the 150ns required in normal mode. For maximum power savings at low sample rates, Renesas recommends using the minimum $\overline{CS}$ width of 500ns.

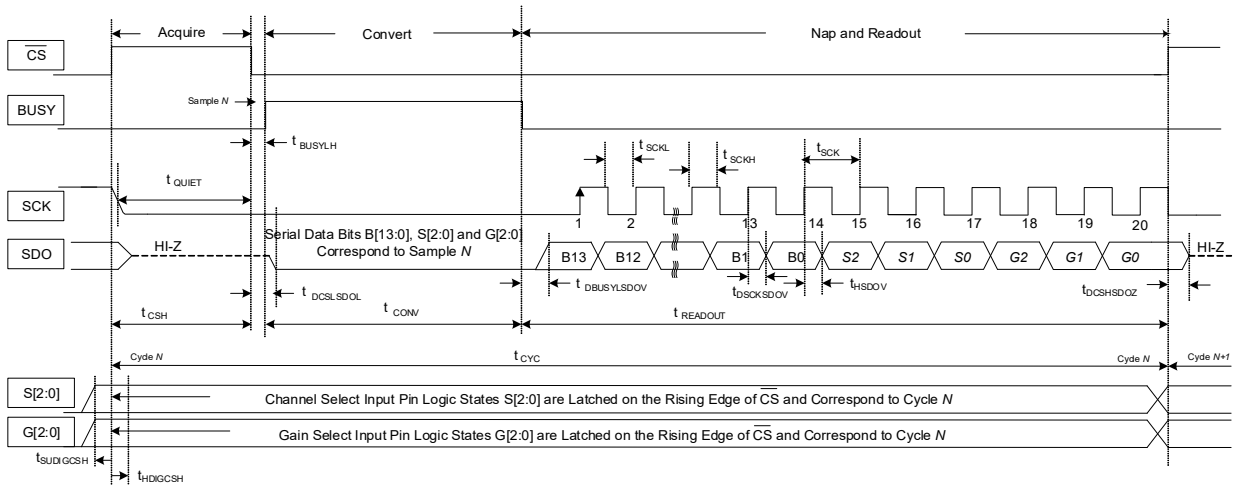


Figure 118. ISL73148SEH Timing Diagram - Low Power Mode

The following is an example of required timing calculation in an application where the ISL73148SEH is operated at its maximum sample rate 684.932ksps in low power mode. For this case, the channel and gain select bits are not clocked out on SDO and the ISL73148SEH is configured in low power mode with the PGA bypassed. The $\overline{CS}$ input must be held high for 500ns (t_{CSH}) in low power mode. The time between the falling edge of $\overline{CS}$ and the rising edge of BUSY is a maximum of 30ns (t_{BUSYLH}). The conversion time (t_{CONV}) is a maximum of 660ns in PGA bypass mode. To clock the data out of the ADC, there must be 14 rising edges of SCK ($t_{READOUT}$). To achieve the maximum sample rate, the 14th SCK falling edge must be coincident with the rising edge of $\overline{CS}$ for the subsequent sample. Using the maximum SCK frequency of 50MHz yields same readout period in low power mode as it is in normal operation:

$$t_{READOUT} = 13 \times 20ns + 10ns = 270ns$$

Note: The 14th SCK edge is coincident with the rising edge of $\overline{CS}$ so there is only a 1/2 period for the 14th SCK. The cycle time is calculated using Equation 2:

(EQ. 2) $$t_{CYC} = t_{CSH} + t_{BUSYLH} + t_{CONV} + t_{READOUT}$$

Using the timing parameters previously discussed, the sampling period and sampling rate when in low power mode is calculated as follows:

$$t_{CYC} = 500ns + 100ns + 660ns + 270ns = 1460ns$$

$$f_{SAMP} = \frac{1}{1460ns} = 684.932ksps$$

With the PGA enabled in low power mode, the timing and sample rate calculate to:

$$t_{CYC} = 500ns + 100ns + 1550ns + 270ns = 2420ns$$

$$f_{SAMP} = \frac{1}{2420ns} = 413.22ksps$$

When the ISL73148SEH has the PGA enabled and the channel and gain selection bits are clocked out on SDO along with the data, there must be additional time alloted resulting in a reduction in the sample rate. The six additional bits require an additional 6 clock cycles of SCK to be clocked out on SDO. In this case, to achieve the maximum sample rate the 20th SCK falling edge must be coincident with the rising edge of $\overline{CS}$ for the subsequent sample. Using the maximum SCK frequency of 50MHz yields:

$$t_{READOUT} = 19 \times 20ns + 10ns = 390ns$$

To accommodate the additional 180ns of read out time, the sample rate of the ISL73148SEH must be reduced. The minimum sample period with the PGA enabled when clocking out the channel and gain selection bits is:

$$t_{CYC} = 500ns + 100ns + 1550ns + 390ns = 2540ns$$

The longer sample period of 2540ns results in a maximum sample rate of:

$$f_{SAMP} = \frac{1}{2540ns} = 393.701ksps$$

Table 2 provides the minimum sample period for various configurations of PGA state and bits read out on SDO. **Note:** The channel and gain bits can always be clocked out with the data. If these bits are clocked out, the sample period must be increased to accommodate the additional clock cycles required. Channel bits are clocked out first, from MSB to LSB, followed by the gain bits also from MSB to LSB.

Table 2. Minimum Sample Periods in Low Power Mode

PGA	Channel Bits	Gain Bits	Sample Period (µs)
Disabled	No	No	1.46
Disabled	Yes	No	1.52
Enabled	No	No	2.42
Enabled	Yes	Yes	2.54

5.3.3 Gain and Channel Select Bits Timing

The logic values present on the channel select pins (S2, S1, and S0) and on the gain select pins (G2, G1, G0) are internally latched on the rising edge of $\overline{CS}$. In normal operation, shown in Figure 117, there is a one sample cycle delay for both the channel and gain settings to be applied. This means that the channel and gain selection bits latched into the ISL73148SEH on sample *n* are applied on sample *n + 1*. In low power mode, shown in Figure 118, the channel and gain select bits are latched on the rising edge of $\overline{CS}$ and applied to the conversion initiated on the next falling edge of $\overline{CS}$. This means that the channel and gain selection bits latched into the ISL73148SEH on sample *n* are applied on sample *n*. Although the channel and gain select signals can be updated by the user at any time before the setup time required before the rising edge of $\overline{CS}$, Renesas recommends not changing the signal state during the conversion process (such as when BUSY is a logic high).

5.3.4 PGA Gain and Analog Input Range

The ISL73148SEH can be operated with the PGA bypassed or with the PGA gain set to a value of either 1, 2, 3, 4, 6, 8, 12, and 16. There is a single PGA in the ISL73148SEH. Therefore, if a different gain is required for each channel, the gain select pins must be changed accordingly. Proper setup and hold times must be met depending on the mode of operation. When operating the ISL73148SEH with bipolar (signed) output data (such as with the COM pin bypassed to ground with 0.1µF ceramic capacitor), the common mode voltage on the analog input should be set to $V_{REF}/2$. The ISL73148SEH may also be operated in unipolar (unsigned) mode in which case the common mode voltage on the analog input should be adjusted based on the gain setting of the PGA. For example, when operating in unipolar mode with a PGA gain of four, the common mode voltage on the analog input should be set to $V_{REF}/8$. In unipolar mode, the common mode voltage should ideally be set to 1/2 the input range.

Table 3. Analog Input Range

PGA Gain Setting	Unipolar Common Mode	Unipolar Input Range	Bipolar Common Mode	Bipolar Input Range
PGA Bypass	1.25V	0V to 2.5V	1.25V	±1.25V
Gain = 1	1.25V	0V to 2.5V	1.25V	±1.25V
Gain = 2	625mV	0V to 1.25V	1.25V	±1.25V
Gain = 3	416.7mV	0V to 833mV	1.25V	±833mV
Gain = 4	312.5mV	0V to 625mV	1.25V	±625mV
Gain = 6	208.5mV	0V to 417mV	1.25V	±417mV
Gain = 8	156mV	0V to 312mV	1.25V	±312mV
Gain = 12	104mV	0V to 208mV	1.25V	±208mV
Gain = 16	78mV	0V to 156mV	1.25V	±156mV

5.3.5 Digital Clamping and Full-Scale Range

The ISL73148SEH has a digital clamp that limits the output code range so that the output code values do not roll over in either the positive (full scale) or negative (zero scale) directions when operating in bipolar mode with the PGA enabled with the gain equal to two or greater. When operating in this mode, the output code range is limited to the range of 10 0000 0000 0000 (-8192) to 01 1111 1111 1111 (8191). In unipolar mode, the digital clamp does not allow the ADC to roll over at zero scale. However, the digital clamp on full scale only applies when operating in bipolar mode with the gain set to a value ≥ 2. The ISL73148SEH does not clamp the full-scale values when operating in unipolar mode regardless of PGA gain or in bipolar mode with a PGA gain of less than two. This means it is possible to see an output code greater than the expected full-scale value under these conditions. This is because of the fact that the ADC core in the ISL73148SEH has a differential input and to exercise the full range of the ADC the data format must be set to bipolar and the PGA gain must equal 2 or greater. The full-scale range for each mode of operation is shown in Table 4. As an example condition, if the ISL73148SEH is configured in

unipolar mode with any gain setting, the output code can go above 8191 if the analog input exceeds the full-scale input voltage (VREF).

Table 4. Full-Scale Range

PGA Gain Setting	Unipolar Mode (Zero Scale)	Unipolar Mode (Full Scale)	Bipolar Mode (Zero Scale)	Bipolar Mode (Full Scale)
PGA Bypass	0[1]	8191	-4096	4095
Gain = 1	0[1]	8191	-4096	4095
Gain ≥ 2	0[1]	8191	-8192[1]	8191[1]

1. Digitally clamped.

5.3.6 Input Channel Sequencer (SCAN Mode)

The ISL73148SEH features an internal sequencer which, when enabled, cycles through all eight channels from CH0 to CH7, repeating while SCAN is asserted. The SCAN input acts as a digital gating window for the sequencing function. The first sample after SCAN is asserted in normal mode is an initialization cycle. The second sample after SCAN is asserted should be ignored. The channel sequence begins with the sampling of CH0. The sampling instant for CH0 occurs on the second falling edge of $\overline{CS}$ following the rising edge of SCAN as shown in Figure 119, which ensures a full acquisition period for the sample of the CH0 analog input. Subsequent rising edges of $\overline{CS}$ increment the sequencer to acquire the next channel (such as CH1, CH2,...CH7). Following CH7, the sequencer returns to CH0. The SCAN pin should be asserted for the duration of the required sequence. The gain selection (G2, G1, G0) values are clocked in on the rising edge of $\overline{CS}$ on sample *n* and apply to sample *n+1* as show in Figure 119. When the SCAN pin is de-asserted, the channel select inputs (S2, S1, S0) resume control of the active channel. While SCAN is asserted, the channel select inputs (S2, S1, S0) are ignored.

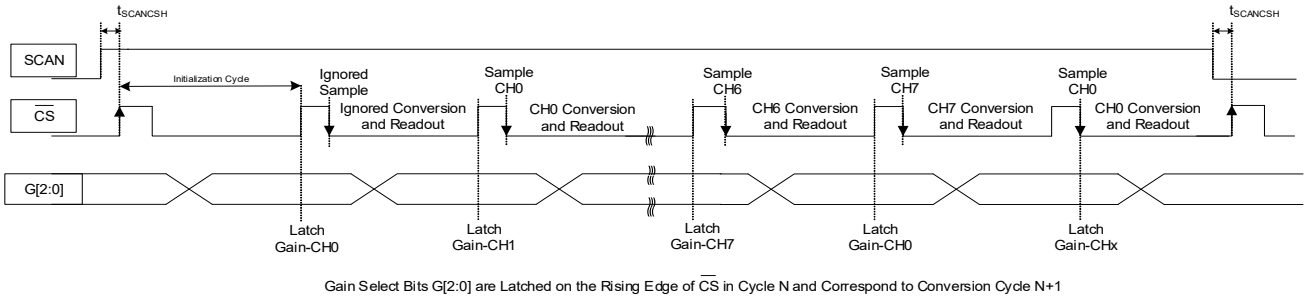


Figure 119. ISL73148SEH SCAN and Gain Select Timing Diagram - Normal Mode

When SCAN mode is selected while operating the ISL73148SEH in low power mode (LPM enabled), the sample following the first rising edge of $\overline{CS}$ where SCAN is asserted should be ignored. The sampling instant for CH0 occurs on the second falling edge of $\overline{CS}$ following the rising edge of SCAN as shown in Figure 120, ensuring a full acquisition period for the sample of the CH0 analog input. Subsequent rising edges of $\overline{CS}$ increment the sequencer to acquire the next channel (such as CH0, CH1,...CH7) as shown in Figure 120. Following CH7, the sequencer returns to CH0. The SCAN pin should be asserted for the duration of the required sequence. The gain selection (G2, G1, G0) values are clocked in on the rising edge of $\overline{CS}$ on sample *n* and apply to sample *n* as shown in Figure 120. When the SCAN pin is de-asserted, the channel select inputs (S2, S1, S0) resume control of the active channel. While SCAN is asserted, the channel select inputs (S2, S1, S0) are ignored.

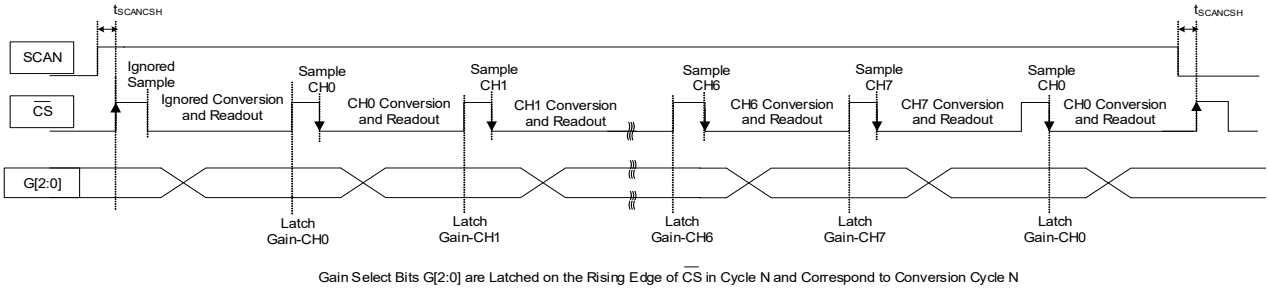


Figure 120. ISL73148SEH SCAN and Gain Select Timing Diagram - Low Power Mode

In both normal operation and low power modes of operation, the ISL73148SEH the data readout on SDO in SCAN mode is performed with the same timing as given in Figure 117 and Figure 118. The active channel and gain settings for the conversion can still be optionally read out following the LSB (adjusting the sample rate period accordingly). When in SCAN mode, the active channel bits correspond to the sequencer selected channel and not the channel input pin states (S2, S1, and S0). Gain can be adjusted when operating in SCAN mode as long as the specified setup and hold times are obeyed. Gain settings are applied to the current sample in lower power mode and are applied one cycle later in normal operation mode as shown in Figure 117 and Figure 118. When SCAN is de-asserted, the sample at the subsequent rising edge of $\overline{CS}$ is from the last channel selected by the sequencer. For example, if SCAN is de-asserted when the sequencer is selecting CH1, the next sample is CH2. Following the CH2 sample, the output channel selection is driven by the channel select pins (S2, S1, S0).

5.4 Convert Start ($\overline{CS}$) Pin

The convert start input ($\overline{CS}$) initiates a conversion in the ISL73148SEH. The input logic level of $\overline{CS}$ is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. A falling edge on this input starts a new conversion. The conversion is timed using an internal oscillator. The logic state of the $\overline{CS}$ pin controls the state of the SDO pin. A logic high on the $\overline{CS}$ pin disables the SDO pin driver resulting in a high-impedance state on the SDO pin. A logic low on the $\overline{CS}$ pin enables the SDO driver (unless $\overline{PD}$ is low) and allows data to be read out following a conversion. Renesas recommends using a low jitter (low phase noise) source to provide the input to this pin. Exact jitter requirements depend highly on the acceptable noise in a given application. This pin should be held low at power-up and when in power-down or the device is inactive.

5.5 Power-Down ($\overline{PD}$) Pin

The ISL73148SEH has a separate power-down pin that is active low ($\overline{PD}$). Anytime the ISL73148SEH is powered up and operated statically without a required conversion (CSB held low), this pin should be asserted. When this pin is asserted, the ISL73148SEH is powered down to ≤115µW of total power dissipation. If $\overline{PD}$ is asserted during a conversion, the conversion is halted, and the SDO pin is held in high impedance (high-Z). The ISL73148SEH is brought out of power-down mode by de-asserting $\overline{PD}$. When operating the ISL73148SEH in normal mode (LPM = 0V), there is a one-sample delay before output data is valid and the channel and gain selections are applied (see Figure 117). When operating the ISL73148SEH in low power mode (LPM = DV_{CC}), the sample on the first rising edge of $\overline{CS}$ is valid, and the channel and gain selections are applied to that sample (see Figure 118). The wake-up time for the ISL73148SEH to come out of power-down and be ready to begin sampling is specified in the electrical tables as Wake-Up time from Power-Down Mode. The input logic level of $\overline{PD}$ is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. There is an internal 500kΩ pull-up resistor connected to DV_{CC} on this pin.

5.6 Reference Input (REF) Pin

The ISL73148SEH has a voltage reference input that determines the full-scale input range. The input voltage range of this pin is from 2.4V up to 2.6V. Decouple this pin to ground with a high quality, low ESR 10µF ceramic

capacitor. Renesas recommends using a capacitor with a voltage rating of 10V or greater and to place the capacitor as close as possible to the REF pin.

Use a low noise, low temperature drift reference to drive this pin. Input noise from the input reference directly impacts the noise performance of the device. Temperature drift of the external reference affects the full-scale error performance over temperature for the ISL73148SEH. Exact specifications for the noise and temperature drift requirements depend heavily on the application. As an example, the ISL73148SEH evaluation board uses a 2.5V voltage reference with a typical output noise voltage of 1.9µV_{P-P} and a maximum temperature coefficient of 7ppm/°C.

5.7 Common Input (COM) Pin

The ISL73148SEH has a common input pin for the complementary analog input. For bipolar operation, the COM pin should be floated and bypassed to ground with a 0.1µF ceramic capacitor. Alternatively, for unipolar operation, the COM pin should be tied directly to ground (GND). When operating the ISL73148SEH in unipolar mode, it is important that a low-impedance connection to the PCB ground plane is maintained. If not properly connected to the ground plane to maintain a voltage of 0V, the output codes can be affected. For more information on the analog input range in bipolar and unipolar modes, see the Analog Input Range table in PGA Gain and Analog Input Range. The COM pin is internally referenced to the voltage at the REF pin (VREF). The equivalent circuit for the COM pin is shown in Figure 121. The output voltage of the COM pin is factory trimmed to precisely set the value to $V_{REF}/2$ when operating in bipolar mode.

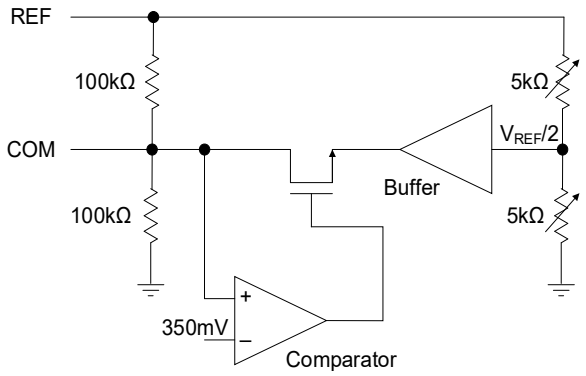


Figure 121. ISL73148SEH COM Pin Equivalent Circuit

5.8 Low Power Mode (LPM) Pin

The ISL73148SEH has a low power mode (LPM) pin that can be asserted high to enable the device to operate in a mode with significantly lower power dissipation especially at lower sample rates. Low power mode also offers accurate sampling immediately, following initial power-up or when exiting from power-down mode. To enter low power mode, the ISL73148SEH must be powered up and at least one sample must be acquired with the LPM pin asserted. The input logic level of LPM is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. There is an internal 500kΩ pull-down resistor connected to GND on this pin.

5.9 SCAN Pin

The ISL73148SEH has a SCAN pin that enables an internal sequencer that controls the channel selection. When the SCAN pin is asserted high, the sequencer is enabled and the device sequences through the eight input channels beginning on next rising edge of $\overline{CS}$. The channel selection begins with CH0 and consecutively selects through all eight channels up to CH7 on each subsequent rising edge of $\overline{CS}$. As long as SCAN is asserted high, the ISL73148SEH continues to sequence through the eight input channels consecutively from CH0 to CH7 on each rising edge of $\overline{CS}$. While SCAN is asserted, the channel selection pins (S2, S1, and S0) are ignored. The input logic level of SCAN is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V.

5.10 Channel Selection (S2, S1, and S0) Pins

The ISL73148SEH has three channel selection input pins: S2, S1, and S0. These three pins determine which of the analog input channels, CH0 to CH7, are selected. If the SCAN pin is asserted, the channel selection input pins are ignored. The channel selection is determined by the logic states of pins S2, S1, and S0 and are shown in Table 5. The input logic level of the S2, S1, and S0 pins is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. These inputs are ignored when the SCAN pin is asserted.

Table 5. Channel Selection Logic (S2, S1, S0)

S2	S1	S0	Channel
0	0	0	CH0
0	0	1	CH1
0	1	0	CH2
0	1	1	CH3
1	0	0	CH4
1	0	1	CH5
1	1	0	CH6
1	1	1	CH7

5.11 Gain Selection (G2/PGABP, G1, and G0) Pins

The ISL73148SEH has three gain selection input pins: G2/PGABP, G1, and G0. These three pins determine the gain setting of the PGA. The gain selection of the PGA is determined by the logic states of pins G2/PGABP, G1, and G0 and are shown in Table 6. When G2/PGABP is put into a high impedance (high-Z) condition, the PGA is bypassed and pins G1, G0 are ignored. When using the G2/PGABP pin to bypass the PGA, the pin should not be switched dynamically during operation to set the configuration of the PGA. A 100pF capacitor should be placed from G2/PGABP to ground when bypassing the PGA. When the PGA is configured in bypass mode, adequate time should be given at device power-up for the G2/PGABP voltage level to settle. This is determined by the RC time constant of the external 100pF capacitor and the internal resistance of the G2/PGABP pin, which can be up to 300kΩ. This means that at device power-up you should wait at least 100pF × 150kΩ = 15µs before acquiring sample data. **Note:** The 15µs time constant is less than the typical wait time specified from power-down (t_{WAKE}) of 20µs. The gain (including the G2/PGABP pin) can be adjusted dynamically during operation so long as setup and hold times are met with or without the sequencer being enabled (sequencer is enabled when SCAN is asserted to a logic high). The input logic level of the G2/PGABP, G1, and G0 pins is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V.

Table 6. Gain Selection Logic (G2/PGABP, G1, G0)

G2/PGABP	G1	G0	Gain
High-Z	X	X	Bypass
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	6
1	0	1	8
1	1	0	12
1	1	1	16

5.12 Transfer Function

Figure 122 gives the transfer function of the ISL73148SEH when operating in bipolar mode and in unipolar mode. Code transitions in the digital outputs bits of the device occur at midway points between successive integer LSB values that range from 0.5 LSB, 1.5 LSB, 2.5 LSB, 3.5 LSB... and FS - 3.5 LSB, FS - 2.5 LSB, FS - 1.5 LSB, FS - 0.5 LSB. To exercise the full 14-bit range of the ADC, the ISL73148SEH must be operated in bipolar mode with the PGA gain set to a value of 2 or higher. Operating the ISL73148SEH in unipolar mode with any gain setting, in bipolar mode with the PGA bypassed, or in bipolar mode with a PGA gain setting of one results in the ADC operating with a 13-bit effective range.

When the COM pin is floated and bypassed to GND with a 0.1µF capacitor, the device operates in bipolar mode. In bipolar mode, the output data is in two's complement format. With the PGA gain set to a value of 2 or greater, the device operates as a 14-bit ADC with an output code range in two's complement from $-2^{(N-1)}$ to $2^{(N-1)}-1$ where N = 14, making the total code range -8192 to 8191 inclusive. With the PGA bypassed or set to a gain of one the devices operates effectively as a 13-bit ADC because the input range to the ADC is only 1/2 scale. In this case, the output code range in two's complement from $-2^{(N-1)}$ to $2^{(N-1)}-1$ where N = 13, making the total code range -4096 to 4095 inclusive.

With the COM pin tied to GND, the device operates in unipolar mode. The device operates effectively as a 13-bit ADC with an output code range in decimal from 0 to 2^N-1 where N = 13, making the total code range 0 to 8191 inclusive.

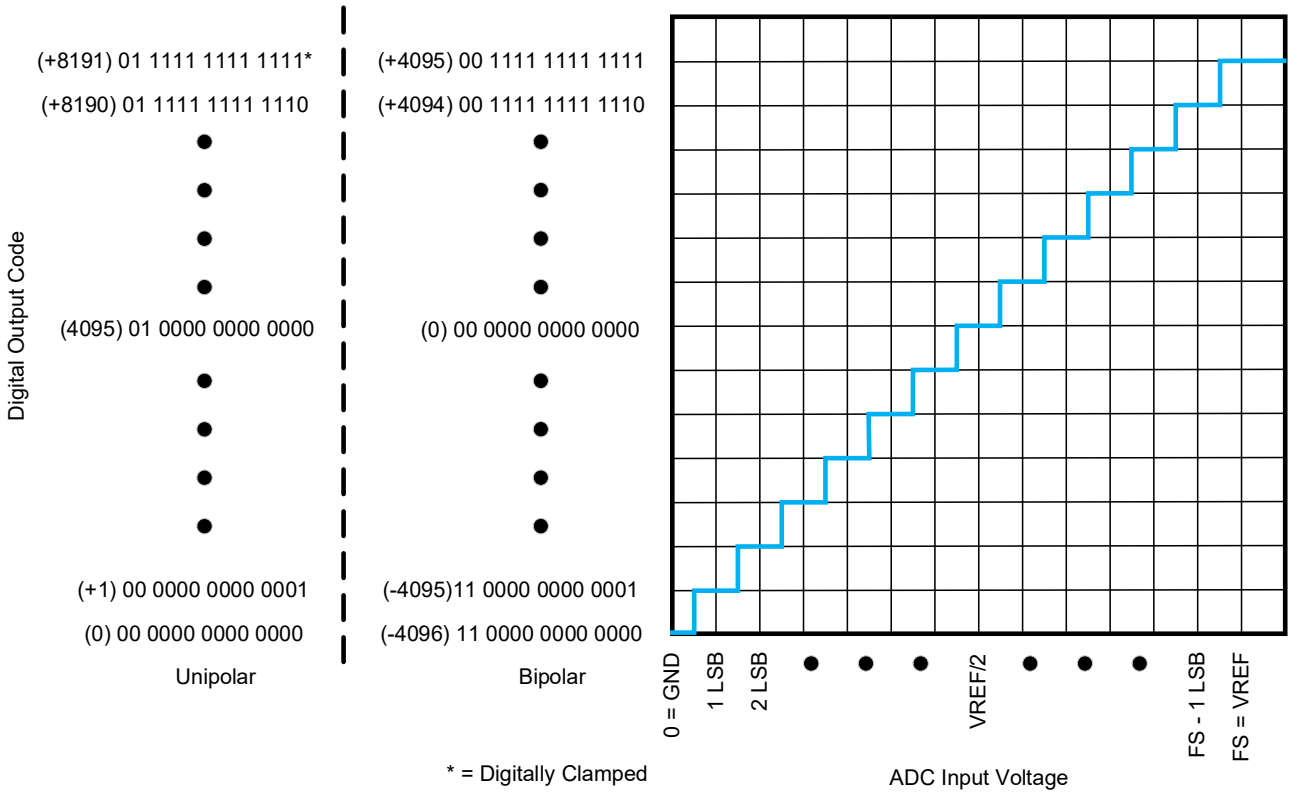


Figure 122. ISL73148SEH Transfer Function - Unipolar (All Gains) and Bipolar (Gain = 1) Operation

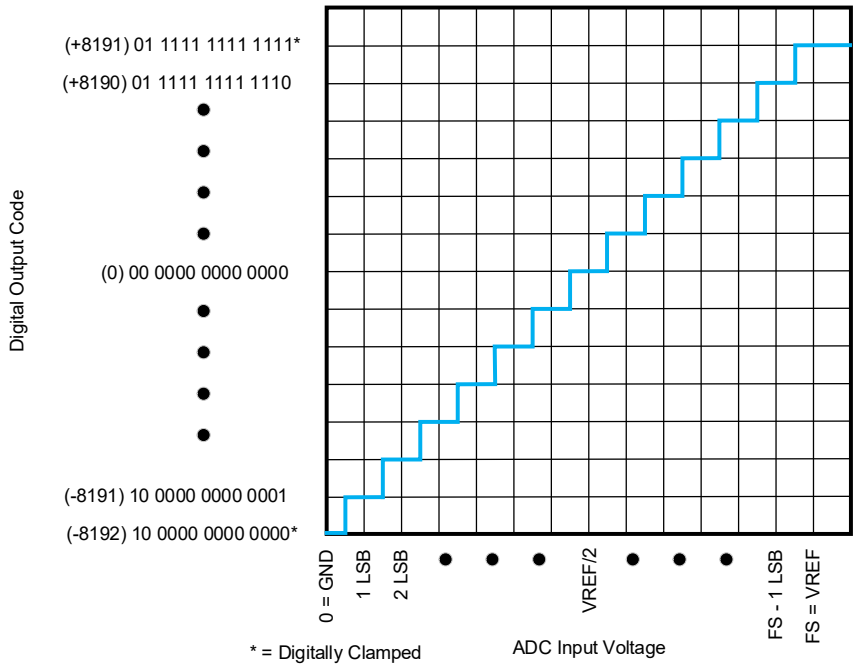


Figure 123. ISL73148SEH Transfer Function - Bipolar (Gain ≥ 2) Operation

5.13 Power Supply Sequencing

The ISL73148SEH does not have any specific power sequencing requirements. **Important:** You must follow the guidelines in the recommended operating conditions and take care in observing the maximum supply voltage conditions set forth in the Absolute Maximum Ratings section.

5.14 CH0 - CH7 Analog Input Pins

The analog input pins are independently buffered and exhibit high input impedance (1GΩ) and low input capacitance (3pF) to ease input drive requirements. Any unused input pins should always be terminated using a 50Ω resistor to ground.

The ISL73148SEH supports single-ended input drive only. ***Important:*** Ensure that proper grounding techniques and supply decoupling are used in circuit board layout to achieve optimum performance. The ISL73148SEH evaluation board can be used as a guide for proper circuit optimization. The analog input channels feature a high-impedance input that exhibits an equivalent load of approximately 3pF and 1GΩ. Because of the high bandwidth (50MHz) of the analog input, Renesas recommends using an Anti-Alias Filter (AAF) appropriate for the required application. Any unused input channels should be terminated using a 50Ω resistor to ground. It is not required to operate the ISL73148SEH with an input amplifier because the device has an integrated PGA, but it can ease input common mode biasing and/or provide additional gain in certain applications. An example topology is given in Figure 124, which uses a driver amplifier and an RC input filter. Care must be taken to choose an amplifier with low noise and distortion because the ADC performance is directly impacted. It is also important to choose feedback resistance values that are less than 1kΩ (typically, 100Ω to 200Ω) to minimize the impact of resistor thermal noise. The noise of the resistor is directly related to its value by Equation 3.

(EQ. 3) $\text{Power Spectral Density (PSD)} = 4kTR\ (V^2/Hz)$

where

- k = Boltzmans constant (1.38×10^{-23})
- T = Temperature in Kelvin (room temperature = 27°C = 300K)
- R = Resistance value

At the input to the ADC, a simple RC filter should be sufficient for most applications. Choose the RC circuit values appropriately for the application. A low-value resistor ($R_S \leq 50$) is recommended for low noise performance. Add a high-quality shunt capacitor (C_P) as close as possible to each channel input pin to limit the input bandwidth to the ISL73148SEH. This capacitor should have a low ESR value with a low temperature and voltage coefficient. The exact requirements depend highly on the application and the signal(s) being sampled. The recommended value for the C_P is 20-50pF. Larger values for C_P can be used for slower conversion rates.

Note: Large values of shunt capacitance are not required to squelch charge kickback from the multiplexer or the ADC because each analog input is independently buffered.

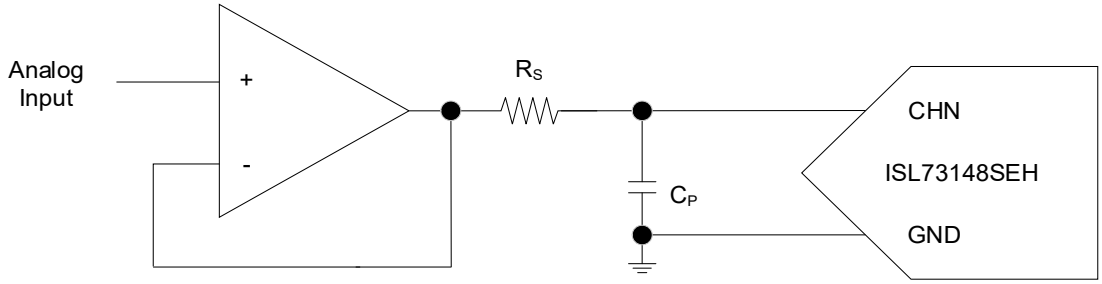


Figure 124. ISL73148SEH Analog Input Amplifier Example Circuit

Renesas recommends using a high quality ceramic capacitor (C_P) in shunt on the analog input that is at an appropriate value for the required application. Choose the series resistance in the analog input circuit based on the output impedance of the driver amplifier and the input bandwidth requirements. An example topology is given in Figure 125, which converts a 0V input common-mode voltage to the ADC input common-mode voltage of $V_{REF}/2$. This circuit is employed on the ISL73148SEH evaluation board to allow the ADC to be driven from various types of signal generators.

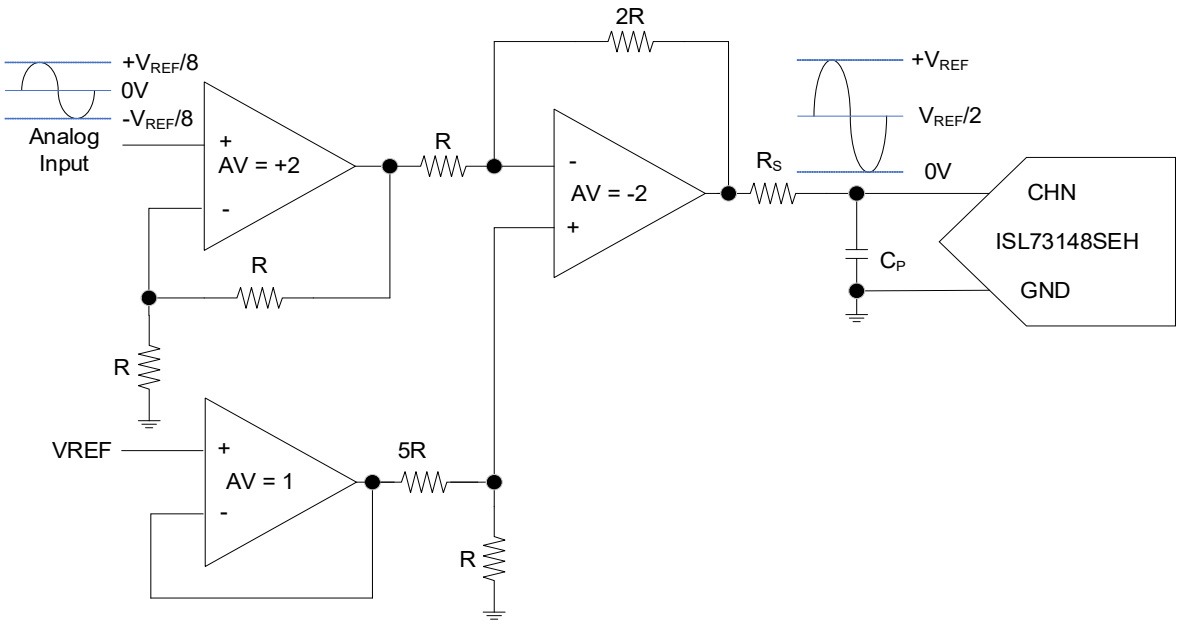


Figure 125. ISL73148SEH Common-Mode Conversion Amplifier Example Circuit

It is important to understand the settling time associated with the analog input of the ISL73148SEH and the impacts of R_S and C_P. To allow the ISL73148SEH to accurately resolve the input signal, it is important that the input signal is settled completely before the signal is sampled by the ISL73148SEH. To meet the datasheet

specifications, the settling time must be met for the input signals on the analog input of the ISL73148SEH. To accurately resolve to 1 LSB, the settling time is defined by Equation 4:

(EQ. 4) $$\frac{1}{2^N} = e^{-t/\tau}$$

Simplifying this results in Equation 5:

(EQ. 5) $$\ln(2^N) = -\frac{t}{\tau}$$

Solving for t results in:

$t = -\tau \times \ln(2^N)$, which can be written as $t = N \times \tau \times \ln(2)$ and further simplified to $t = 0.693 \times N \times \tau$.

Settling time is t, $R_S \times C_P$ is τ, and the resolution of the ADC is N.

The ISL73148SEH is a 14-bit ADC, which means the settling time to attain 1 LSB accuracy is 9.7 × τ. For example, the ISL73148SEHEV1Z evaluation board employs a 24Ω resistor for R_S and a 47pF capacitor for C_P, which means that the required settling time would be t = 0.693 × 14 × 24Ω × 47pF = 10.94ns. If different R_S and C_P values are used, calculate the settling time for those conditions. These calculations assume the settling time of the input network R_S and C_P are much larger than the settling time of any amplifier driving the ISL73148SEH analog input. If this is not the case, the settling time of the input network must be root-sum-squared with the settling time of the amplifier to determine the required settling time using Equation 6:

(EQ. 6) $$t = \sqrt{(t_{AMP})^2 + (t_{RC})^2}$$

5.15 Static Power Dissipation

The ISL73148SEH can be placed into an operating mode where the device is ready to initiate a sample, but where the power consumption is considerably reduced. While operating in normal mode, this low static power state can be entered on initial power up by holding $\overline{CS}$ low or by holding $\overline{CS}$ low and asserting/de-asserting the $\overline{PD}$ pin. While operating in low power mode, the ISL73148SEH must be powered up and have at least one sample acquisition in with the LPM pin asserted to place the device into low power mode. Subsequently, the ISL73148SEH can enter a low static power state by holding $\overline{CS}$ low and asserting/de-asserting the $\overline{PD}$ pin.

5.16 Cold Sparing Operation

The ISL73148SEH can be used in applications that require connections to multiple input devices with only one active at a given time, which is commonly referred to as cold sparing. The analog input of the ISL73148SEH connects to an 8-channel multiplexer with high impedance inputs. Only one channel can be selected at a given time for sampling. In many cold-sparing applications, the unused devices connected to the unused channels are completely powered down with the supply voltage removed. However, for the ISL73148SEH any device connected to any one of the eight analog inputs should be provided a supply voltage, but may be placed into power-down mode using the $\overline{PD}$ pin of the individual device.

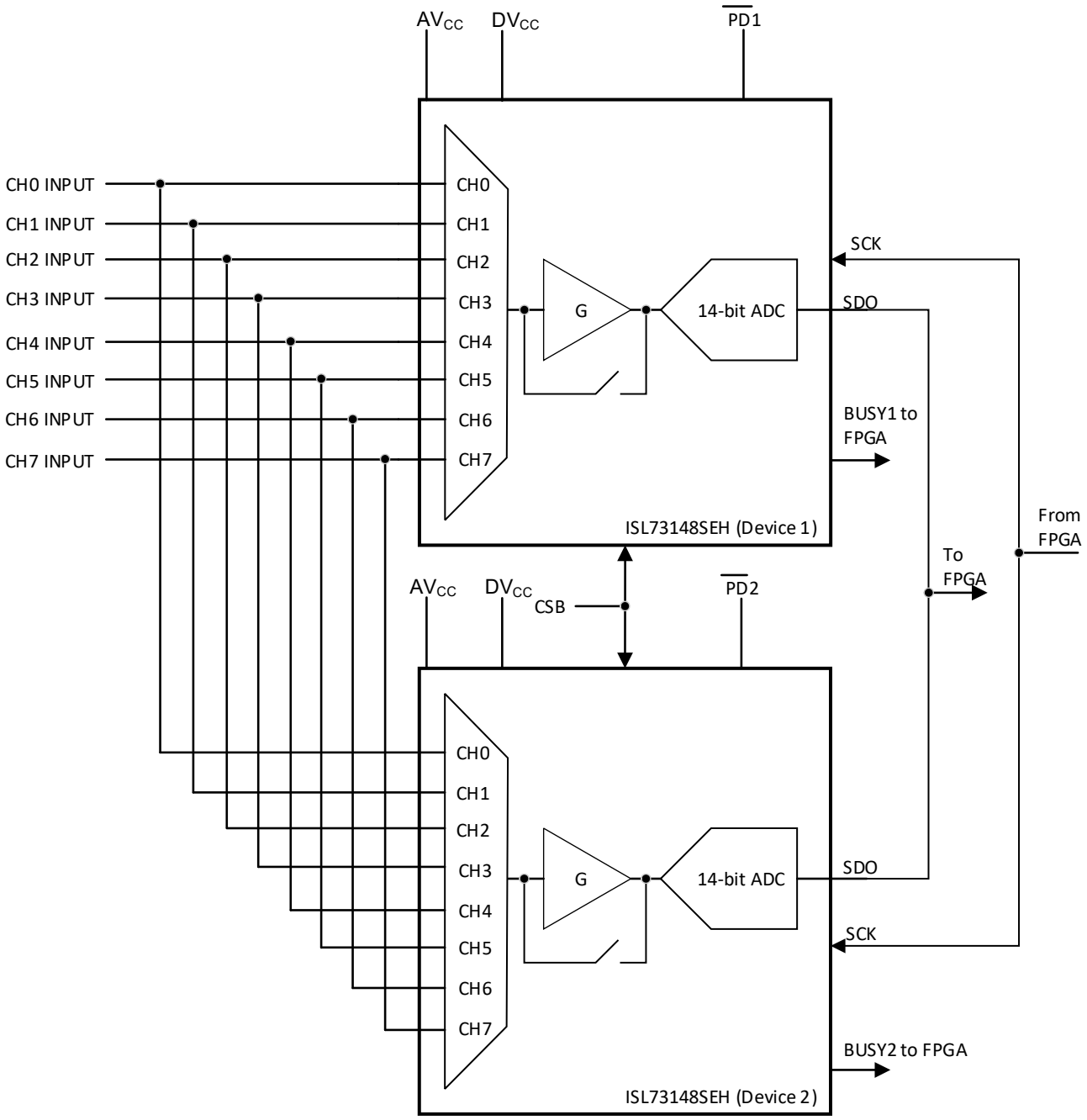


Figure 126. ISL73148SEH Cold Sparing Example Circuit

5.17 Configuration Examples

The ISL73148SEH can be used in a variety of applications that require that the device be set up in a particular configuration. There are several ways to configure the ISL73148SEH so that it may provide the best performance for a given application. A key configuration parameter for the ISL73148SEH is the data format. The ISL73148SEH can operate with a bipolar (signed) data format or a unipolar (unsigned) data format. When operating the ISL73148SEH in bipolar data format, the input common mode should always be set to VREF/2 (1.25V) and the COM input should be left floating and decoupled to ground with a 0.1µF ceramic capacitor. When operating the ISL73148SEH in unipolar data format, the input common mode should be set to (VREF/2)/(PGA Gain) and the COM input should be connected to ground.

Note: In the following examples given in section Normal Mode, PGA Gain, Bipolar Format through Operating with Unipolar Format, an arbitrary channel is chosen. However, any channel can be used or the ISL73148SEH can be placed in SCAN mode where all eight channels are selected sequentially in a repeating mode (see Input Channel Sequencer (SCAN Mode) for more details on SCAN mode).

5.17.1 Normal Mode, PGA Gain, Bipolar Format

In applications that require the most analog input range and highest sample rate from the ADC, the ISL73148SEH can be configured into normal mode setting the PGA gain to a value of 2 or greater and the data format set to bipolar. This gives you the ability to use the full input range (0V - 2.5V) and the full output code range of the ISL73148SEH (+8191/-8192). The ADC core in the ISL73148SEH has a differential input; therefore, requiring a PGA gain of at least two to use its full range. As an example, to select this operating mode with a PGA gain of two using Channel 1 of the ISL73148SEH, the pin configuration should be as follows:

Table 7. ISL73148SEH Selection Logic

S2	S1	S0	G2/PGABP	G1	G0	COM	LPM
0	0	1	0	0	1	Floating	0

5.17.2 Normal Mode, PGA Bypassed, Bipolar Format

In applications that require the highest sample rate from the ADC, but where the full input range is not required, you can configure the ISL73148SEH into normal mode with the PGA bypassed and the data format to bipolar. An input signal can still be applied to one of the eight channels with a voltage up to the full input range (0V - 2.5V), but the output code range from the ADC is reduced by 1/2 (+4095/-4096). As an example, to select this operating mode with the PGA bypassed using Channel 4 of the ISL73148SEH, the pin configuration should be as follows:

Table 8. ISL73148SEH Selection Logic

S2	S1	S0	G2/PGABP	G1	G0	COM	LPM
1	0	0	Hi-Z	X	X	Floating	0

5.17.3 Low Power Mode, PGA Enabled, Bipolar Format

In applications that require lower power consumption and where a lower sample rate is sufficient, the ISL73148SEH can be configured into low power mode. In this example, the most full analog input range is used when the PGA gain is set to a value of two or greater and the data format set to bipolar. This gives you the ability to use the full input range (0V - 2.5V) and the full output code range of the ISL73148SEH (+8191/-8192). Although the sample rate is only slightly reduced in low power mode, the power consumption is significantly reduced, especially for lower sample rates. As an example, to select this operating mode with a PGA gain of four using Channel 1 of the ISL73148SEH, the pin configuration should be as follows:

Table 9. ISL73148SEH Selection Logic

S2	S1	S0	G2/PGABP	G1	G0	COM	LPM
0	0	1	0	1	1	Floating	1

5.17.4 Low Power Mode, PGA Bypassed, Bipolar Format

In applications that require lower power consumption where a lower sample rate is sufficient and the full analog input range of the ADC is not required, the ISL73148SEH can be configured into low power mode with the PGA bypassed and the data format set to bipolar. This gives you the ability to use the full input range (0V - 2.5V) but with half the output code range of the ISL73148SEH (+4095/-4096). The sample rate is only slightly reduced compared to normal mode with the PGA bypassed and the power consumption is significantly reduced. As an example, to select this operating mode using Channel 5 of the ISL73148SEH, the pin configuration should be as follows:

Table 10. ISL73148SEH Selection Logic

S2	S1	S0	G2/PGABP	G1	G0	COM	LPM
1	0	1	Hi-Z	X	X	Floating	1

5.17.5 Operating with Unipolar Format

In applications that require an output code in unipolar format, the ISL73148SEH can be configured to accommodate this condition. When operating the ISL73148SEH in unipolar format, care must be taken to maintain an appropriate common mode bias on the analog inputs regardless of channel selection and power mode (normal or low power). For example with the PGA gain set to a value of 4, the input common mode voltage on the analog inputs should be set to (VREF/2)/4 = VREF/8 = 0.15625V (when VREF = 2.5V). When operating in unipolar format, the output range of the ISL73148SEH is 0 to 8191 regardless of the PGA gain setting (*Note:* there are no negative output codes in unipolar mode). As an example, to select this operating mode with normal mode and a PGA gain of four using Channel 2 of the ISL73148SEH, the pin configuration should be as follows:

Table 11. ISL73148SEH Selection Logic

S2	S1	S0	G2/PGABP	G1	G0	COM	LPM
0	1	0	0	1	1	GND	0

5.17.6 Dual Footprint ISL73148SEH/ISL71148

The ISL73148SEH can be configured in a dual footprint configuration with the ISL71148M/ISL71148SLH in a single-ended application. The configuration is shown in Figure 127.

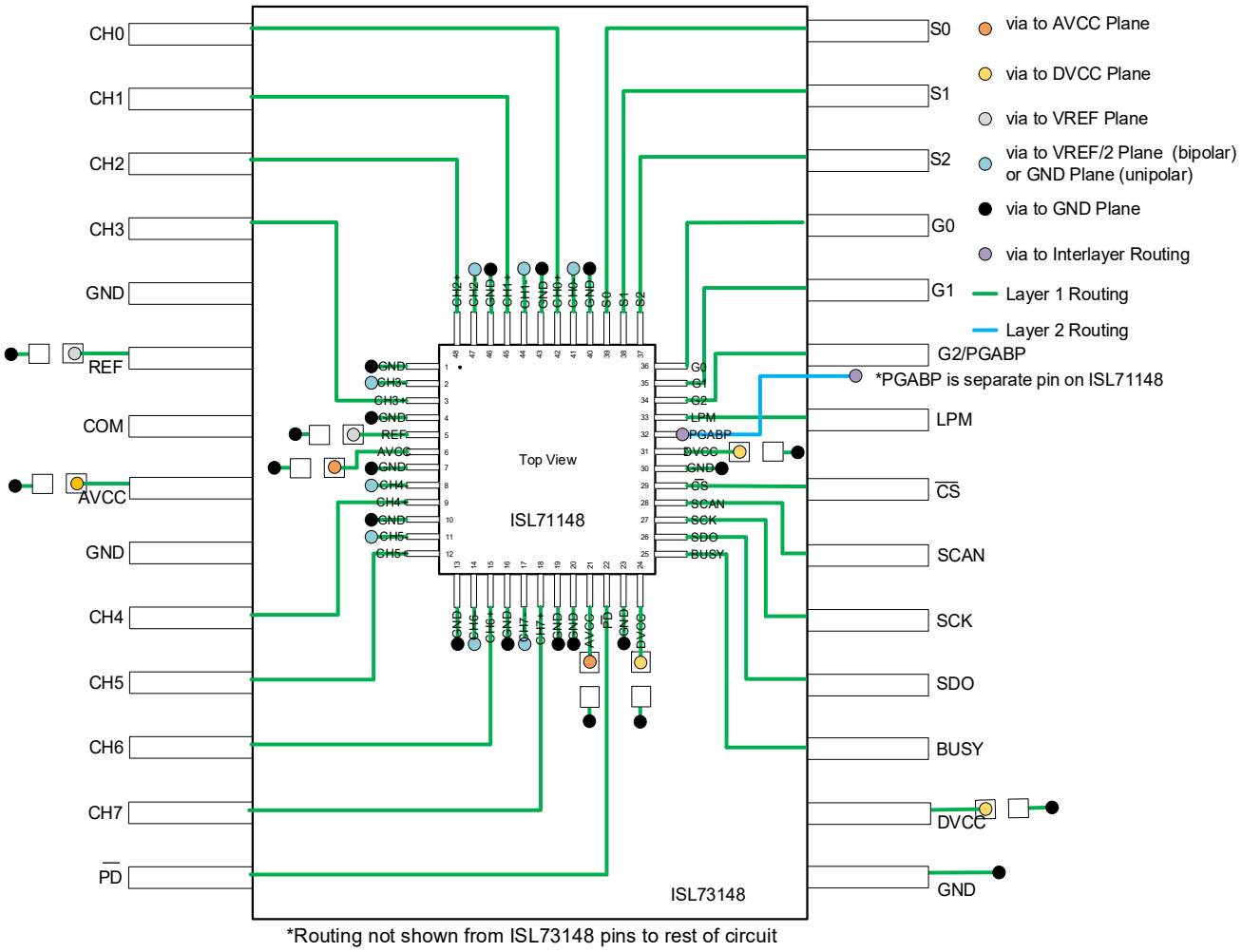


Figure 127. Dual Footprint ISL73148/ISL71148

5.18 Package

The ISL73148SEH is available in a 28 Ld hermetically sealed Ceramic Dual Flatpack (CDFP) package (see Package Outline Drawing). Pin 15 (DGND) is electrically connected to the package seal ring and the package lid.

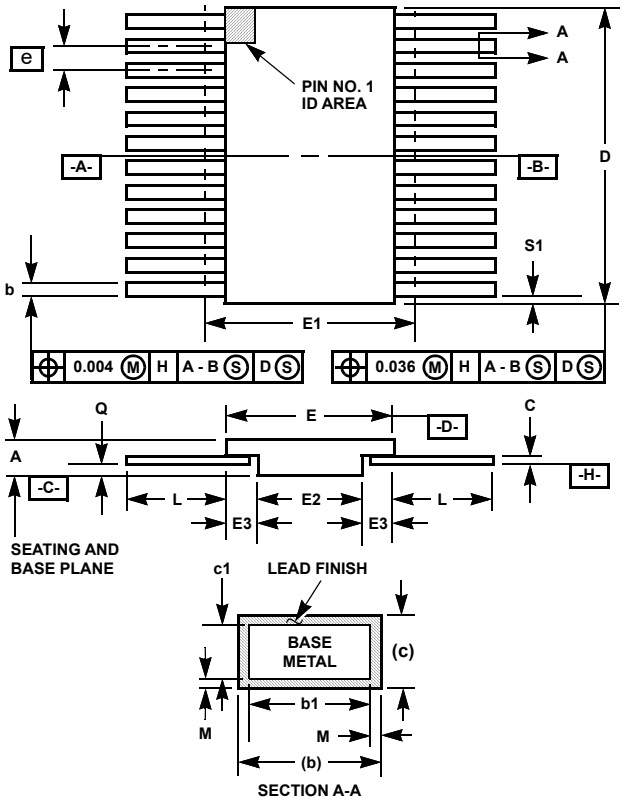
6. Die and Assembly Characteristics

Table 12. Die and Assembly Related Information

Die Information	
Dimensions	4495µm x 4495µm (177 mils x 177 mils) Thickness: 482.6µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Passivation	Oxide/Nitride Total Thickness 24.5kÅ
Top Metallization	Top metal/Bond Pad Composition 99.5% Al, 0.5%Cu
Process	0.25µm CMOS
Assembly Information	
Substrate Potential	GND
Additional Information	
Transistor Count	142139
Weight of Packaged Device	2.15g (typical) - K28.A package
Lid Characteristics	Finish: Gold Lid Potential: Connected to package Pin 15 (DGND)

7. Package Outline Drawing

For the most recent package outline drawing, see K28.A.



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, Configuration B)
28 Lead Ceramic Metal Seal Flatpack Package (CDFP)

SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		29		-

Rev. 0 5/18/94

Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

8. Ordering Information

Part Number[1]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
ISL73148SEHMF	LDR to 75krad(Si)	28 Ld CDFP Packaged Device (QML-V Level Screening)	K28.A	Tray	-55 to +125°C
ISL73148SEHF/PROTO[2]	N/A	28 Ld CDFP Packaged Device			
ISL73148SEHEV1Z[3]	Single IC Evaluation Board for ISL73148SEH				

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The /PROTO is not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in this datasheet. These part types do not come with a Certificate of Conformance.
3. Evaluation board uses /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effects (SEE) immunity.

9. Revision History

Rev.	Date	Description
1.09	May 30, 2025	Added Dual Footprint ISL73148SEH/ISL71148 section.
1.08	Apr 23, 2025	In the Electrical Specifications, corrected the units for Negative Full-Scale Error and Negative Full-Scale Error Drift.
1.07	Jan 31, 2025	Added SCAN to the list of pins in the Abs Max section for the Digital Input Voltage spec and in the I/O Specifications table for the first subheading and Input Current parameter.
1.06	Nov 15, 2024	Updated Circuit 2 drawing. Updated Channel Voltage Abs Max spec. Added CH0-CH7 Input Current Abs Max spec. Updated the Cold Sparing Example Circuit figure.
1.05	May 1, 2024	Updated Feature bullets. Updated Boldface statements in the Electrical Specifications sections. Updated the Overview section. Updated the Normal Operation Mode Timing section. Updated the Low Power Mode Timing section. Updated the Transfer Function section. Updated Figure 126.
1.04	Apr 20, 2023	Updated test conditions for Input Bandwidth from 25Ω to 50Ω in the ISL73148SEH - Normal Operating Mode section.
1.03	Feb 23, 2023	Added Features bullet. Updated Ordering Information table package descriptions.
1.02	Oct 27, 2022	Updated Figures 23, 24, 67, and 68.
1.01	Sep 20, 2022	Changed radiation tolerant to radiation hardened throughout the document. Corrected /PROTO part number in the ordering information table.
1.00	Aug 10, 2022	Initial release

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