ISL72991RH

Radiation Hardened Low Dropout Adjustable Negative Voltage Regulator

FN9054
Rev.7.01
Jun 16, 2022

The radiation hardened ISL72991RH is a low dropout adjustable negative regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (ILIM), and a shutdown pin (SD) for easy on/off control.

The device incorporates unique circuitry that enables precision performance across the -55°C to +125°C temperature range and post-irradiation. Specifications across the full temperature range include an internal reference voltage of -1.25V +40mV/-50mV (maximum), line regulation of ±25mV (maximum), and load regulation of ±15mV (maximum). The reference voltage is the ADJ to GND voltage.

Constructed with the dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Applications

- Post switching power supplies
- DC/DC converters
- Motor controllers

Features

- Electrically screened to DLA SMD # 5962-02503
- QML qualified per MIL-PRF-38535 requirements
- Latch-up immune DI process
- Wide input voltage range . . . . . -3V to -30V
- Nominal output voltage range . . . . . -2.25V to -26V
- Line regulation. . . . . ±25mV (maximum)
- Load regulation . . . . . ±12mV (typical); ±15mV (maximum)
- Dropout voltage (100mA) . . . 0.2V (typical); 0.3V (maximum)
- Dropout voltage (1A) . . . . . 1V (maximum)
- Minimum load current. 3.0mA
- 5V-12V TTL input-level shutdown (SD); low or floating = on; high = off
- Operating temperature range. . . . . -55°C to +125°C
- Radiation acceptance testing
  - HDR (50-300rad(Si)/s):. . . . . 300krad(Si)
- SEE hardness (see SEE report for details)
  - SEL/SEB LET_{TH} (V_S = -30V) . . . . . 86.4MeV•cm^2/mg

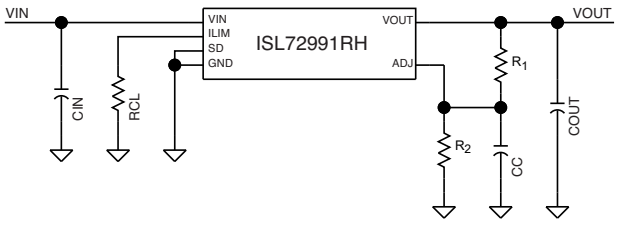


FIGURE 1. TYPICAL APPLICATION

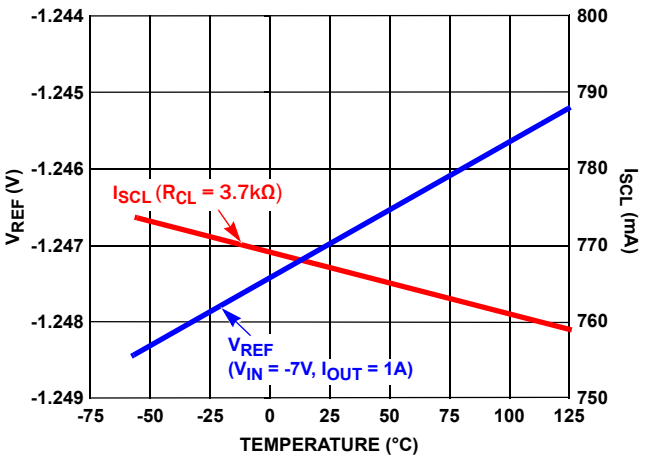


FIGURE 2. V_{REF} AND I_{SCL} vs TEMPERATURE

Ordering Information

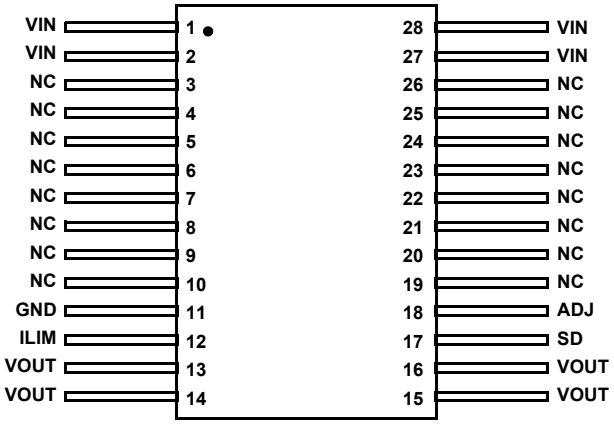
ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS COMPLIANT)	PKG. DWG. #	TEMP RANGE
5962F0250301VXC	ISL72991RHVF	HDR to 300krad(Si)	28 Ld Flatpack	K28.A	-55 to +125°C
5962F0250301QXC	ISL72991RHQF				
5962F0250301V9A	ISL72991RHVX (Note 3)		DIE	N/A	
N/A	ISL72991RHF/PROTO (Note 4)	N/A	28 Ld Flatpack	K28.A	
N/A	ISL72991RHX/SAMPLE (Notes 3, 4)	N/A	DIE	N/A	
N/A	ISL72991RHEVAL2Z (Note 5)	Evaluation Board			

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 5.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

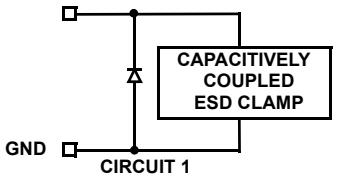
Pin Configuration

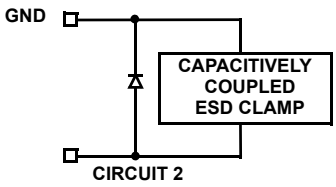
28 LD FLATPACK
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1, 2, 27, 28	VIN	Circuit 2	Regulator bias and input connection. All 4 pins must be tied together.
12	ILIM	Circuit 2	Current limiting set input.
13, 14, 15, 16	VOUT	Circuit 2	Regulator output connection. All 4 pins must be tied together.
17	SD	Circuit 1	Shut down input, active high.
18	ADJ	Circuit 2	Output voltage adjust input
11	GND	-	Ground connection
3, 4, 5, 6, 7, 8, 9, 10, 19, 20, 21, 22, 23, 24, 25, 26	NC	-	No Internal connections. Can be connected to ground or thermal plane.





Functional Block Diagram

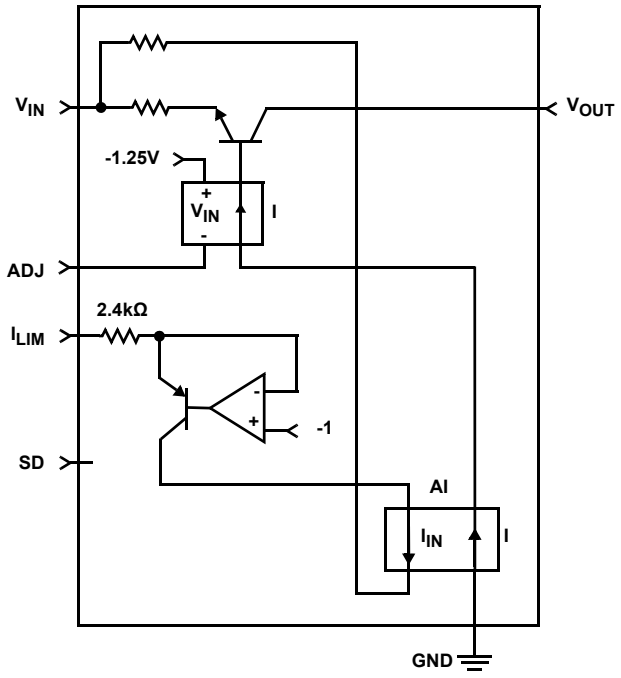


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Typical Application

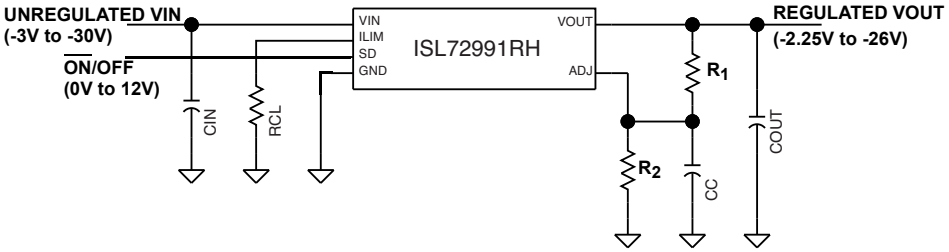


FIGURE 4. TYPICAL APPLICATION

Absolute Maximum Ratings

Minimum Supply Voltage ..... -35V
Minimum Supply Voltage (Note 8) ..... -30V
Minimum Output Current 3mA
Output Short-Circuit Duration. Thermal Protection ..... Indefinite
ESD Rating
Human Body Model (HBM) (Tested per MIL-PRF-883 3015.7)..... 3kV
Machine Model (MM) (Tested per EIA/JESD22-A115-A) 300V
Charged Device Model (CDM) (Tested per JESD22-C101D) 1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld Flatpack (Notes 6, 7)	60	5

Maximum Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) ..... +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range ..... -55°C to +125°C
Maximum Operating Junction Temperature ..... +150°C
Supply Voltage ..... -3V to -30V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.
7. For θ_{JC}, the "case temp" location is the center of the package underside.
8. The minimum supply limit specified is for operation in a heavy ion environment at an LET = 86.4MeV•cm^2/mg.

Electrical Specifications

$V_O \le V_{IN}$ -1.5V, I_O = 100mA, C_O = 47µF, SD = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

DESCRIPTION	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Reference Voltage (ADJ to GND)	V_{REF}	I_O = 3mA to 1A	-1.279	-1.250	-1.231	V
			-1.300		**-1.210**	V
Minimum Output Voltage	V_{Omin}	V_{IN} = -3V, I_O = 3mA to 100mA			**-2.25**	V
Maximum Output Voltage	V_{Omax}	V_{IN} = -30V, I_O = 3mA to 100mA	**-26**			V
Output Voltage Load Regulation	V_{LDR}	V_{IN} = -7V, V_O = -5V I_O = 3mA to 1A	-12		12	mV
			-15		**15**	mV
Output Voltage Line Regulation	V_{LNR}	$V_O \le V_{IN}$ -1V to V_{IN} = -30V, I_O = 100mA	**-25**		**25**	mV
0.1A Dropout Voltage	V_{DOL}	$dV_O \le$ 50mV, I_O = 0.1A			0.2	V
					0.3	V
1A Dropout Voltage (Pulse Tested)	V_{DOH}	$dV_O \le$ 50mV, I_O = 1A			**1**	V
Adjust Current	I_{ADJ}	$V_O \le V_{IN}$ -1V to V_{IN} = -30V, I_O = 500mA		1.7	**5.0**	µA
Dropout Quiescent Current	I_{QDO}	V_O - V_{IN} = 0.2V, I_O = 500mA			25	mA
		V_O - V_{IN} = 0.3V, I_O = 500mA			**25**	mA
SD Input Voltage	V_{SD}	V_O = ON			**0.8**	V
		V_O = OFF	**2.4**			V
SD Input Current	I_{SD}	V_{SD} = 0.8V			**50**	µA
		V_{SD} = 2.4V			100	µA
					150	µA
Output Short-Circuit Current Limit	I_{SCL}	V_{IN} = - 7V, V_O = 0V, R_{CL} = 3.7kΩ	**0.60**	0.75	**0.90**	A
GND Quiescent Current	I_{GND}	-3V≤ V_{IN} ≤ -30V, I_O < 1A		6		mA
Power Supply Rejection Ratio	PSRR	Frequency = 1MHz		-49		dB
Thermal Protection	OT_{PROT}			150		°C
Thermal Hysteresis	OT_{HYS}			20		°C

Post Radiation Electrical Specifications

$V_O \leq V_{IN}$ -1.5V, I_O = 100mA, C_O = 47µF, SD = 0V, T_A = +25°C, across a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
V_{REF}	Reference Voltage	I_O = 3mA to 1A	-1.279		-1.231	V
V_{Omin}	Minimum Output Voltage	V_{IN} = -3V, I_O = 3mA to 100mA			-2.25	V
V_{Omax}	Maximum Output Voltage	V_{IN} = -30V, I_O = 3mA to 100mA	-26			V
VLDR	Output Voltage Load Regulation	V_{IN} = -7V, V_O = -5V I_O = 3mA to 1A	-12		12	mV
VLNR	Output Voltage Line Regulation	$V_O \leq V_{IN}$ -1V to V_{IN} = -30V, I_O = 100mA	-25		25	mV
VDO_L	0.1A Dropout Voltage	$dV_O \leq$ 50mV, I_O = 0.1A			0.2	V
VDO_H	1A Dropout Voltage (Pulse Tested)	$dV_O \leq$ 50mV, I_O = 1A			1	V
I_{ADJ}	Adjust Current	$V_O \leq V_{IN}$ -1V to V_{IN} = -30V, I_O = 500mA			5	µA
I_{QDO}	Dropout Quiescent Current	V_O - V_{IN} = 0.3V, I_O = 500mA			25	mA
V_{SD}	SD Input Voltage	V_O = ON			0.8	V
		V_O = OFF	2.4			V
I_{SD}	SD Input Current	V_{SD} = 0.8V			50	µA
		V_{SD} = 2.4V			100	µA
I_{CL}	Output Short-Circuit Current Limit	V_{IN} = - 7V, V_O = 0V, R_{CL} = 3.7kΩ	0.6		0.9	A

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Total Dose Radiation Characteristics This data is typical mean test data post total dose radiation exposure at a high dose rate (HDR) of 50 to 300rad(Si)/s to 300krads. This data is intended to show typical parameter shifts due to total dose rate radiation. These are not limits nor are they guaranteed.

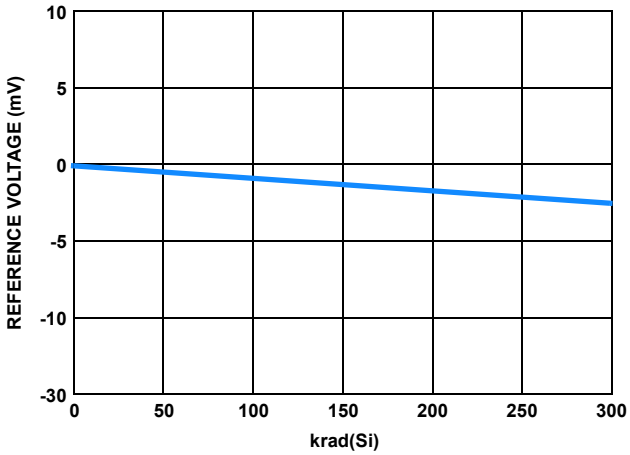


FIGURE 5. REFERENCE VOLTAGE CHANGE vs TOTAL DOSE RADIATION

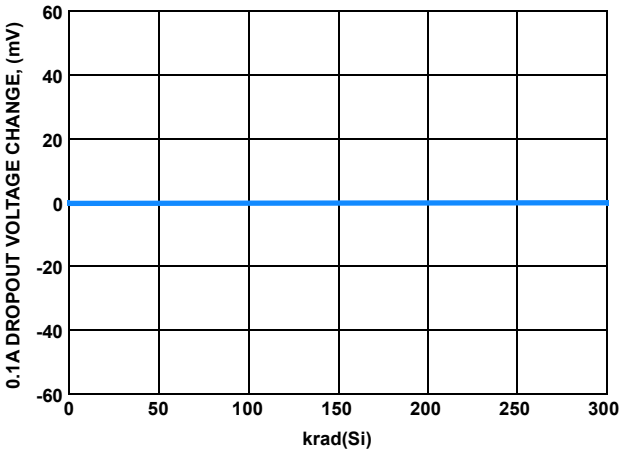


FIGURE 6. 0.1A DROPOUT VOLTAGE CHANGE vs TOTAL DOSE RADIATION

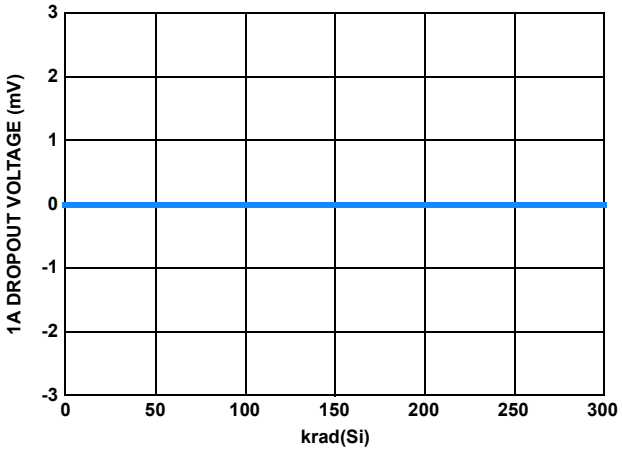


FIGURE 7. 1A DROPOUT VOLTAGE CHANGE vs TOTAL DOSE RADIATION

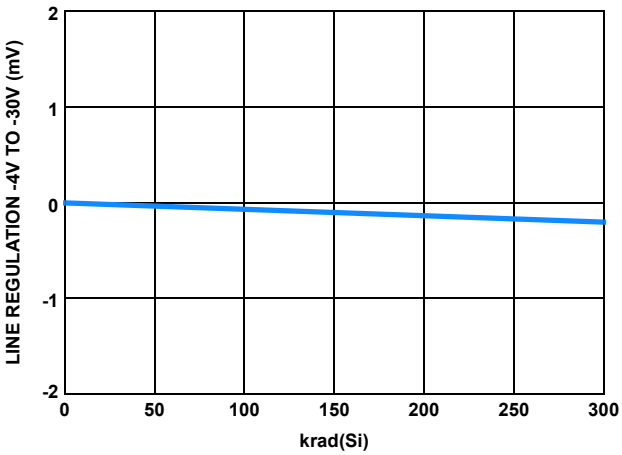


FIGURE 8. OUTPUT VOLTAGE LINE REGULATION CHANGE vs TOTAL DOSE RADIATION

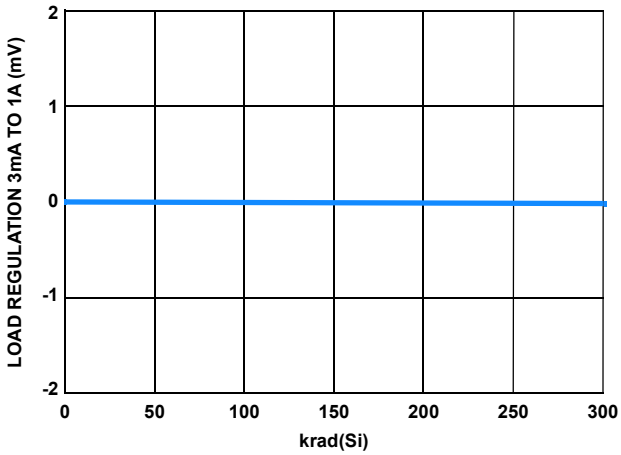


FIGURE 9. OUTPUT VOLTAGE LOAD REGULATION CHANGE vs TOTAL DOSE RADIATION

Typical Performance Curves

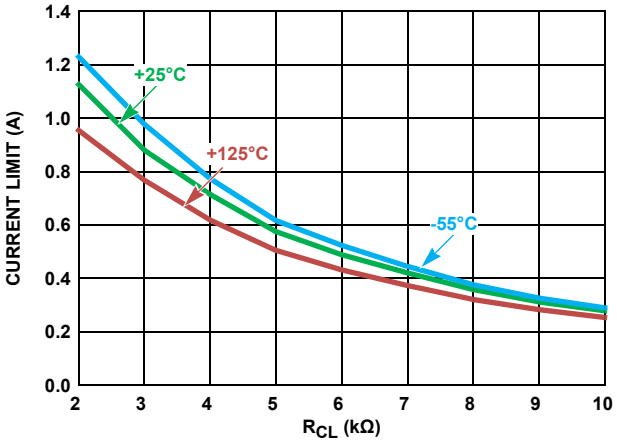


FIGURE 10. $-7V_{IN}$, $-5V_{OUT}$

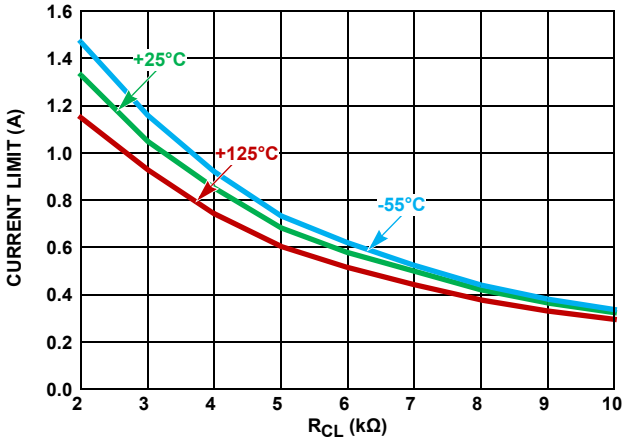


FIGURE 11. $-12V_{IN}$, $-5V_{OUT}$

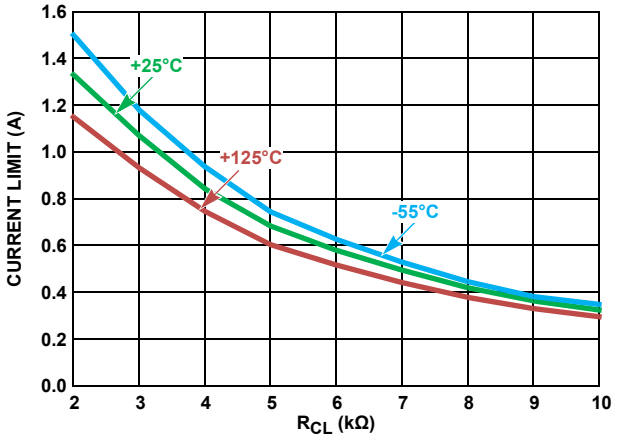


FIGURE 12. $-12V_{IN}$, $-10V_{OUT}$

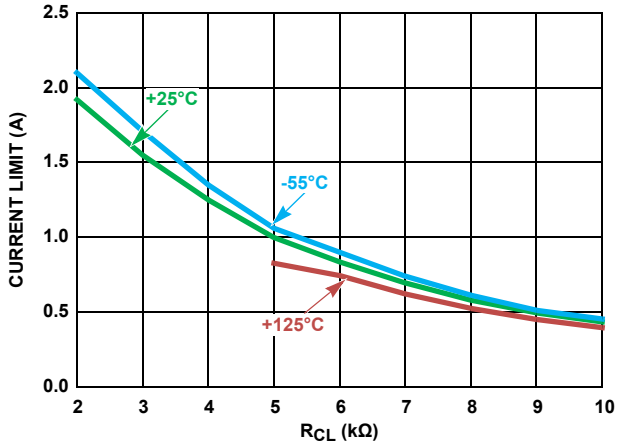


FIGURE 13. $-20V_{IN}$, $-10V_{OUT}$

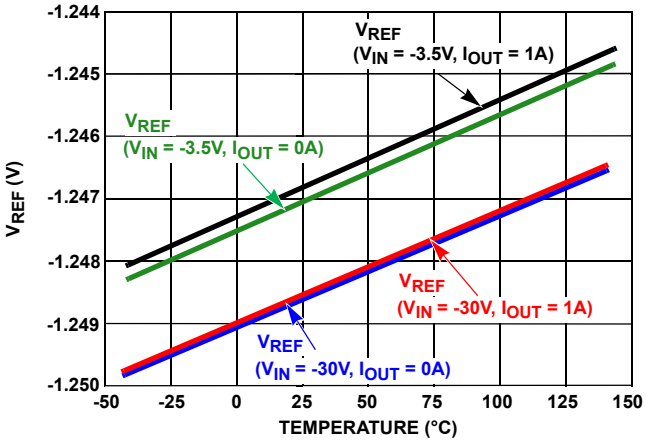


FIGURE 14. V_{REF} vs TEMPERATURE

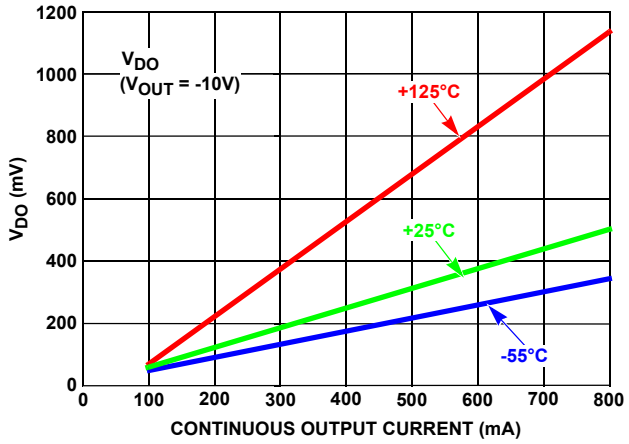


FIGURE 15. DROPOUT VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

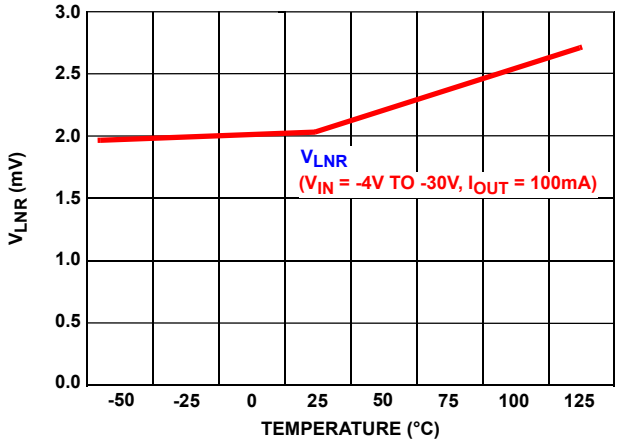


FIGURE 16. LINE REGULATION vs TEMPERATURE

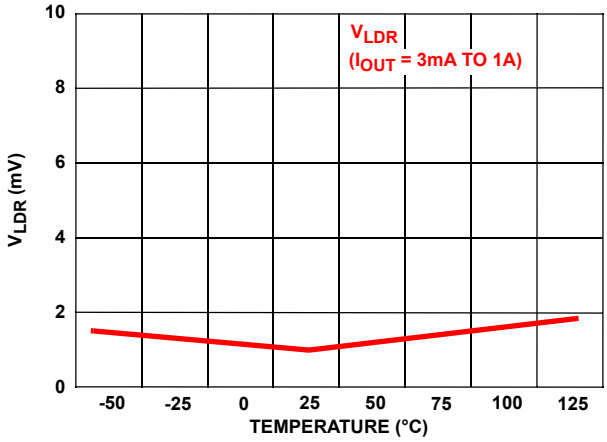


FIGURE 17. LOAD REGULATION vs TEMPERATURE

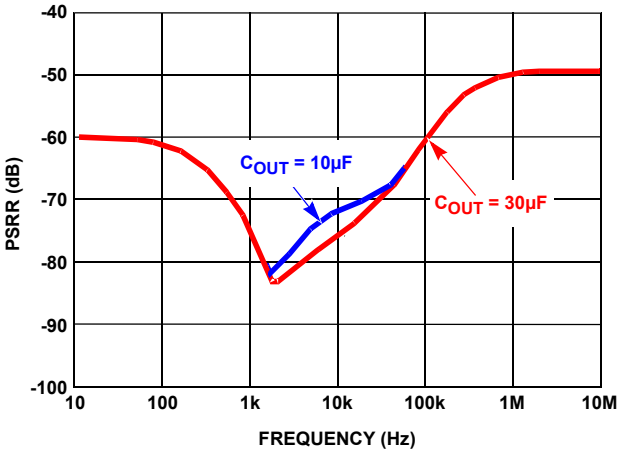


FIGURE 18. PSRR vs FREQUENCY (V_{IN} = -20V, V_{OUT} = -18V)

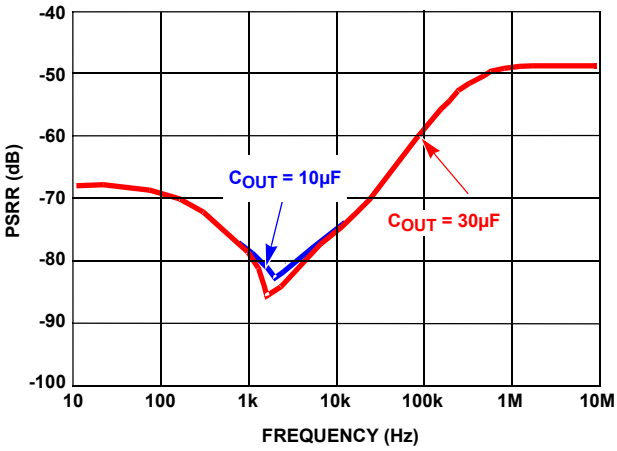


FIGURE 19. PSRR vs FREQUENCY (V_{IN} = -7V, V_{OUT} = -5V)

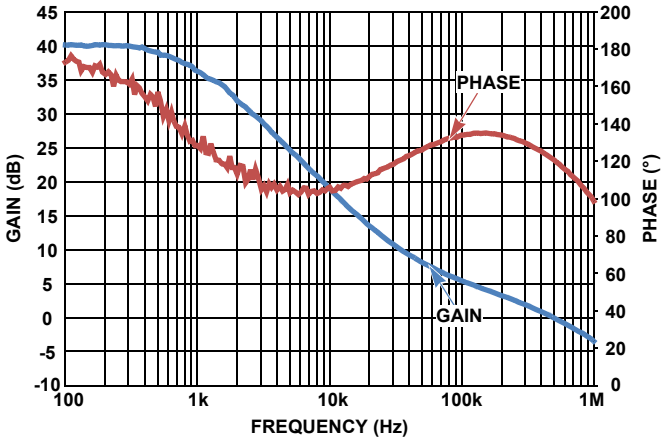


FIGURE 20. GAIN/PHASE -12V_{IN}, -5V_{OUT}, 0.5A I_{OUT}

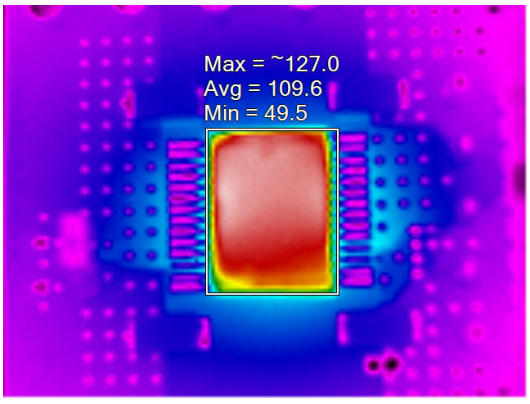


FIGURE 21. THERMAL (V_{IN} = -12V, V_{OUT} = -5V, I_{OUT} = 0.74A, T_A = +25°C)

Functional Description

Functional Overview

The radiation hardened ISL72991RH is a low dropout adjustable negative regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (ILIM), and a shutdown pin (SD) for easy on/off control. The part is constructed using the dielectrically isolated, complimentary bipolar RSG process. It is immune to single-event latch-up and has been specifically designed to provide reliable performance in harsh radiation environments.

Application Information

Output Voltage Programming

The output voltage of the regulator can be programmed with two external resistors and is described by Equation 1:

$$V_{OUT} = -1.25(1 + R_1/R_2) - (I_{ADJ} \times R_1) \quad \text{(EQ. 1)}$$

Output Current Limit Programming

The output current limit threshold of the regulator is set with a single external resistor (R_{CL}) connected from I_{LIM} to ground.

The effective current limit at any single R_{CL} value is influenced by the V_{IN} to V_{OUT} difference, temperature, and V_{IN} amplitude. Figures 22 through 24 illustrate these effects.

Figure 22 shows that for a given V_{OUT} (-5V) and temperature (+25°C) the effect of V_{IN} to V_{OUT} differential on the current limit level is significant.

Figure 23 shows the effect of temperature at a single V_{IN} to V_{OUT} voltage condition across the R_{CL} range of 2.1kΩ to 10kΩ.

Figure 24 shows that for a given differential voltage (V_{IN} to V_{OUT}) and temperature, the effect of V_{IN} amplitude is less significant than seen in Figure 22.

Because of these numerous variables, there is no one formula relating R_{CL} to I_{CL} that will suffice for the range of likely possible conditions. Figures 10 through 13 on page 8 provide guidance in setting the R_{CL} value for a limited number of possible conditions. Users are advised to evaluate their specific condition for satisfactory performance.

Capacitor Selection

An input capacitor is required if the regulator is located more than 6 inches from the power supply filter capacitors. A 10µF solid tantalum capacitor is recommended.

An output capacitor of at least 10µF must be used to ensure stability of the regulator. Additional capacitance may be added as required to improve the dynamic response of the regulator. Solid tantalum or ceramic capacitors are recommended.

Loop Compensation

The output capacitor and ESR comprise a zero in the loop transfer function that must be compensated with a pole to ensure loop stability in accordance with Equation 2:

$$C_C \times R_1 = C_{OUT} \times ESR \quad \text{(EQ. 2)}$$

The compensating capacitor should be a low ESR ceramic type.

Layout Guidelines

The stability of the regulator is sensitive to layout. It is strongly recommended that a continuous copper ground plane (1oz. or greater) be used. In addition, component lead lengths and interconnects should be minimized, but should not exceed 1/2 inch. Finally, the return lead of the compensation capacitor (C_C) should be connected as close as possible to the GND pin of the IC.

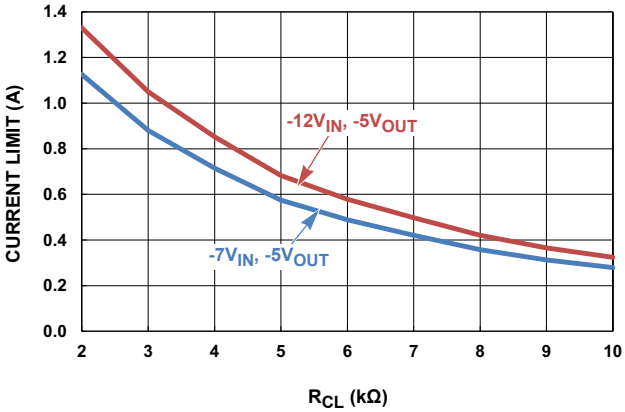


FIGURE 22. I_{CL} vs R_{CL} AND V_{IN} AMPLITUDE

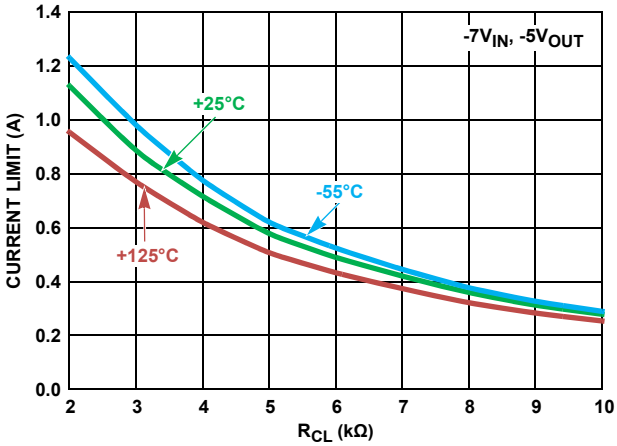


FIGURE 23. I_{CL} vs R_{CL} AND TEMPERATURE

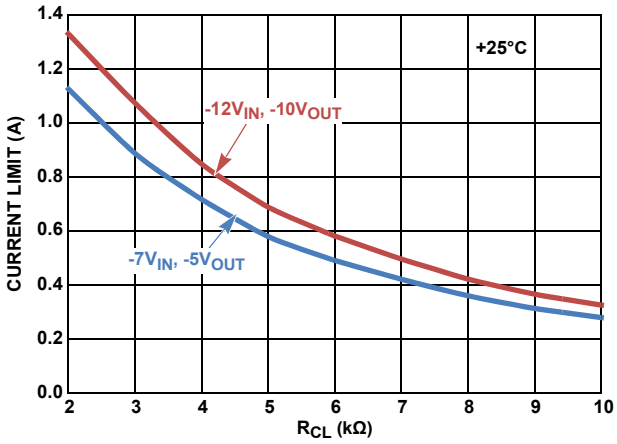


FIGURE 24. I_{CL} vs R_{CL} AND V_{IN} TO V_{OUT} DIFFERENTIAL

Package Characteristics

Weight of Packaged Device

2.2 Grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased
Case Isolation to Any Lead: 20 x 10^9 Ω (min)

Die Characteristics

Die Dimensions

5870µm x 5210µm (231.1 mils x 205.1 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ±1.0kÅ

TOP METALLIZATION

Type: AlSiCu (Si 0.75-1%/Cu 0.5%)
Thickness: 16.0kÅ ±2kÅ

BACKSIDE FINISH

Silicon

Assembly Related Information

SUBSTRATE AND LID POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

<2 x 10^5 A/cm^2

PROCESS

Dielectrically Isolated Radiation Hardened Silicon Gate

Metallization Mask Layout

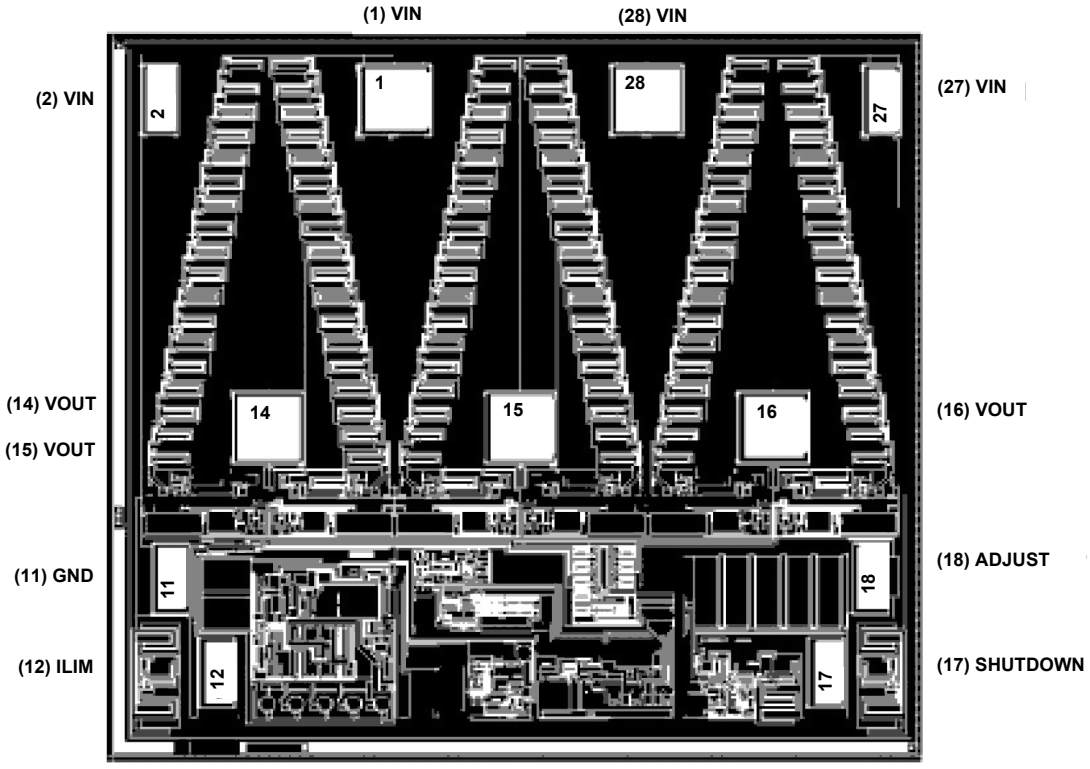


TABLE 1. DIE PAD COORDINATES

PAD NAME	X-COR CENTER	Y-COR CENTER	DX PAD SIZE	DY PAD SIZE
ILIM	-1300.5	-4348	258	516
(15)VOUT	920	-2554	516	516
SHUTDOWN	3140.5	-4348	258	516
ADJUST	3473.5	-3658	258	516
(16)VOUT	2917	-2554	516	516
(27)VIN	3580	0	258	516
(28)VIN	1840	0	516	516
(1)VIN	0	0	516	516
(2)VIN	-1740	0	258	516
(14)VOUT	-1077	-2554	516	516
GND	-1662	-3657	258	516

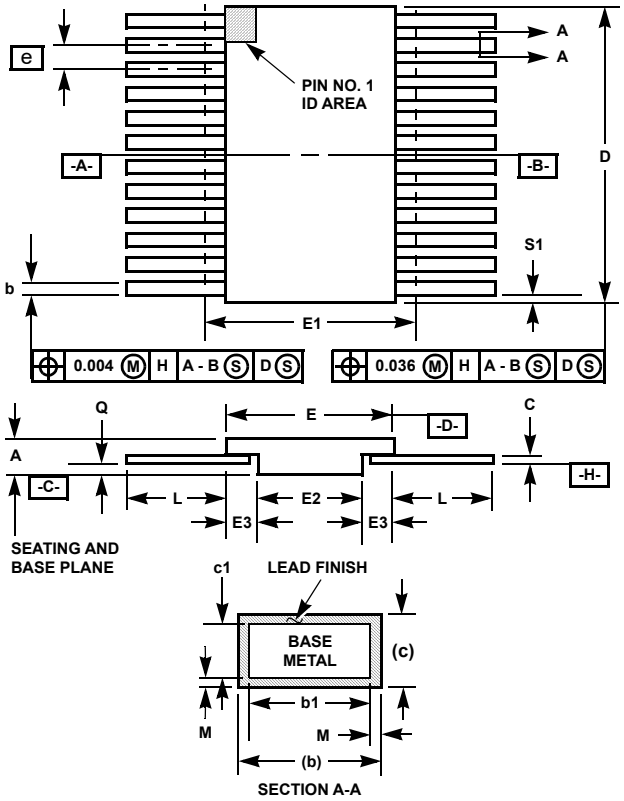
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Revision.

DATE	REVISION	CHANGE
Jun 16, 2022	7.01	Updated features bullet. Removed related literature section. Updated Figures 4 and 22.
Oct 2, 2020	7.00	Updated links throughout. Applied new formatting standard to Radiation Acceptance Testing and SEE Hardness Features bullets. Updated Ordering information table by adding Rad Hard data, adding Note 3, and updating Note 4. In Table 1 on page 12 Updated pad name (27) to VIN and corrected Y-COR CENTER coordinates for the following pad names: - (15)VOUT, (27) VIN, and (2)VIN Removed About Intersil section
Apr 14, 2017	6.00	Added Notes 4 and 5 on page 2. Added Table 1 on page 12.
Aug 17, 2016	5.00	Updated Equation 2 Loop Compensation equation to change R2 to R_1.
May 7, 2015	4.00	Replaced Figures 10, 11, 12 and 13 on page 8. Replaced Figures 22, 23 and 24 on page 10. Updated Equation 1 on page 10: from VOUT = -1.25(1+R2/R1) - (IADJ x R2) to VOUT = -1.25(1+R1/R2) - (IADJ x R1).
Jan 29, 2015	3.00	“Typical Performance Curves” on page 8: Added Figures 18 and 19.
Mar 26, 2014	2.00	Added Related Literature on page 1. Added significant relevant content throughout the document, expanding from 3 to 12 pages.
Jun, 28, 2004	1.00	Updated file.
Jul 9, 2001	4.00	Initial Release.

Package Outline Drawing

For the most recent package outline drawing, see K28.A.



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 lead ceramic metal seal flatpack package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/