ISL71610SLHM

Radiation Hardened Passive-Input Digital Isolator

The ISL71610SLHM is a passive-input digital signal isolator with a CMOS output. It has a similar interface but with better performance and higher package density than optocouplers.

The ISL71610SLHM is manufactured with Giant Magnetoresistive (GMR) technology for small size, high speed, and low power. A ceramic/polymer composite barrier provides excellent isolation and an unlimited barrier life. A series external resistor sets the input coil current and a capacitor in parallel with the current-limiting resistor provides improved dynamic performance. This versatile component can replace a variety of optocouplers, functioning over a wide range of data rates, edge speeds, and power supply levels. The device output is compatible with 3.3V and 5V supplies, allowing an interface to controllers without additional level shifting. With the coil energized with a minimum of ±8mA (bidirectional current), the ISL71610SLHM is suitable for single-ended and differential drive applications.

The ISL71610SLHM is offered in an 8 Ld 5mmx4mm SOIC package and is fully specified across the military ambient temperature range of -55°C to +125°C.

Applications

- Isolated power
- CAN bus/device net
- Differential line receiver
- Optocoupler replacement
- SPI interface
- RS-485, RS-422, or RS-232

Features

- Barrier Voltage Endurance
  - 2.5kV$_{RMS}$, for 1 minute, 600V$_{RMS}$ continuous (VDE V 0884-10 certified: file 5022321-4880-0001)
  - 1.5kV$_{DC}$ continuous
  - 500V$_{DC}$ at 60MeV•cm^2/mg SEDR
- Production testing and qualification follow the AS6294/1 standard (see Radiation Hardened Plastic Production and QCI Flow)
- UL 1577 recognized: file reference E483309
- Up to 100Mbps data rate
- Flexible inputs with very wide input voltage range (resistor limited current through coil)
- No carrier or clock for low EMI emissions and susceptibility
- 3V to 5.5V signaling operation
- Passes NASA low outgassing specifications
- NiPdAu-Ag leadframes (Pb-free, Sn-free)
- Full military temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- Radiation characterization
  - Low Lose Rate (LDR) (0.01rad(Si)/s): 75krad(Si)
- SEE Characterization
  - No SEB/SEL,V_{DD} = 6.5V: LET = 86MeV•cm^2/mg

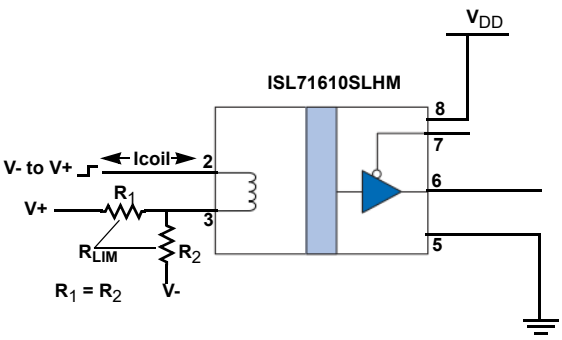


Figure 1. Single-Ended Configuration

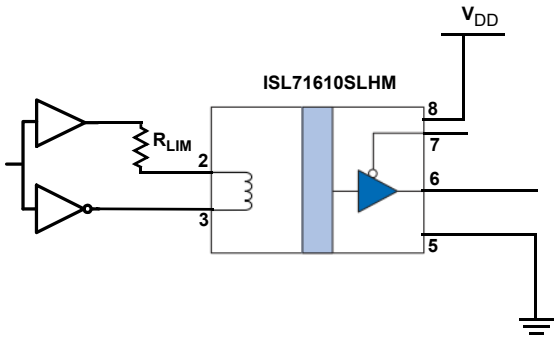
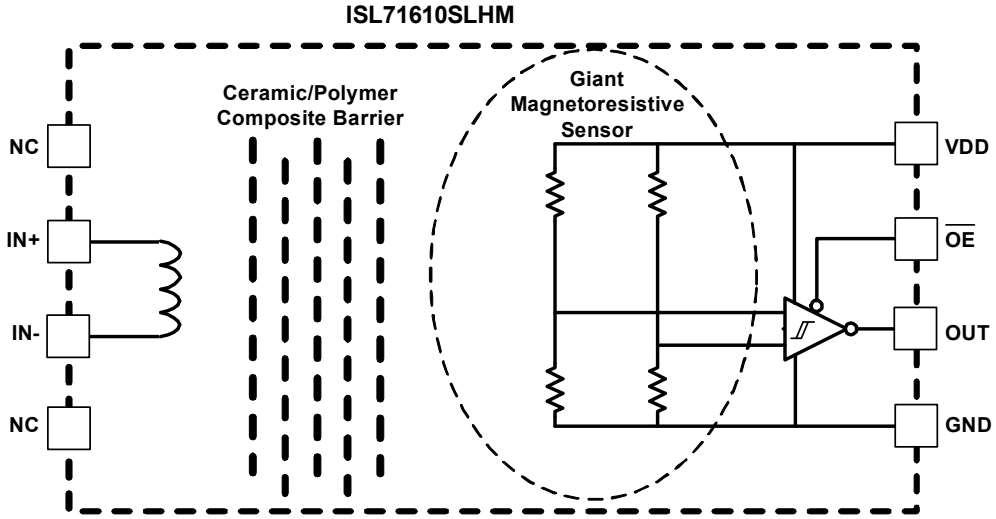


Figure 2. Differential Configuration

Contents

1. Overview

1.1 Functional Block Diagram

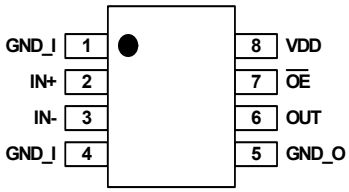


Ground the NC pins to prevent ion charge buildup on floating metal

Figure 3. Block Diagram

2. Pin Information

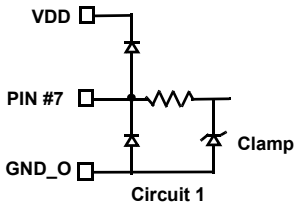
2.1 Pin Assignments



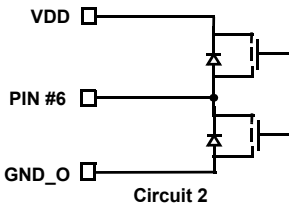
Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 4	GND_I	N/A	No internal connection. Use for input shielding, connect to input side ground
2	IN+	N/A	Coil connection. The voltage applied to IN+ is more negative than IN- to cause the voltage of OUT to switch to V_{OL} (logic low).
3	IN-	N/A	Coil connection. The voltage applied to IN- is more positive than IN+ to cause the voltage of OUT to switch to V_{OL} (logic low).
5	GND_O	N/A	Ground return for VDD
6	OUT	2	Data output. The OUT pin logic high is the zero input current state.
7	$\overline{OE}$	1	Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected.
8	VDD	N/A	Receiver supply voltage



Circuit 1



Circuit 2

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VDD	GND - 0.3	GND + 7	V
IN+, IN-	-25	25	mA
OUT, $\overline{OE}$	GND - 0.3	V_{DD} + 1.5	V
OUT, $\overline{OE}$	-10	10	mA
Voltage Difference Across the Package (Pins 1, 2, 3, 4 to Pins 5, 6, 7, 8)		500	V
Power Dissipation		675	mW
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per AEC-Q100-002)	1.2		kV
Charged Device Model (Tested per AEC-Q100-011)	1.5		kV
Latch-up (Tested per JESD-78E; Class 2, Level A) at +125°C	100		mA

3.2 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material [1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material of <0.1%.

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W) (Top)	θ_{JC} (°C/W) (Bottom)	Ψ_{JT} (°C/W)[2]
NSOIC Package M8.15G	60	73	40	10

1. θ_{JA} is measured with the component soldered to double-sided board; free air.
2. For Ψ_{JT} characterization parameter, the package top temperature is measured at the top center of the mounted package. See TB379.

Parameter	Minimum	Maximum	Unit
Junction Temperature	-55	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-55	+125	°C
VDD	3	5.5	V
OUT, $\overline{OE}$	0	V_{DD}	V
OUT	-4	4	mA
Maximum Coil Current	-20	20	mA
Minimum Coil Current to Ensure Correct Output	-8	8	mA

3.5 Insulation Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Creepage Distance (external)		IPC-2221B	2.54			mm
Total Barrier Thickness (internal)			12	13		µm
Leakage Current		$240V_{RMS}$, 60Hz		200		nA
Barrier Resistance	R_{IO}	$500V_{DC}$		>100		TΩ
Barrier Capacitance	C_{IO}	1MHz		7		pF
Comparative Tracking Index	CTI	Per IEC:60112	>175			V
AC High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	V_{IO}AC	+125°C ambient	600			V_{RMS}
DC High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	V_{IO}DC	+125°C ambient	1500			V
Barrier Life		100°C, 1000 V_{RMS}, 60% Confidence Level activation energy		44000		Years

3.6 Safety and Approvals

3.6.1 VDE V 0884-10 (VDE V 0884-11 pending) (Basic Isolation; VDE File Number 5022321-4880-0001)

- Working voltage (V_{IORM}): $600V_{RMS}$ ($848V_{PK}$); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}): $2500V_{RMS}$
- Transient overvoltage (V_{IOTM}): $4000V_{PK}$
- Surge rating: 4000V
- Each part tested at $1590V_{PK}$ for 1s, 5pC partial discharge limit
- Samples tested at $4000V_{PK}$ for 60s; then $1358V_{PK}$ for 10s with 5pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Unit
Safety Rating Ambient Temperature	T_S	+180	°C
Safety Rating Power	P_S	270	mW
Supply Current Safety Rating (Total of Supplies)	I_S	54	mA

3.6.2 UL 1577 (Component Recognition Program File Number E483309)

- Each part tested at $3000V_{RMS}$ ($4240V_{PK}$) for 1s; each lot sample tested at $2500V_{RMS}$ ($3530V_{PK}$) for 1min

3.7 Electrical Specifications

Unless otherwise noted, V_{DD} = 3V - 5.5V; OUT and $\overline{OE}$ are open, VDD is bypassed to GND with a 47nF X7R capacitor; $T_A = T_J$ = +25°C. Limits apply across the operating temperature range, -55°C to +125°C, unless otherwise stated.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Input Specifications						
Coil Input Resistance	R_{COIL}	T = 25°C	47	85	112	Ω
Coil Input Resistance	R_{COIL}	T = -55°C	31	60		Ω
Coil Input Resistance	R_{COIL}	T = 125°C		115	138	Ω
Coil Resistance Temperature Coefficient [2]	TC R_{COIL}			0.2	0.25	Ω/K
Coil Inductance	L_{COIL}			9		nH
DC High Input Threshold (5V)	I_{INH-DC}	Single-ended circuit, V_{DD} = 4.5V - 5.5V	0.5	1		mA
DC Low Input Threshold (5V)	I_{INL-DC}	Single-ended circuit, V_{DD} = 4.5V - 5.5V		3.5	8	mA
Differential High Input Threshold	$I_{INH-DIFF}$	Differential circuit, V_{DD} = 3V - 5.5V, C_{BOOST} = 0pF, symmetric reversing input	0.5	1		mA
Differential Low Input Threshold	$I_{INL-DIFF}$	Differential circuit, V_{DD} = 3V - 5.5V, C_{BOOST} = 0pF, symmetric reversing input		3.5	8	mA
Failsafe High Input Current (5V)	$I_{FS-HIGH}$	Single-ended circuit, V_{DD} = 4.5V - 5.5V	-25		0.5	mA
Failsafe Low Input Current (5V)	I_{FS-LOW}	Single-ended circuit, V_{DD} = 4.5V - 5.5V	5		25	mA
Input Signal Rise and Fall Times[2]	t_{IR}, t_{IF}				1	µs
Common-Mode Transient Immunity[2]	$\|CM_H\|$,$\|CM_L\|$	$V_{TRANSIENT}$ = $300V_{PEAK}$	15	20		kV/µs
5V Electrical Specifications (V_{DD} = 4.5V - 5.5V; T = -55°C to +125°C unless otherwise stated)						
5V Quiescent Supply Current	I_{DDQ}	IN+ = IN- = open		2	3	mA
Logic High Output Voltage	V_{OH}	V_{DD} = 5 V, OUT = 20µA	4.9	5		V
		V_{DD} = 5 V, OUT = 4mA	4.6	4.8		V
Logic High Output Drive Current	I_{OH}			-10	-7	mA
Logic Low Output Voltage	V_{OL}	V_{DD} = 5 V, OUT = -20µA		0	0.1	V
		V_{DD} = 5 V, OUT = -4mA		0.2	0.8	V
Logic Low Output Drive Current	I_{OL}		7	10		mA
Output Disable	V_{OE}			2.7		V
5 V Switching Specifications (V_{DD} = 4.5 V - 5.5 V; T = -55°C to +125°C unless otherwise stated)						
Data Rate		Single-ended circuit, t_{IR} = t_{IF} = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF			100	Mbps
Minimum Pulse-Width[2]	PW	Single-ended circuit, t_{IR} = t_{IF} = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF	10			ns
Propagation Delay Input to Output (High-to-Low)	t_{PHL}	Single-ended circuit, t_{IR} = t_{IF} = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		8	15	ns
Propagation Delay Input to Output (Low-to-High)	t_{PLH}	Single-ended circuit, t_{IR} = t_{IF} = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		8	15	ns

Unless otherwise noted, V_{DD} = 3V - 5.5V; OUT and $\overline{OE}$ are open, VDD is bypassed to GND with a 47nF X7R capacitor; $T_A = T_J$ = +25°C. Limits apply across the operating temperature range, -55°C to +125°C, unless otherwise stated. **(Continued)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Average Propagation Delay Drift	t_{PDD}	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		10		ps/°C
Pulse Width Distortion $\lvert t_{PHL}-t_{PLH}\rvert$	PWD	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		3	6	ns
Pulse Jitter	t_J	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		100		ps
Propagation Delay Skew [2]	t_{PSK}	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF	-2		2	ns
Propagation Delay Enable to Output (High-to-High Impedance)	t_{PHZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance)	t_{PLZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High)	t_{PZH}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low)	t_{PZL}	C_L = 15pF	-	3	7	ns
Output Rise Time (10% to 90%)[2]	t_R	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		2	4	ns
Output Fall Time (10% to 90%)[2]	t_F	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		2	4	ns
3.3V Electrical Specifications (V_{DD} = 3V - 3.6V; T = -55°C- 125°C unless otherwise stated)						
3.3V Quiescent Supply Current	I_{DDQ}	IN+ = IN- = open		1.3	2	mA
Logic High Output Voltage	V_{OH}	V_{DD} = 3.3V, OUT = 20µA	3.2	3.3		V
		V_{DD} = 3.3V, OUT = 4mA, 25°C, -55°C	3.0	3.1		V
		V_{DD} = 3.3V, OUT = 4mA, +125°C	2.85	3.0		V
Logic High Output Drive Current	I_{OH}			-10	-7	mA
Logic Low Output Voltage	V_{OL}	V_{DD} = 3.3V, OUT = -20µA		0	0.1	V
Logic Low Output Voltage	V_{OL}	V_{DD} = 3.3V, OUT = -4mA		0.2	0.8	V
Logic Low Output Drive Current	I_{OL}		7	10		mA
Output Disable	V_{OE}			1.6		V
3.3V Switching Specifications (V_{DD} = 3V - 3.6V; T = -55°C - 125°C unless otherwise stated)						
Data Rate		Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF			100	Mbps
Minimum Pulse Width [2]	PW	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF	10			ns
Propagation Delay Input to Output (High-to-Low)	t_{PHL}	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		12	18	ns
Propagation Delay Input to Output (Low-to-High)	t_{PLH}	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		12	18	ns
Average Propagation Delay Drift	t_{PDD}	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		10		ps/°C

Unless otherwise noted, V_{DD} = 3V - 5.5V; OUT and $\overline{OE}$ are open, VDD is bypassed to GND with a 47nF X7R capacitor; $T_A = T_J$ = +25°C. Limits apply across the operating temperature range, -55°C to +125°C, unless otherwise stated. **(Continued)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Pulse Width Distortion |tPHL-tPLH|	PWD	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		3	6	ns
Propagation Delay Skew[2]	t_{PSK}	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF	-2		2	ns
Propagation Delay Enable to Output (High-to-High Impedance)	t_{PHZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance)	t_{PLZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High)	t_{PZH}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low)	t_{PZL}	C_L = 15pF	-	3	7	ns
Output Rise Time (10% to 90%) [2]	t_R	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		3	5	ns
Output Fall Time (10% to 90%) [2]	t_F	Single-ended circuit, $t_{IR} = t_{IF}$ = 3ns, C_{BOOST} = 16pF, R_{OUT} = 1kΩ, C_{OUT} = 16pF		3	5	ns

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Parameter not tested in production.

4. Typical Performance Graphs

V_{DD} = 5V, T_A = +25°C, unless otherwise specified.

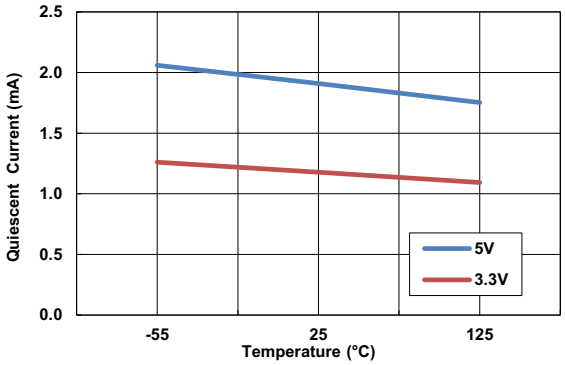


Figure 4. Quiescent Current vs Temperature, Voltage

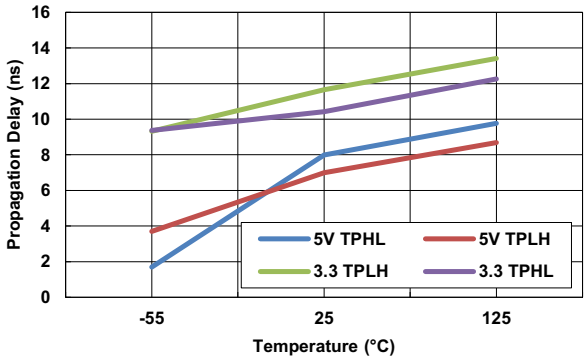


Figure 5. Propagation Delay vs Temperature, Voltage

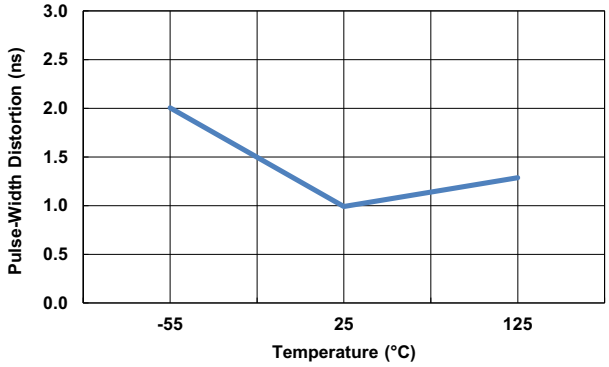


Figure 6. Pulse-Width Distortion vs Temperature

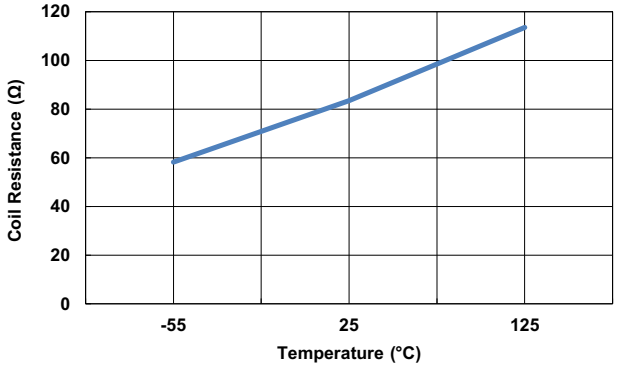


Figure 7. Coil Resistance vs Temperature

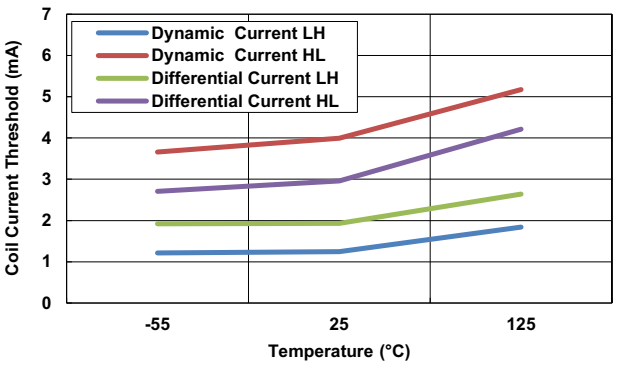


Figure 8. Coil Current Threshold vs Temperature, Voltage

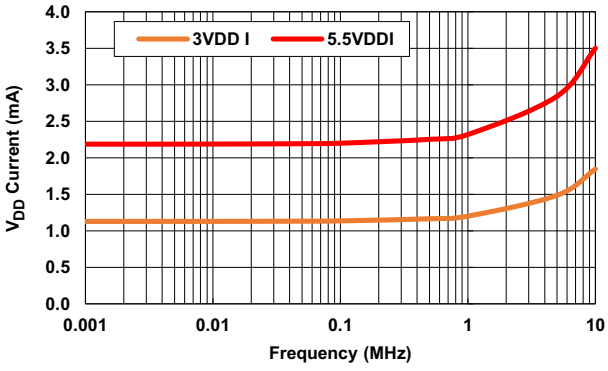


Figure 9. V_{DD} Current vs Frequency, Voltage, 0 Load, 50% Duty Cycle

V_{DD} = 5V, T_A = +25°C, unless otherwise specified. **(Continued)**

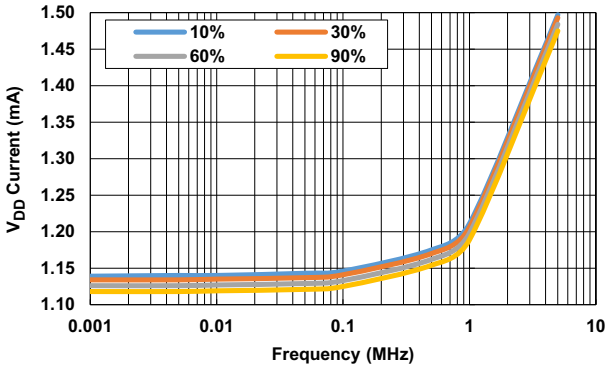


Figure 10. 3V V_{DD} Current vs Frequency, Duty Cycle, 0 load

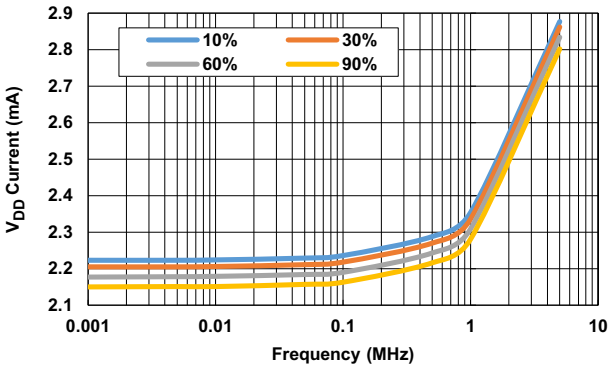


Figure 11. 5.5V V_{DD} Current vs Frequency, Duty Cycle, 0 load

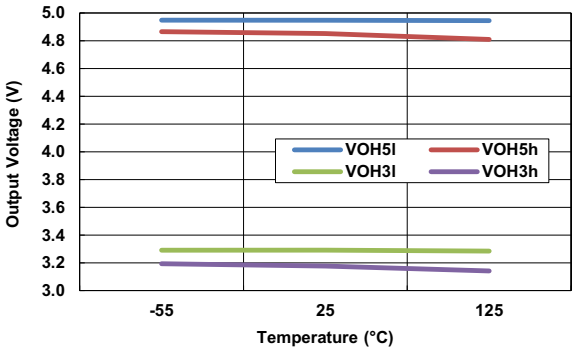


Figure 12. Output High Voltage for 5V and 3.3V with I_{OUT} of 20µA and 4mA

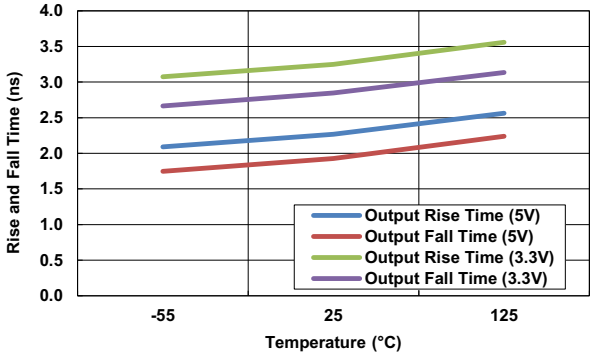


Figure 13. Rise and Fall Time vs Voltage and Temperature

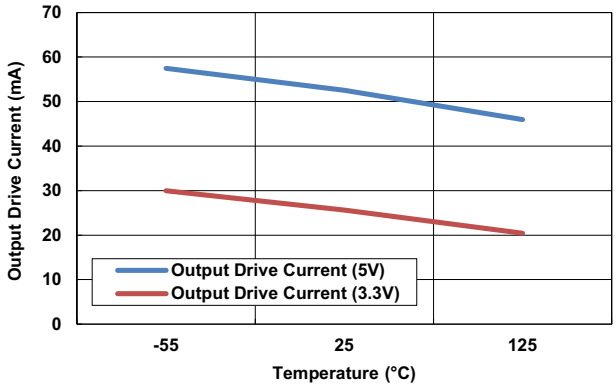


Figure 14. Output Drive Current Capability vs Temperature and Voltage

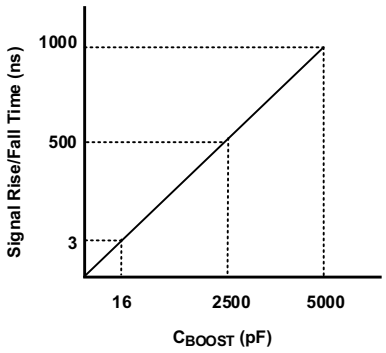


Figure 15. Boost Capacitor (C_{BOOST}) Selector Guide

V_{DD} = 5V, T_A = +25°C, unless otherwise specified. VRlimit trace shows the timing of the coil current through the current limiting resistor and coil as a voltage across the resistor and coil, coil current rise/fall time ~20ns, V_{OUT} rise/fall time ~10ns.

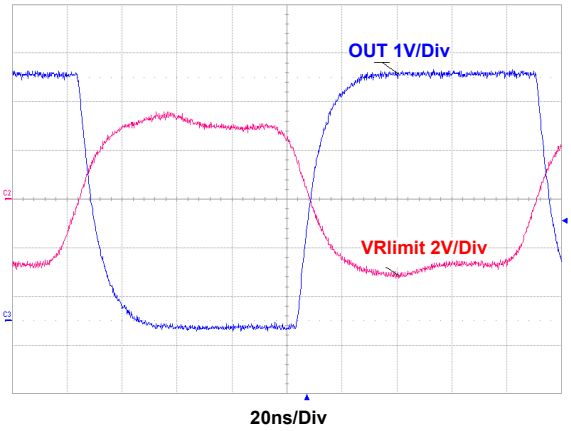


Figure 16. Switching, Coil Current ~±8mA, C_{BOOST} = 15pF, C_{OUT} = 15pF, V_{DD} = 5V

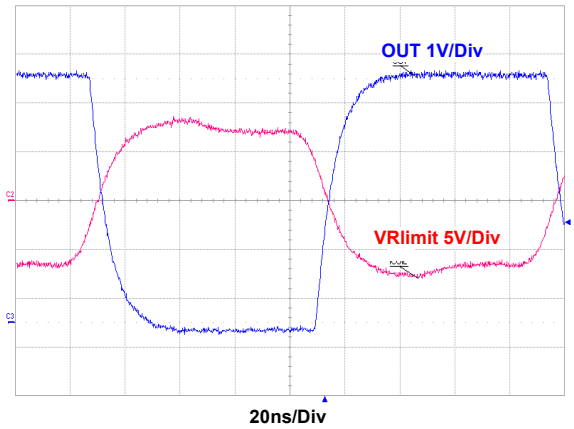


Figure 17. Switching, Coil Current ~±18mA, C_{BOOST} = 15pF, C_{OUT} = 15pF, V_{DD} = 5V

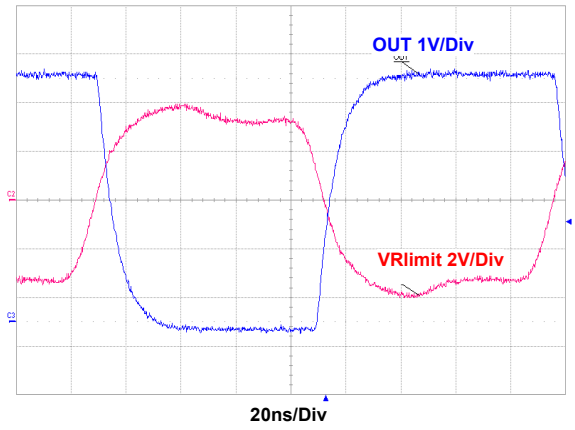


Figure 18. Switching, Coil Current ~±8mA, C_{BOOST} = 5pF, C_{OUT} = 15pF, V_{DD} = 5V

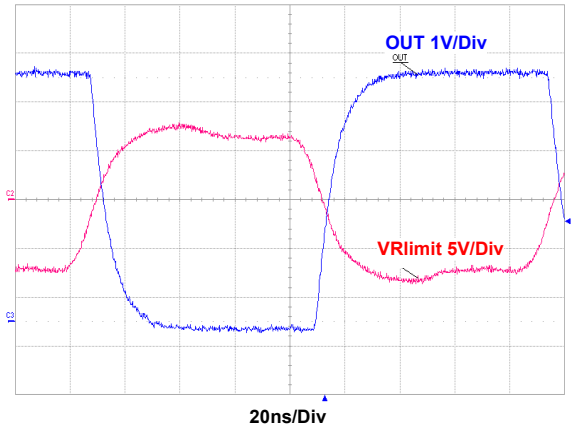


Figure 19. Switching, Coil Current ~±18mA, C_{BOOST} = 5pF, C_{OUT} = 15pF, V_{DD} = 5V

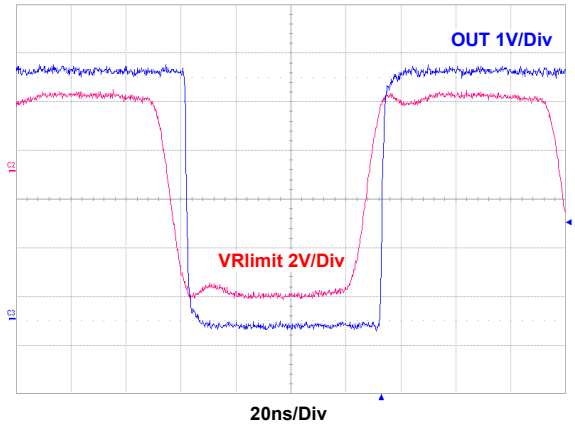


Figure 20. Non Inverting Configuration, Switching Coil Current ~±10mA, C_{BOOST} = 5pF, C_{OUT} = 15pF, V_{DD} = 5V

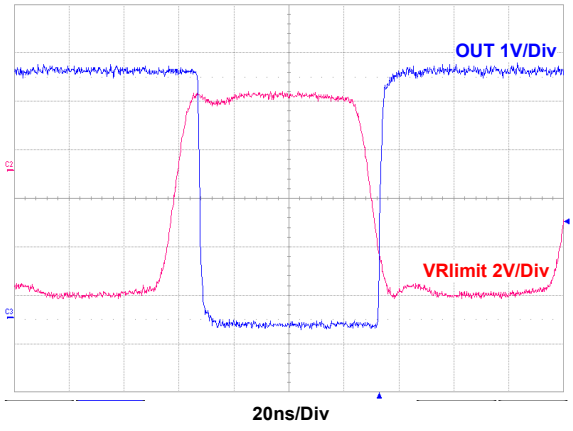


Figure 21. Inverting Configuration, Switching, Coil Current ~±10mA, C_{BOOST} = 5pF, C_{OUT} = 15pF, V_{DD} = 5V

5. Device Information

The ISL71610SLHM isolator is a passive input current mode device. Changes in current flow into the input coil result in logic state changes at the output.

5.1 Coil Polarity

The ISL71610SLHM switches to logic low if current flows from the IN- pin to the IN+ pin. **Note:** The designations IN- and IN+ refer to logic levels, not current flow. Positive current values mean conventional current flows into the IN- input. To ensure an output state in an ion environment, the coil must be energized in either direction and must not be in a zero-current condition. Figure 16 through Figure 21 illustrate the bidirectional current drive waveforms.

5.2 Input Resistor Selection

A series resistor sets the coil input current. There is no limit to the input voltage amplitude because there are no semiconductor input structures. The minimum current amplitude for an assured output state across the voltage range is ±8mA. A boost capacitor creates current reversals at edge transitions, reducing the input logic low threshold current to the differential level of 5mA. For a 25°C 8mA coil current, a typical resistor value for 3.3V signaling is 324Ω, and a typical value for 5V signaling is 511Ω based on an 85Ω coil resistance. These values are approximate and should be adjusted for temperature or other application specifics. Consult the coil resistance specification and temperature coefficient graph for further information and guidance. If the expected temperature range is large, 1% tolerance resistors may provide additional design margin.

5.3 Single-Ended or Differential Input

You can run the ISL71610SLHM with single-ended or differential inputs. In differential mode, the current naturally flows through the coil in both directions without a boost capacitor although the capacitor can still be used for increased external field immunity or improved pulse-width distortion. Because of SEE testing results, the single-ended mode of operation should be implemented with ±8mA minimum of coil current as shown in Figure 1.

An advantage over optocouplers and other high-speed couplers in differential mode is that no reverse bias protection for the input structure is required for a differential signal.

One of the more common applications is for an isolated differential line receiver. For example, RS-485 can drive an ISL71610SLHM directly for a fraction of the cost of an isolated RS-485 node.

5.4 Non-Inverting and Inverting Configurations

ISL71610SLHM can be configured in non-inverting and inverting configurations, each is defined by the direction of current flow through the coil. In the non-inverting configuration current flows through the coil from the IN- side to the IN+ side. The +IN is at a higher voltage potential than the -IN.

5.5 Boost Capacitor

The boost capacitor in parallel with the current-limiting resistor boosts the instantaneous coil current at the signal transition. This ensures switching and reduces propagation delay and reduces pulse-width distortion.

Select the value of the boost capacitor based on the rise and fall times of the signal driving the inputs. The instantaneous boost capacitor current is proportional to input edge speeds (C * dV/dt). Select a capacitor value based on the rise and fall times of the input signal to be isolated that provides approximately 20mA of additional boost current. For high-speed logic signals (t_R,t_F < 10ns), a 16pF capacitor is recommended. The capacitor value is generally not critical; if in doubt, choose a higher value. See Figure 16.

5.6 Dynamic Power Consumption

Power consumption is proportional to duty cycle, not data rate. The use of NRZ coding minimizes power dissipation because no additional power is consumed when the output is in the high state. In differential mode, where the logic high condition may still require a current to be forced through the coil, power consumption is

higher than a typical NRZ single-ended configuration. See Figure 14 through Figure 16 for typical power consumption performance.

5.7 Power Supply Decoupling

A 47nF low-ESR ceramic capacitor is recommended to decouple the power supply. Place the capacitor as close as possible to the VDD pin.

5.8 Maintaining Creepage

Creepage distances are often critical in isolated circuits. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, if ground planes are used, space them to avoid compromising clearance.

5.9 Electromagnetic Compatibility and Magnetic Field Immunity

Because the ISL71610SLHM is completely static, it has the lowest emitted noise of any non-optical isolators. The ISL71610SLHM operates by imposing a magnetic field on a GMR sensor, which translates the change in field into a change in logic state. A magnetic shield and a Wheatstone Bridge configuration provide good immunity to external magnetic fields. Immunity to external magnetic fields can be enhanced by proper orientation of the device with respect to the field direction, the use of differential signaling, and boost capacitors.

5.9.1 Orientation of the Device with Respect to the Field Direction

An applied field into the pin edges of the package is the worst case for magnetic immunity. In this case, the external field is in the same direction as the applied internal field. In one direction it tends to help switching; in the other it hinders switching. This can cause unpredictable operation.

An applied field into the pin-less edges of the package has considerably less effect and results in higher magnetic immunity.

5.9.2 Differential Signaling and Boost Capacitors

Regardless of orientation, driving the coil differentially improves magnetic immunity because the logic high state is driven by an applied field instead of zero field, as is the case with single-ended operation. The higher the coil current, the higher the internal field and the higher the immunity to external fields. Optimal magnetic immunity is achieved by adding the boost capacitor.

5.10 Data Rate and Magnetic Field Immunity

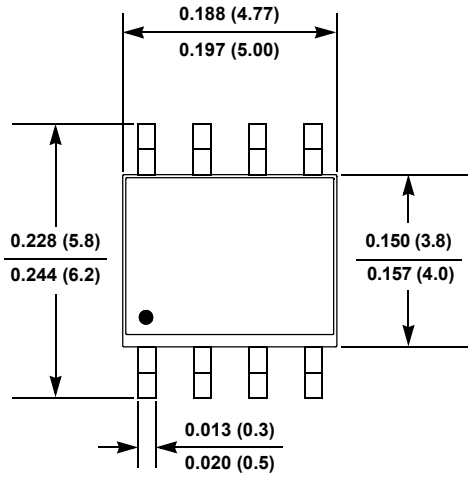
It is easier to disrupt an isolated DC signal with an external magnetic field than it is to disrupt an isolated AC signal. Similarly, a DC magnetic field has a greater effect on the device than an AC magnetic field of the same effective magnitude. For example, signals with pulses longer than 100µs are more susceptible to magnetic fields than shorter pulse widths.

6. Package Outline Drawing

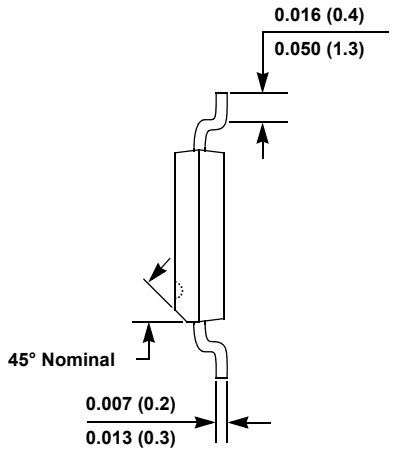
For the most recent package outline drawing, see M8.15G.

M8.15G

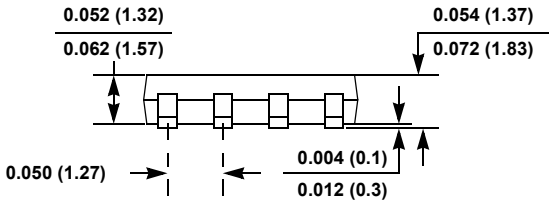
8 Lead Narrow Body Small Outline Plastic Package
Rev 2, 10/18



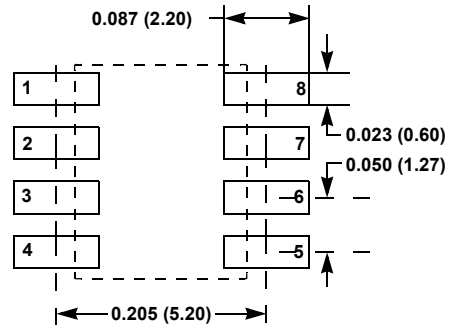
Top View



Side View



End View



Typical Recommended Land Pattern

Notes:

1. **Dimensions in inches (mm); scale = approximately 5X.**
2. **Pin spacing is a BASIC dimension; tolerances do not accumulate.**

7. Ordering Information

Part Number[1] [2]	Part Marking	Radiation Tolerance (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
ISL71610SLHMBZ	71610SLH	LDR to 75krad(Si)	8 Ld NSOIC	M8.15G	Tray	-55 to +125°C
ISL71610SLHMEV1Z	Evaluation Board					

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71610SLHM device page. For more information about MSL, see TB363.

8. Revision History

Rev.	Date	Description
2.2	May 6, 2021	Added link to features bullet. Updated Title. Updated File number to Renesas numbering.
2.1	Mar 19, 2021	Applied latest template. Updated ordering information table.
2.0	Feb 17, 2021	Updated the AS6294/1 and SEE Characterization feature bullets. Removed Radiation Tolerance section and subsections.
1.0	Dec 18, 2020	Initial Release

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(Rev.1.0 Mar 2020)

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