ISL70218SEH, ISL70218SRH

Radiation Hardened Dual 36V Precision Single-Supply, Rail-to-Rail Output, Low-Power Operational Amplifiers

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The ISL70218SEH, ISL70218SRH are dual, low-power precision amplifiers optimized for single-supply applications. These op amps feature a common-mode input voltage range extending to 0.5V below the V^- rail, a rail-to-rail differential input voltage range, and rail-to-rail output voltage swing, which makes it ideal for single-supply applications where input operation at ground is important.

These op amps feature low-power, low-offset voltage and low-temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. They are designed to operate over a single supply range of 3V to 36V or a split supply voltage range of +1.8V/-1.2V to ±18V. The combination of precision and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision instrumentation, data acquisition and precision power supply controls.

ISL70218SEH, ISL70218SRH are available in a 10 lead hermetic ceramic flatpack and operate across the extended temperature range of -55°C to +125°C.

Applications

- Precision instruments
- Active filter blocks
- Data acquisition
- Power supply control

Features

- **DLA SMD# 5962-12222 (ISL70218SEH Only)**
- **Wide single and dual supply range . . . . . 3V to 42V, Abs. Max.**
- **Low current consumption . . . . . .850µA, typical**
- **Low input offset voltage. . . . . 40µV, typical**
- **Rail-to-rail output . . . . . <10mV**
- Rail-to-rail input differential voltage range for comparator applications
- Operating temperature range. . . . . .-55°C to +125°C
- Below-ground (V^-) input capability to -0.5V
- Low noise voltage . . . . . .5.6nV/√Hz, typical
- Low noise current. . . . . 355fA/√Hz, typical
- Offset voltage temperature drift . . . . . .0.3µV/°C, typical
- No phase reversal
- Radiation acceptance testing - ISL70218SRH
  - HDR (50-300rad(Si)/s) . . . . . 100krad(Si)
- Radiation acceptance testing - ISL70218SEH
  - HDR (50-300rad(Si)/s) . . . . . 100krad(Si)
  - LDR (0.01rad(Si)/s) . . . . . .50krad(Si)
- SEE hardness (see SEE report for details)
  - SEB LET_{TH} (V_S = ±18V) . . . . . 86.4MeV•cm^2/mg
  - SEL Immune (SOI Process)

Related Literature

For a full list of related documents, visit our website:

- ISL70218SEH and ISL70218SRH device pages

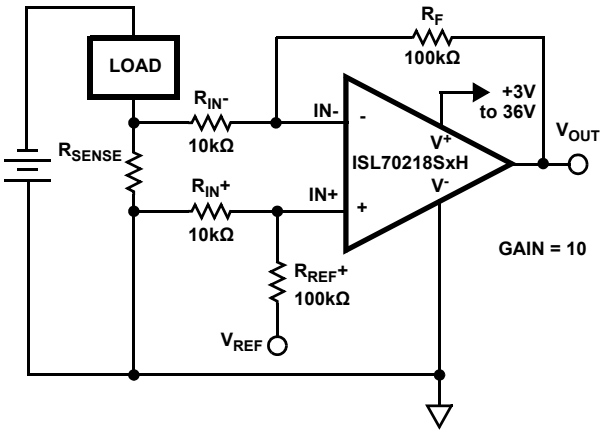


FIGURE 1. TYPICAL APPLICATION: SINGLE-SUPPLY, LOW-SIDE CURRENT SENSE AMPLIFIER

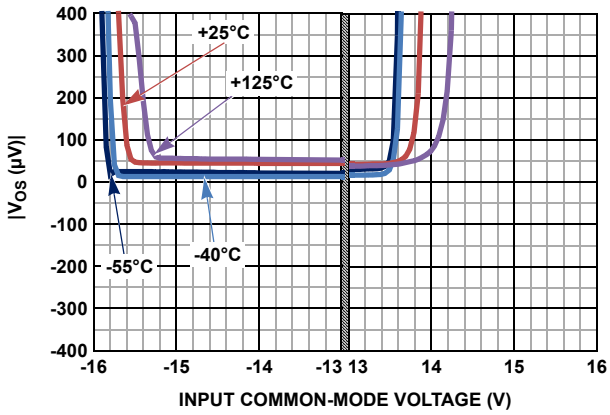
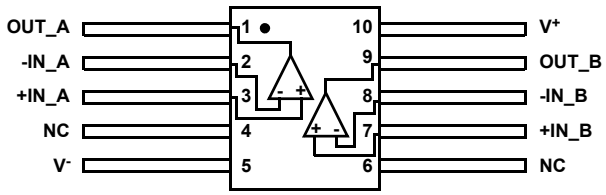


FIGURE 2. INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE, V_S = ±15V

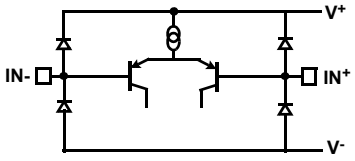
Pin Configuration

ISL70218SEH, ISL70218SRH
(10 LD FLATPACK)
TOP VIEW

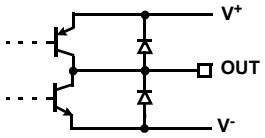


Pin Descriptions

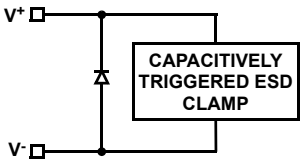
PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	OUT_A	Circuit 2	Amplifier A output
2	-IN_A	Circuit 1	Amplifier A inverting input
3	+IN_A	Circuit 1	Amplifier A noninverting input
4, 6	NC		No connect
5	V^-	Circuit 1, 2, 3	Negative power supply
7	+IN_B	Circuit 1	Amplifier B noninverting input
8	-IN_B	Circuit 1	Amplifier B inverting input
9	OUT_B	Circuit 2	Amplifier B output
10	V^+	Circuit 1, 2, 3	Positive power supply



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

ORDERING SMD NUMBER	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R1222201VXC (Note 2)	ISL70218SEHVF	HDR to 100krad(Si), LDR to 50krad(Si)	-55 to +125	10 Ld Flatpack	K10.A
5962R1222201V9A (Note 2)	ISL70218SEHVX (Note 3)		-55 to +125	Die	
NA	ISL70218SEHF/PROTO (Note 4)	N/A	-55 to +125	10 Ld Flatpack	K10.A
NA	ISL70218SEHX/SAMPLE (Notes 3, 4)	N/A	-55 to +125	Die	
NA	ISL70218SRHMF	HDR to 100krad(Si)	-55 to +125	10 Ld Flatpack	K10.A
NA	ISL70218SRHMX (Note 3)		-55 to +125	Die	
NA	ISL70218SRHF/PROTO (Note 4)	N/A	-55 to +125	10 Ld Flatpack	K10.A
NA	ISL70218SRHX/SAMPLE (Notes 3, 4)	N/A	-55 to +125	Die	
NA	ISL70218SRHMEVAL1Z (Note 5)	Evaluation Board			

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 4.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Supply Voltage (Note 8). 36V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage . . . . . V^- - 0.5V to V^+ + 0.5V
Min/Max Input Voltage . . . . . V^- - 0.5V to V^+ + 0.5V
Max/Min Input Current . . . . . ±20mA
Output Short-Circuit Duration (1 output at a time) . . . . . Indefinite
ESD Tolerance
Human Body Model (Tested per MIL-PRF-883 3015.7). 2kV
Machine Model (Tested per JESD22-A115-A) 300V
Charged Device Model (Tested per CDM-22CIOID). 750V
Dielectrically Isolated PR40 Process . . . . . Latch-Up Free

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld Flatpack Package (Notes 6, 7)	130	20

Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Supply Voltage . . . . . 3V (+1.8V/-1.2V) to 30V (±15V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See TB379 for details.
7. For θ_{JC}, the "case temp" location is the center of the package underside.
8. Tested in a heavy ion environment at LET = 86.4 MeV•cm^2/mg at +125°C (T_C) for SEB. See AN1677 for more information.

Electrical Specifications

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{OS}	Offset Voltage			40	230	µV
					290	µV
TCV_{OS}	Offset Voltage Drift			0.3	**1.4**	µV/°C
ΔV_{OS}	Input Offset Voltage Match Channel-to-Channel			44	280	µV
					365	µV
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
I_B	Input Bias Current		-575	-230		nA
			-800			nA
V_{CMIR}	Common-Mode Input Voltage Range	Guaranteed by CMRR Test	(V^-) - 0.5		(V^+) - 1.8	V
			V^-		**(V^+) - 1.8**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = V^- to V^+ -1.8V	100	118		dB
		V_{CM} = V^- to V^+ -1.8V	**97**			dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage	105	124		dB
			100			dB
A_{VOL}	Open-Loop Gain	R_L = 10kΩ to ground, V_O = -13V to +13V	120	130		dB
			115			dB
V_{OH}	Output Voltage High, V^+ to V_{OUT}	R_L = 10kΩ			110	mV
					120	mV
V_{OL}	Output Voltage Low, V_{OUT} to V^-	R_L = 10kΩ			70	mV
					80	mV
I_S	Supply Current/Amplifier			0.85	1.10	mA
					1.4	mA
I_{S+}	Source Current Capability		10			mA

Electrical Specifications

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
I_{S-}	Sink Current Capability		10			mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	3		40	V
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2k		4		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz, V_S = ±18V		300		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz, V_S = ±18V		8.5		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz, V_S = ±18V		5.8		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz, V_S = ±18V		5.6		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz, V_S = ±18V		5.6		nV/√Hz
in	Current Noise Density	f = 1kHz, V_S = ±18V		355		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 10V_{P-P}	±1.0	±1.2		V/µs
			±0.4			V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100	200	ns
					400	ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100	230	ns
					400	ns
t_s	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		8.5		µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
					35	%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
					35	%

Electrical Specifications

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) (ISL70218SEH only) with exposure at a low dose rate of <10mrad(Si)/s.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{OS}	Offset Voltage			40	230	µV
					290	µV
TCV_{OS}	Offset Voltage Drift			0.3	**1.4**	µV/°C
ΔV_{OS}	Input Offset Voltage Match Channel-to-Channel			44	280	µV
					365	µV
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
I_B	Input Bias Current		-575	-230		nA
			-1500			nA

Electrical Specifications V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) (ISL70218SEH only) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{CMIR}	Common-Mode Input Voltage Range	Guaranteed by CMRR Test	(V^-) - 0.5		(V^+) -1.8	V
			V^-		**(V^+) - 1.8**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = V^- to V^+ -1.8V	100	118		dB
		V_{CM} = V^- to V^+ -1.8V	**97**			dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage	105	124		dB
			100			dB
A_{VOL}	Open-Loop Gain	R_L = 10kΩ to ground V_O = -13V to +13V	120	130		dB
			115			dB
V_{OH}	Output Voltage High, V^+ to V_{OUT}	R_L = 10kΩ			110	mV
					120	mV
V_{OL}	Output Voltage Low, V_{OUT} to V^-	R_L = 10kΩ			70	mV
					80	mV
I_S	Supply Current/Amplifier			0.85	1.1	mA
					1.4	mA
I_{S+}	Source Current Capability		10			mA
I_{S-}	Sink Current Capability		10			mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	3		40	V
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2kΩ		4		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz, V_S = ±18V		300		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz, V_S = ±18V		8.5		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz, V_S = ±18V		5.8		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz, V_S = ±18V		5.6		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz, V_S = ±18V		5.6		nV/√Hz
in	Current Noise Density	f = 1kHz, V_S = ±18V		355		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 10V_{P-P}	±1.0	±1.2		V/µs
			±0.4			V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100	230	ns
					400	ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100	200	ns
					400	ns
t_s	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		8.5		µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
					35	%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
					35	%

Electrical Specifications

V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{OS}	Offset Voltage			40		µV
ΔV_{OS}	Input Offset Voltage Match Channel to Channel			44		µV
I_{OS}	Input Offset Current			4		nA
I_B	Input Bias Current			-230		nA
V_{CMIR}	Common-Mode Input Voltage Range	Guaranteed by CMRR Test	(V^-) - 0.5		(V^+) - 1.8	V
			V^-		**(V^+) - 1.8**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = V^- - 0.5V to V^+ - 1.8 V_{CM} = V^- to V^+ - 1.8V		117		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage		124		dB
A_{VOL}	Open-Loop Gain	R_L = 10kΩ to ground V_O = -3V to +3V		130		dB
V_{OH}	Output Voltage High, V^+ to V_{OUT}	R_L = 10kΩ		65		mV
				70		mV
V_{OL}	Output Voltage Low, V_{OUT} to V^-	R_L = 10kΩ		38		mV
				45		mV
I_S	Supply Current/Amplifier			0.85		mA
I_{S+}	Source Current Capability			8		mA
I_{S-}	Sink Current Capability			8		mA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			3.2		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		320		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		9		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		5.7		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz		5.5		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		5.5		nV/√Hz
in	Current Noise Density	f = 1kHz		380		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 1.25V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 4V_{P-P}		±1		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	AV = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
t_s	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 4V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		4		µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

High Dose Rate Post Radiation Characteristics

V_S ±15V, V_{CM} = 0V, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.**

SYMBOL	PARAMETER	TEST CONDITIONS	50k RAD	75k RAD	100k RAD	UNIT
V_{OS}	Offset Voltage		35	35	35	µV
I_{OS}	Input Offset Current		2	3	5	nA
I_B	Input Bias Current		200	400	575	nA
CMRR	Common-Mode Rejection Ration	V_{CM} = -13V to +13V	129	128	127	dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±15V	130	130	130	dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V R_L = 10kΩ to ground	131.6	131.1	131.1	dB
V_{OH}	Output Voltage High V^+ to V_{OUT}	R^L = 10kΩ to ground	71	74	76	mV
V_{OL}	Output Voltage Low V_{OUT} to V^-	R_L = 10kΩ to ground	54	57	59	mV
I_S	Supply Current/Amplifier		830	830	830	µA
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 10, R_L = 2kΩ, V_O = $4V_{P-P}$	1.24	1.23	1.22	V/µs

Low Dose Rate Post Radiation Characteristics

V_S ±15V, V_{CM} = 0V, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **This data is typical test data post radiation exposure at a rate of 10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.**

SYMBOL	PARAMETER	TEST CONDITIONS	10k RAD	20k RAD	50k RAD	UNIT
V_{OS}	Offset Voltage		20	20	20	µV
I_{OS}	Input Offset Current		6	8	10	nA
I_B	Input Bias Current		300	500	1200	nA
I_S	Supply Current/Amplifier		650	625	615	µA

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

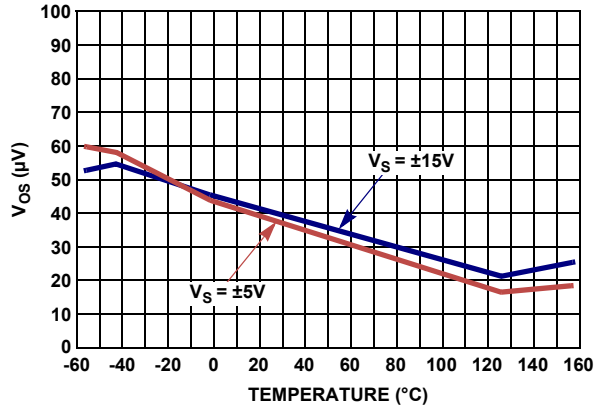


FIGURE 3. V_{OS} vs TEMPERATURE

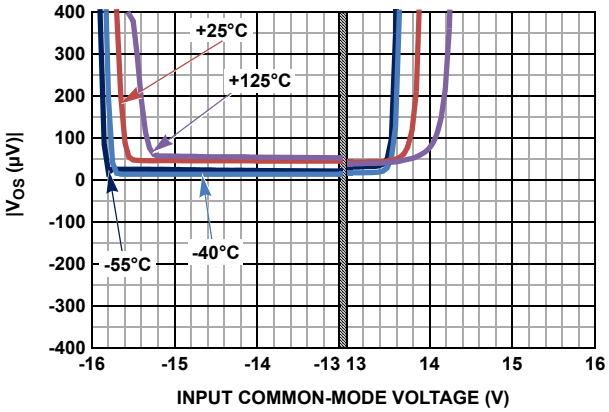


FIGURE 4. INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE, V_S = ±15V

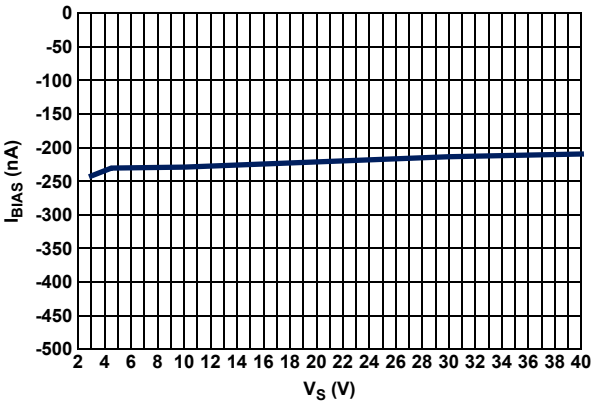


FIGURE 5. I_{BIAS} vs V_S

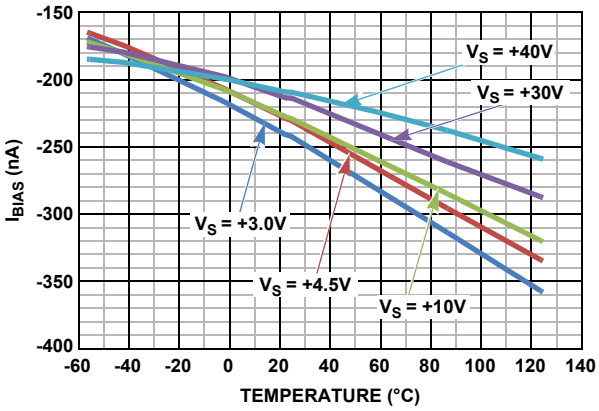


FIGURE 6. I_{BIAS} vs TEMPERATURE vs SUPPLY

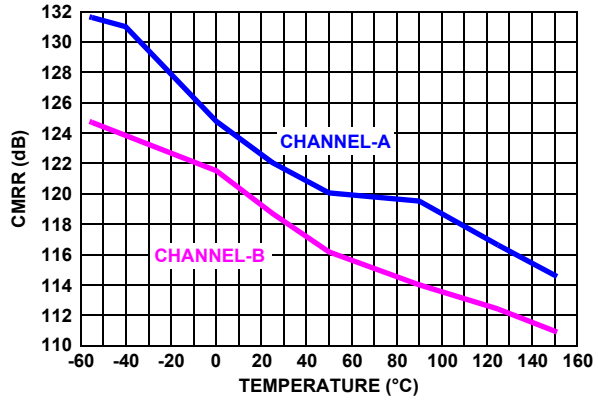


FIGURE 7. CMRR vs TEMPERATURE, V_S = ±15V

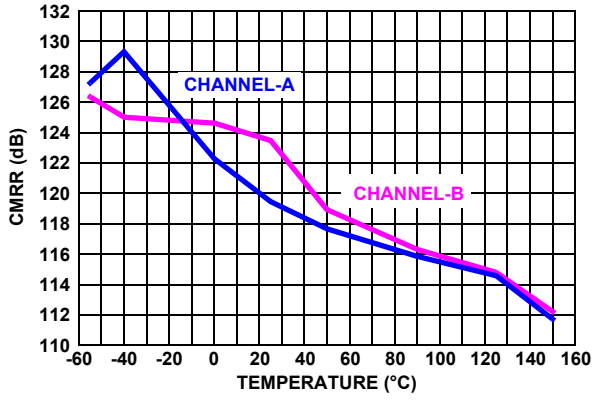


FIGURE 8. CMRR vs TEMPERATURE, V_S = ±5V

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

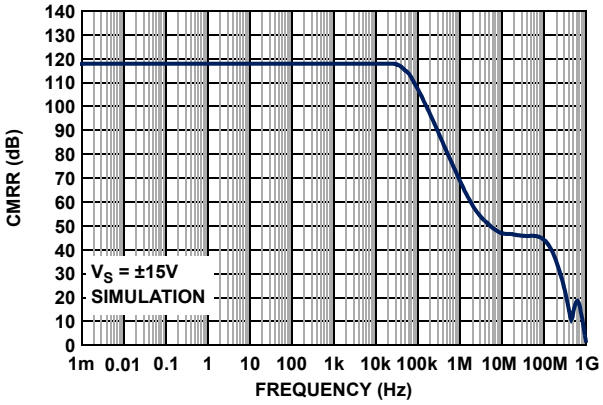


FIGURE 9. CMRR vs FREQUENCY, $V_S = \pm15V$

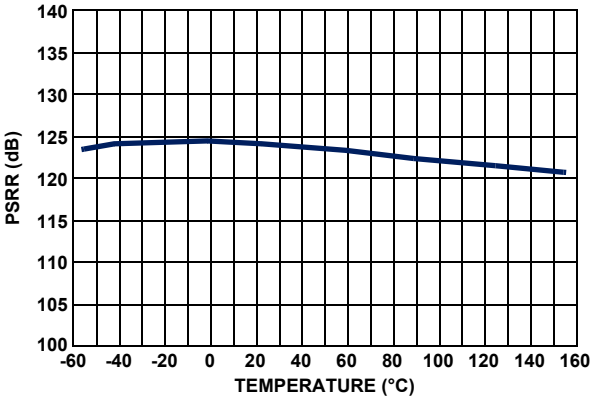


FIGURE 10. PSRR vs TEMPERATURE, $V_S = \pm15V$

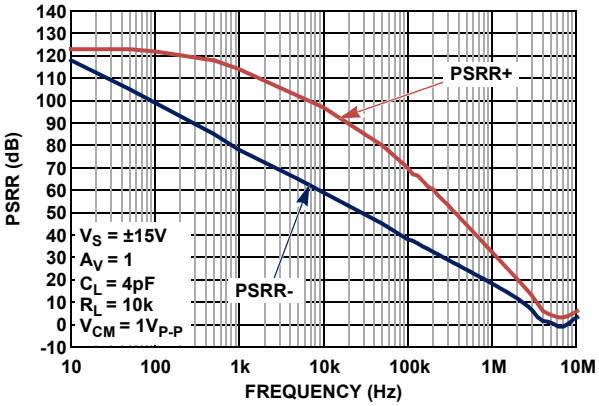


FIGURE 11. PSRR vs FREQUENCY, $V_S = \pm15V$

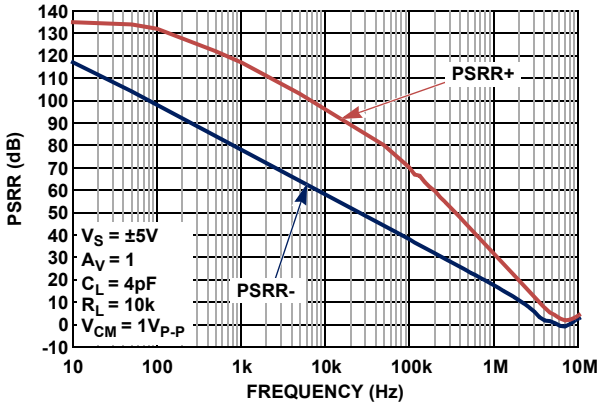


FIGURE 12. PSRR vs FREQUENCY, $V_S = \pm5V$

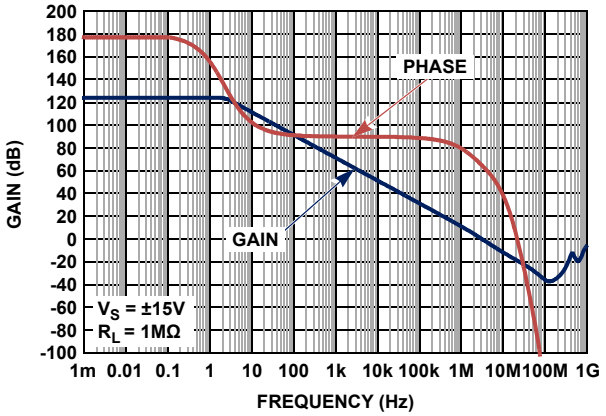


FIGURE 13. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $V_S = \pm15V$

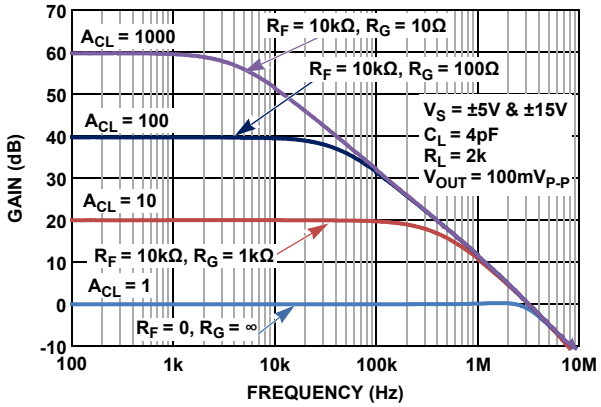


FIGURE 14. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

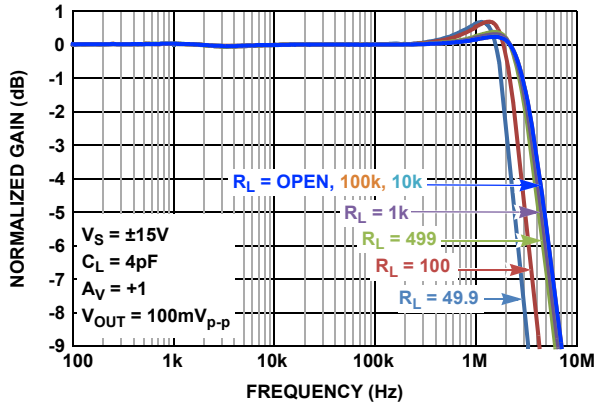


FIGURE 15. GAIN vs FREQUENCY vs R_L, $V_S = \pm15V$

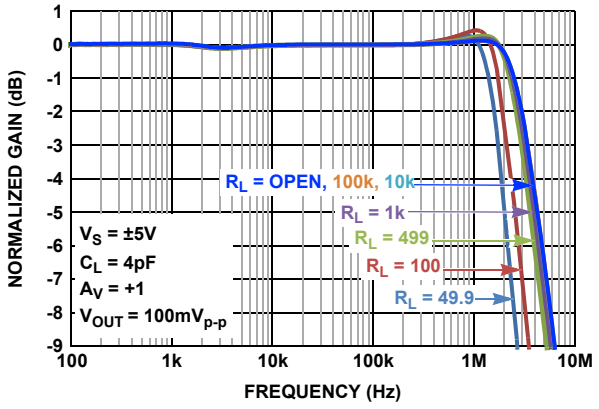


FIGURE 16. GAIN vs FREQUENCY vs R_L, $V_S = \pm5V$

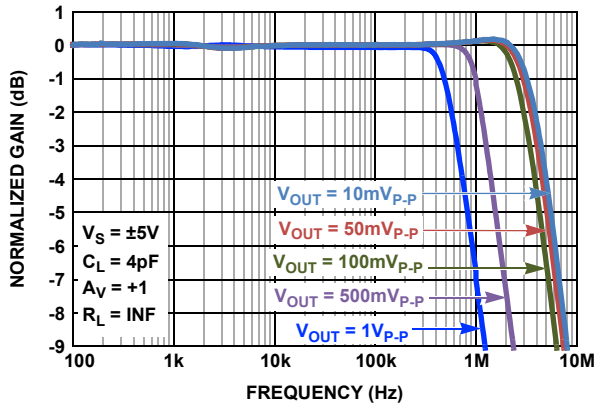


FIGURE 17. GAIN vs FREQUENCY vs OUTPUT VOLTAGE

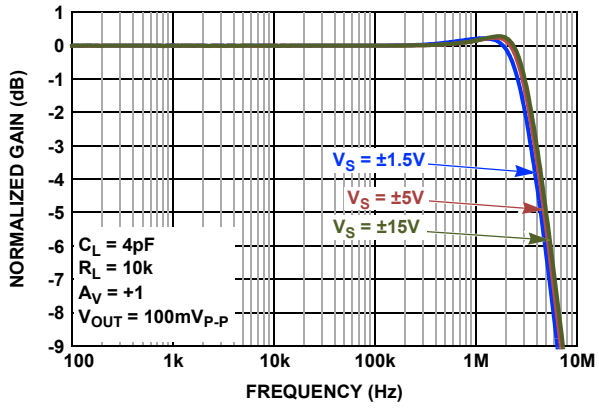


FIGURE 18. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

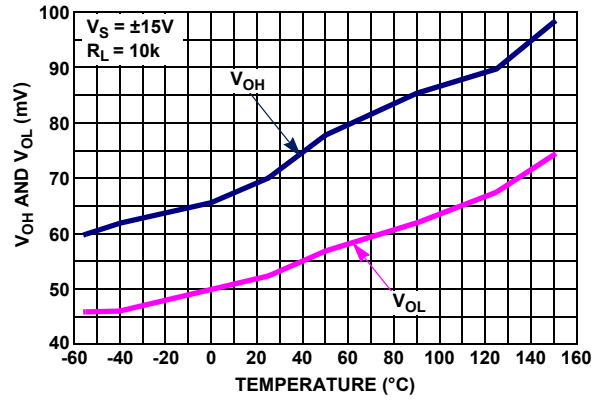


FIGURE 19. OUTPUT OVERHEAD VOLTAGE vs TEMPERATURE, $V_S = \pm15V$, $R_L = 10k$

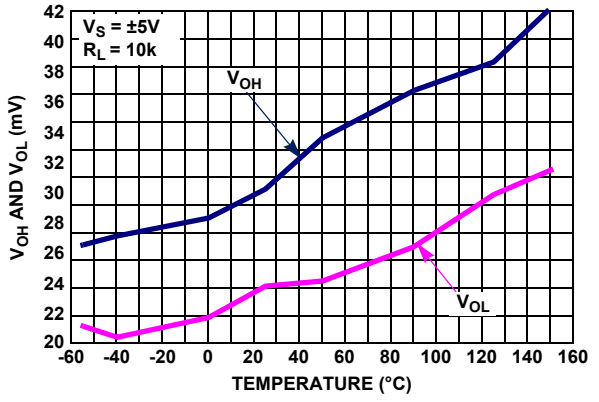


FIGURE 20. OUTPUT OVERHEAD VOLTAGE vs TEMPERATURE, $V_S = \pm5V$, $R_L = 10k$

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

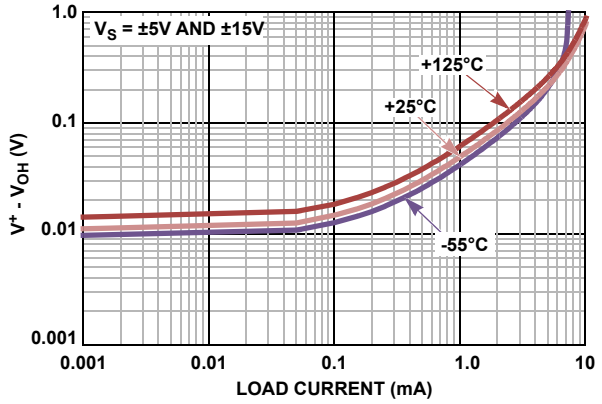


FIGURE 21. OUTPUT OVERHEAD VOLTAGE HIGH vs LOAD CURRENT, V_S = ±5V AND ±15V

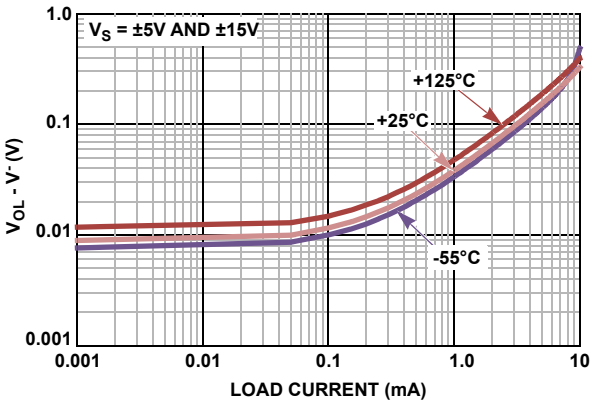


FIGURE 22. OUTPUT OVERHEAD VOLTAGE LOW vs LOAD CURRENT, V^S = ±5V AND ±15V

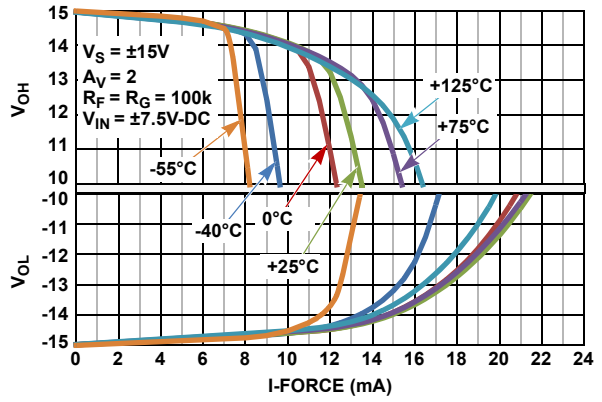


FIGURE 23. OUTPUT VOLTAGE SWING vs LOAD CURRENT, V_S = ±15V

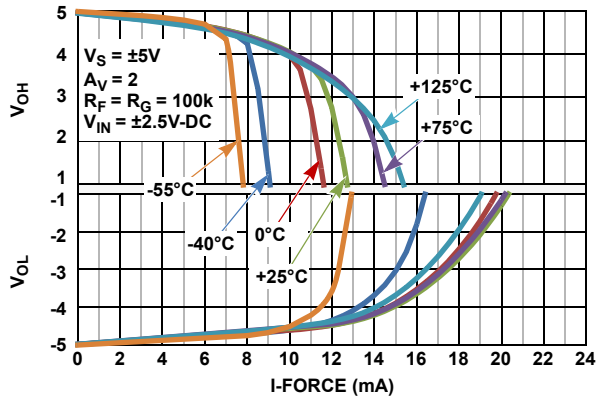


FIGURE 24. OUTPUT VOLTAGE SWING vs LOAD CURRENT, V_S = ±5V

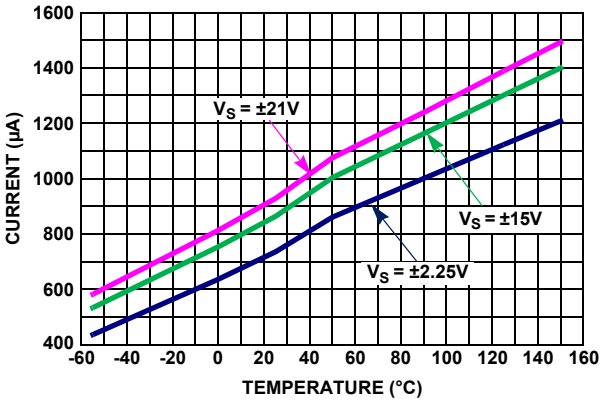


FIGURE 25. SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

FIGURE 26. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

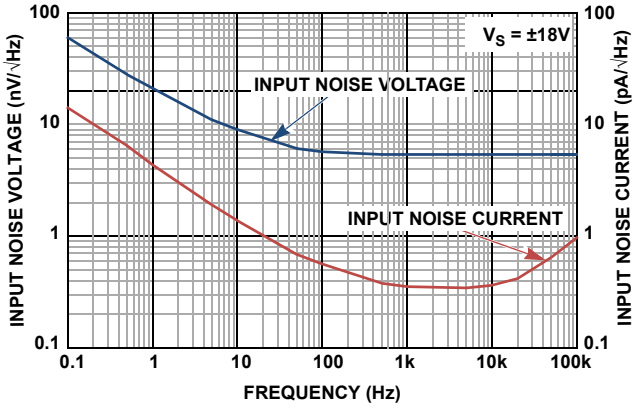


FIGURE 27. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, V_S = ±18V

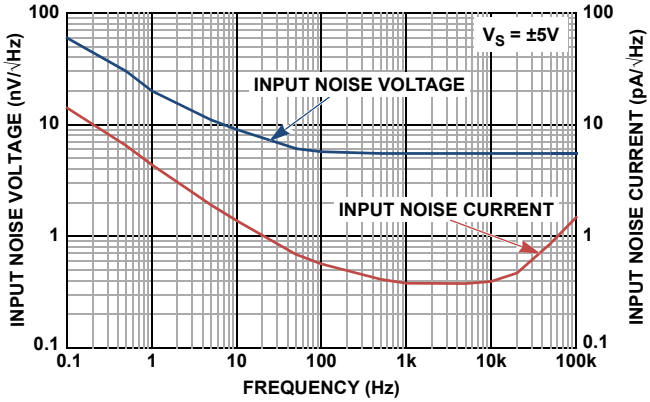


FIGURE 28. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, V_S = ±5V

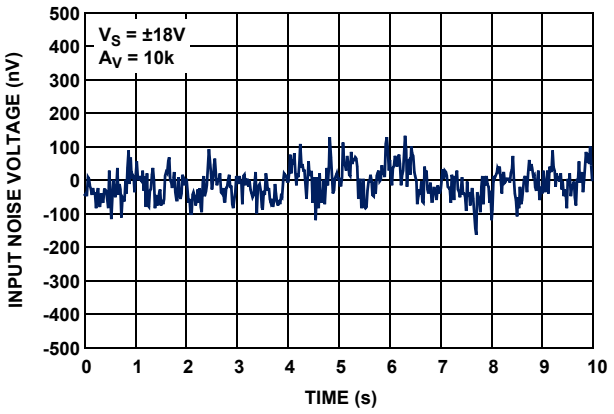


FIGURE 29. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, V_S = ±18V

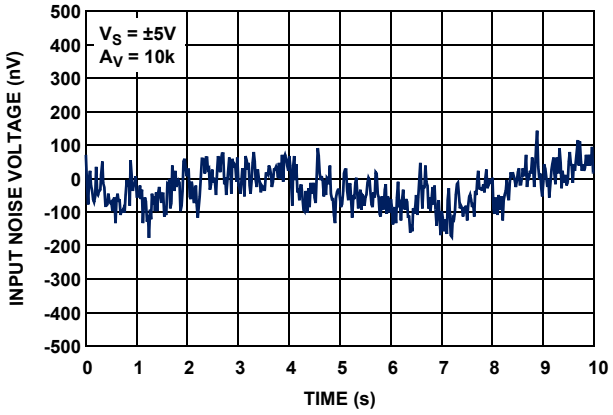


FIGURE 30. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, V_S = ±5V

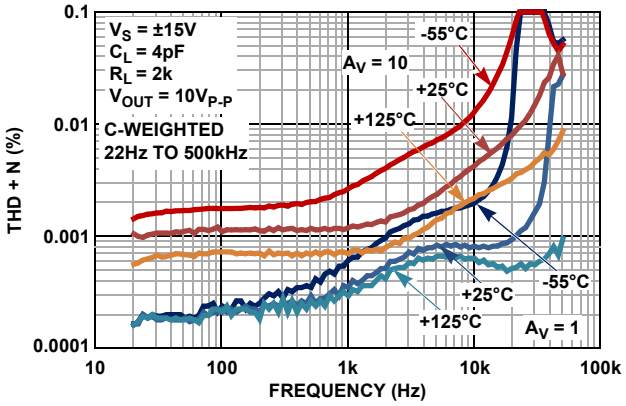


FIGURE 31. THD+N vs FREQUENCY vs TEMPERATURE, A_V = 1, 10, R_L = 2k

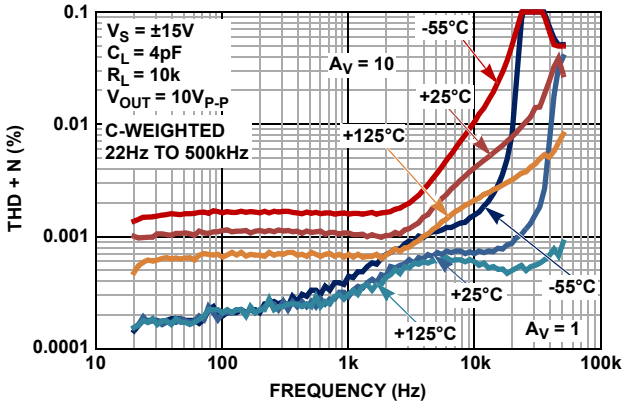


FIGURE 32. THD+N vs FREQUENCY vs TEMPERATURE, A_V = 1, 10, R_L = 10k

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

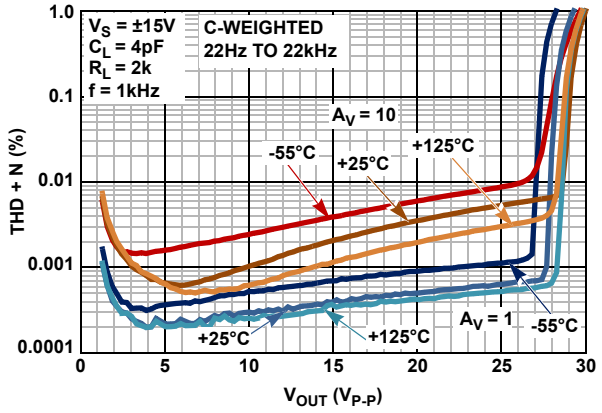


FIGURE 33. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 2k

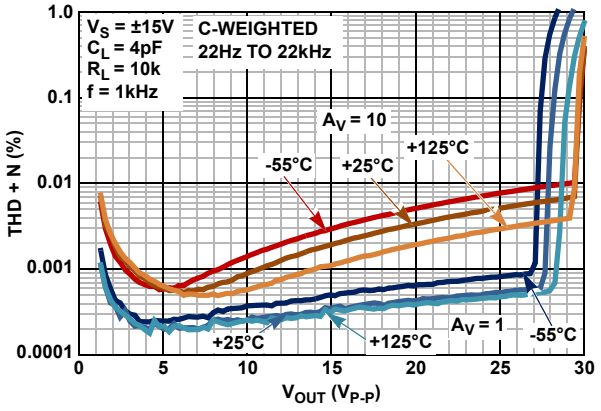


FIGURE 34. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 10k

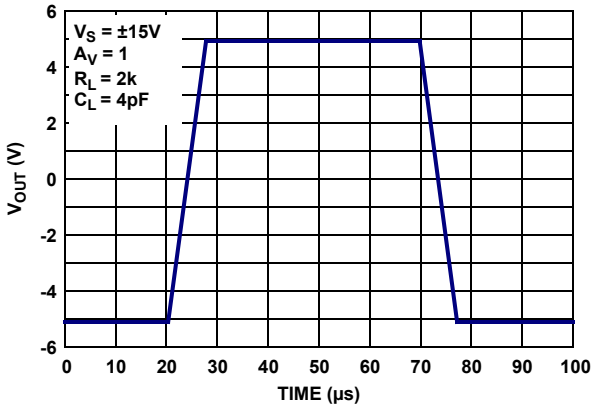


FIGURE 35. LARGE SIGNAL 10V STEP RESPONSE, V_S = ±15V

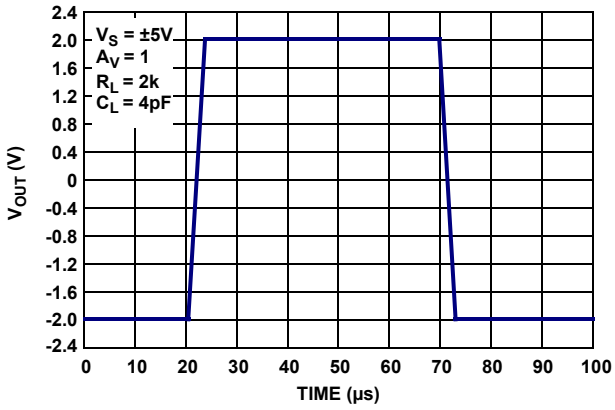


FIGURE 36. LARGE SIGNAL 4V STEP RESPONSE, V_S = ±5V

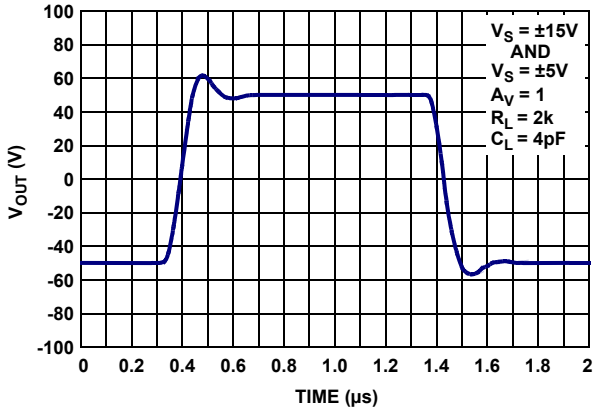


FIGURE 37. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

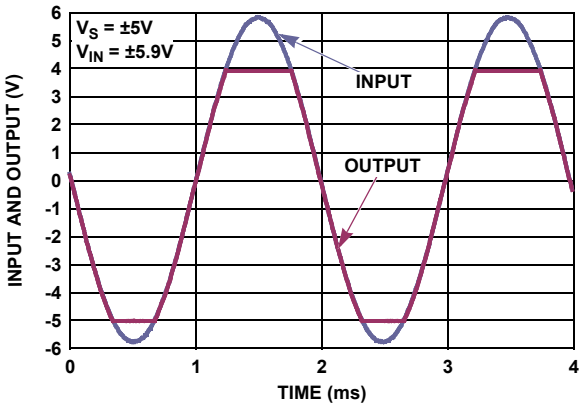


FIGURE 38. NO PHASE REVERSAL

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

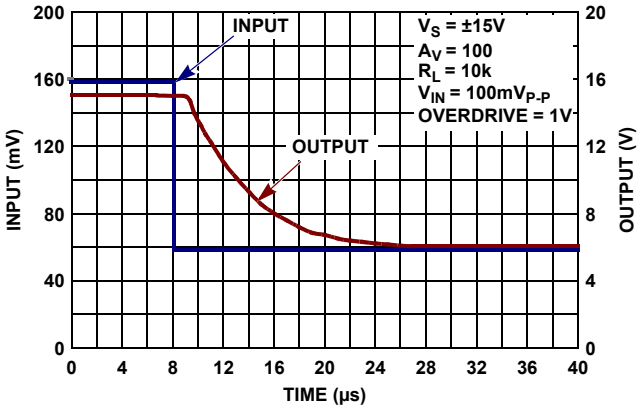


FIGURE 39. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

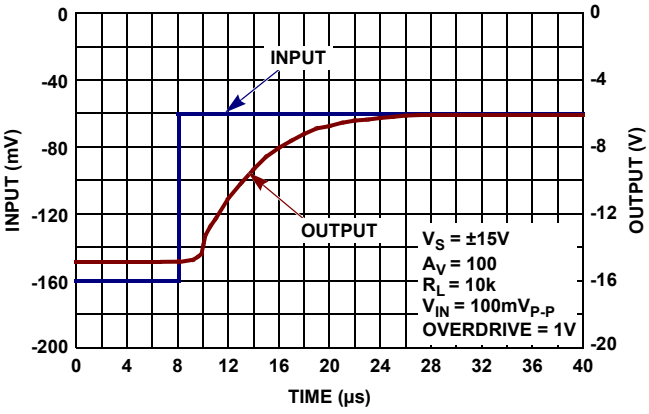


FIGURE 40. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

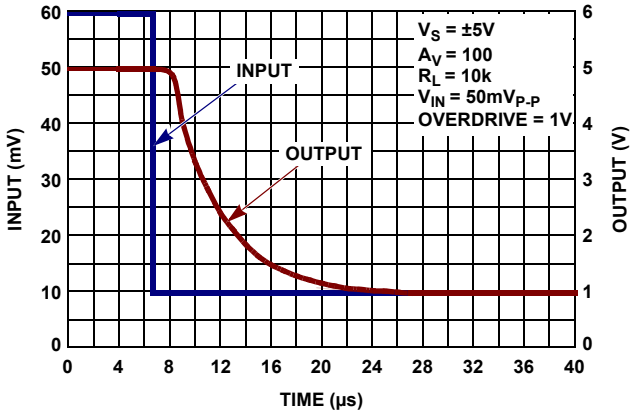


FIGURE 41. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

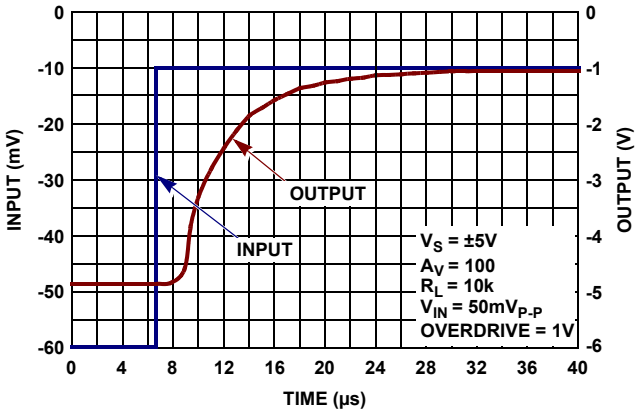


FIGURE 42. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

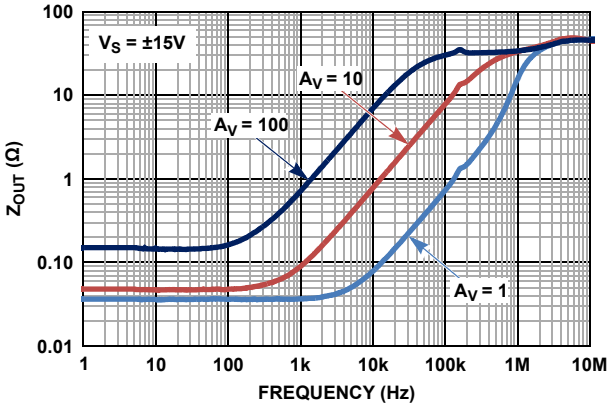


FIGURE 43. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±15V

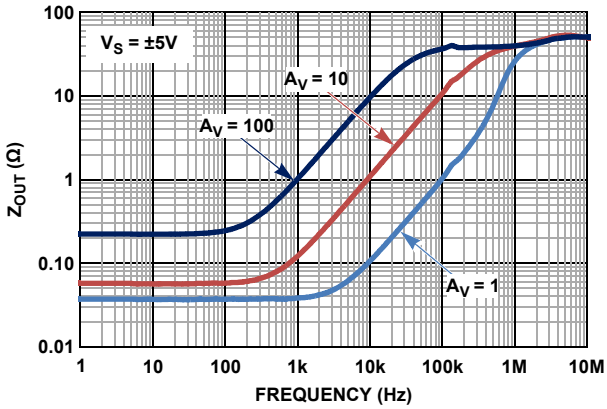


FIGURE 44. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

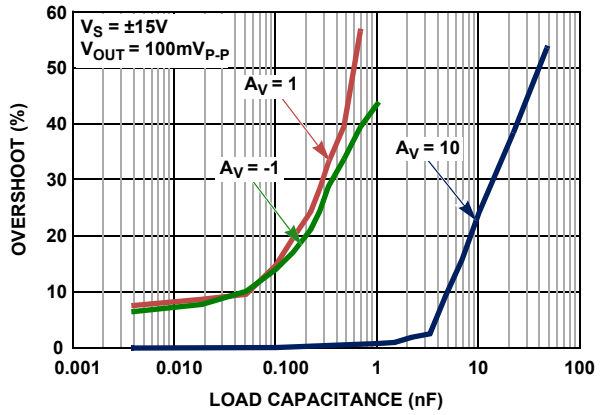


FIGURE 45. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±15V

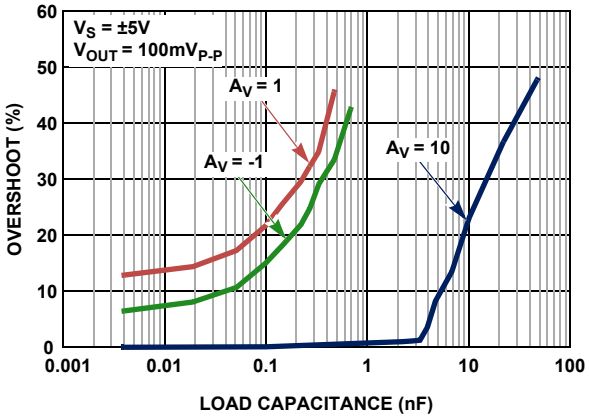


FIGURE 46. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±5V

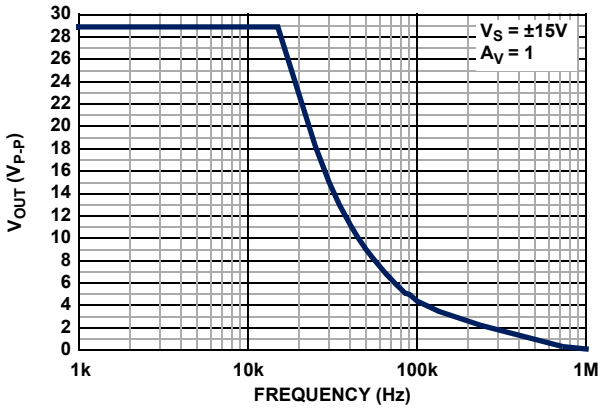


FIGURE 47. I_{MAX} OUTPUT VOLTAGE vs FREQUENCY

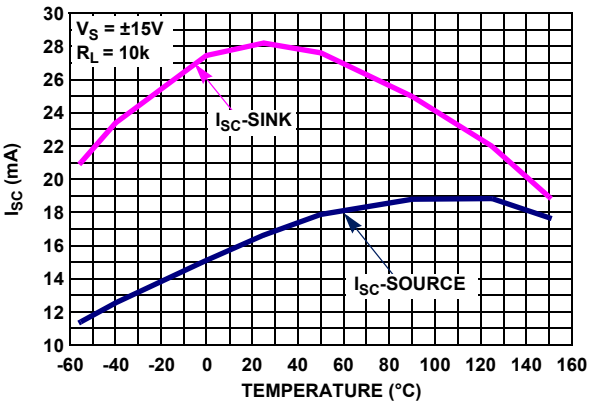


FIGURE 48. SHORT-CIRCUIT CURRENT vs TEMPERATURE, V_S = ±15V

Applications Information

Functional Description

The ISL70218SEH, ISL70218SRH are dual, 3.2MHz, single or dual supply, rail-to-rail output amplifiers with a common-mode input voltage range extending to a range of 0.5V below the V^- rail. The input stage is optimized for precision sensing of ground-referenced signals in single-supply applications. The input stage is able to handle large input differential voltages without phase inversion, making this amplifier suitable for high-voltage comparator applications. The bipolar design features high open loop gain and excellent DC input and output temperature stability. This op amp features very low quiescent current of 850µA, and low temperature drift. The devices are fabricated in a new precision 40V complementary bipolar DI process and is immune from latch-up for up to a 36V supply range.

Operating Voltage Range

The op amps are designed to operate over a single supply range of 3V to 36V or a split supply voltage range of +1.8V/-1.2V to ±18V. The device is fully characterized at 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete operating voltage range. Parameter variation with operating voltage is shown in the "Typical Performance Curves" beginning on page 9.

The input common-mode voltage to the V^+ rail (V^+ - 1.8V across the full temperature range) may limit amplifier operation when operating from split V^+ and V^- supplies. Figure 4 shows the common-mode input voltage range variation over temperature.

Input Stage Performance

The ISL70218SEH, ISL70218SRH PNP input stage has a common-mode input range extending up to 0.5V below ground at +25°C. Full amplifier performance is guaranteed for input voltage down to ground (V^-) across the -55°C to +125°C temperature range. For common-mode voltages down to -0.5V below ground (V-), the amplifiers are fully functional, but performance degrades slightly over the full temperature range. This feature provides excellent CMRR, AC performance, and DC accuracy when amplifying low-level, ground-referenced signals.

The input stage has a maximum input differential voltage equal to a diode drop greater than the supply voltage and does not contain the back-to-back input protection diodes found on many similar amplifiers. This feature enables the device to function as a precision comparator by maintaining very high input impedance for high-voltage differential input comparator voltages. The high differential input impedance also enables the device to operate reliably in large signal pulse applications, without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. Thus, input signal distortion caused by nonlinear clamps under high slew rate conditions is avoided.

In applications in which one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current-limiting resistors may be needed at each input terminal (see Figure 49, R_{IN+}, R_{IN-}) to limit current through the power-supply ESD diodes to 20mA.

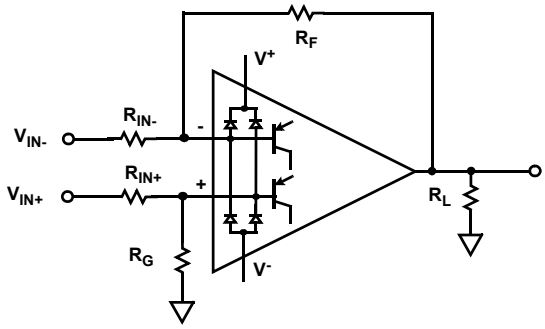


FIGURE 49. INPUT ESD DIODE CURRENT LIMITING

Output Drive Capability

The bipolar rail-to-rail output stage features low saturation levels that enable an output voltage swing to less than 15mV when the total output load (including feedback resistance) is held below 50µA (Figures 21 and 22). With ±15V supplies, this can be achieved by using feedback resistor values >300kΩ.

The output stage is internally current limited. Output current limit over temperature is shown in Figures 23 and 24. The amplifiers can withstand a short-circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only one amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long-term reliability.

The amplifiers perform well when driving capacitive loads (Figures 45 and 46). The unity gain, voltage follower (buffer) configuration provides the highest bandwidth but is also the most sensitive to ringing produced by load capacitance found in BNC cables. Unity gain overshoot is limited to 35% at capacitance values to 0.33nF. At gains of 10 and higher, the device is capable of driving more than 10nF without significant overshoot.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL70218SEH, ISL70218SRH are immune to output phase reversal out to 0.5V beyond the rail ($V_{ABS\ MAX}$) limit (see Figure 38 on page 14).

Single Channel Usage

The ISL70218SEH, ISL70218SRH are dual op amps. If the application requires only one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel oscillates if the input and output pins are floating. This results in higher-than-expected supply currents and possible noise injection into the channel being used. The proper way to prevent oscillation is to short the output to the inverting input, and ground the positive input (Figure 50).

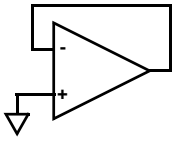


FIGURE 50. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

Where

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- T_{MAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package

PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

Where

- PD_{MAX} = Maximum power dissipation of one amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Package Characteristics

Weight of Packaged Device

0. 4029 grams (Typical)

Lid Characteristics

Finish: Gold
Case Isolation to Any Lead: 20 x 10^9 Ω (min)

Die Characteristics

Die Dimensions

1565µm x 2125µm (62 mils x 84 mils)
Thickness: 355µm ±25µm (14 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

Dielectrically Isolated Complementary Bipolar - PR40

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

< 2 x 10^5 A/cm^2

Metallization Mask Layout

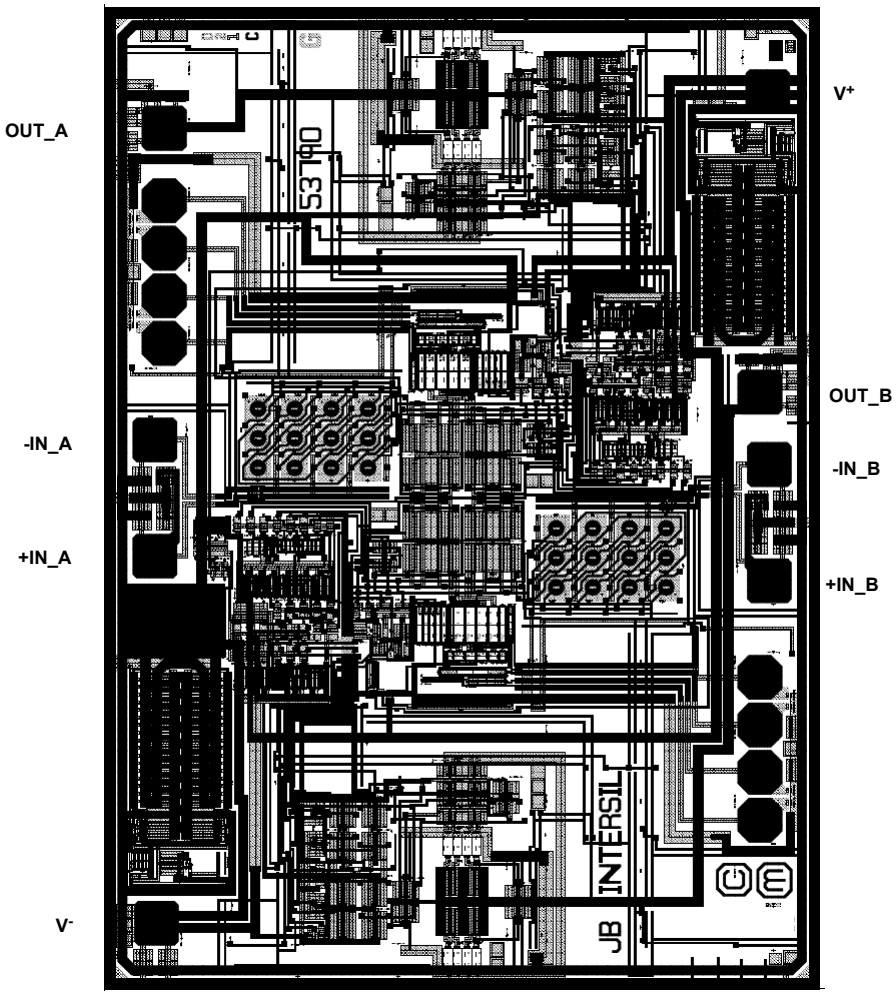


TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
OUT_A	1	16.5	1670	70	70	1
-IN_A	6	-3	1015	70	70	1
+IN_A	7	-3	771	70	70	1
V^-	8	0	0	70	70	1
+IN_B	13	1287	719.5	70	70	1
-IN_B	14	1287	963.5	70	70	1
OUT_B	15	1267.5	1115.5	70	70	1
V^+	16	1284	1746.5	70	70	1

NOTE:

10. Origin of coordinates is the centroid of pad 8.

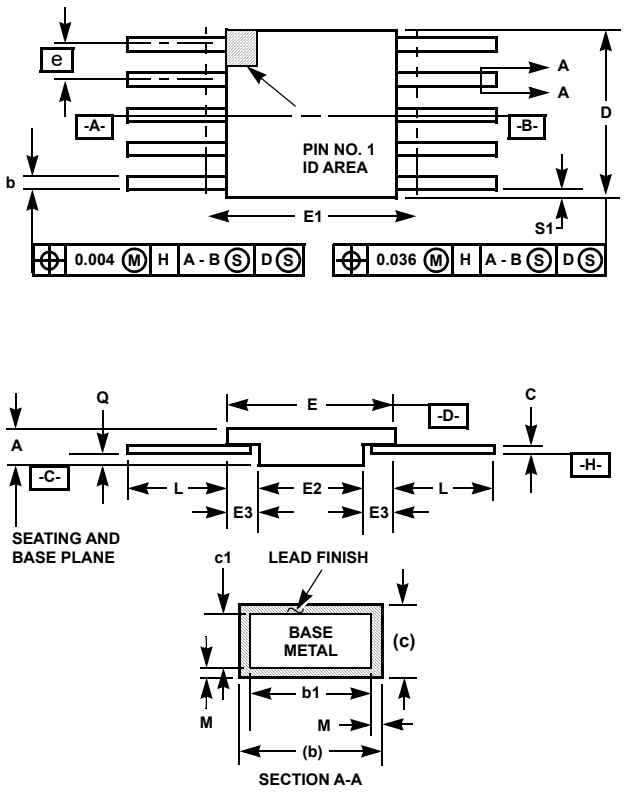
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jun 12, 2020	4.01	Updated the Pad Numbers for last four pads in Table 1.
Feb 7, 2020	4.00	Updated Features bullets for Radiation acceptance testing Updated Related Literature section Ordering Information table: - Updated part number ISL70218SEHVX/SAMPLE to ISL70218SEHX/SAMPLE - Added Radiation Hardness column - Added Notes 3, 4, and 5 to Ordering Information table. Updated Electrical Spec table for radiation Boldface note From: Boldface limits apply over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. To: Boldface limits apply over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) (ISL70218SEH only) with exposure at a low dose rate of <10mrad(Si)/s. Figures 27 and 28, changed Input Noise Current unit of measurement from fA to pA. Removed About Intersil section Updated Disclaimer
May 19, 2016	3.00	Added ISL70218SRH information to datasheet. Removed Pb-Free Reflow Profile information from Thermal Information section as it is not applicable to hermetic packages.
July 24, 2014	2.00	Updated Features on page 1, Radiation Tolerance bullet as follows: from • Radiation Tolerance - SEL/SEB LET_{TH} (V_S = ±18V) . . . . . .86.4 MeV*cm^2/mg - High Dose Rate . . . . . .100krad(Si) - Low Dose Rate . . . . . .100krad(Si) to • Radiation tolerance - High dose rate (50-300rad(Si)/s) . . . . . .100krad(Si) - Low dose rate (0.01rad(Si)/s) . . . . . .100krad(Si)* - SEB LET_{TH} (V_S = ±18V) . . . . . .86.4 MeV•cm^2/mg - SEL Immune (SOI Process) Updated the Ordering Information table on page 3 as follows: - Removed MSL note. - Added SMD ordering note. Replaced the Products verbiage with the About Intersil Verbiage on page 21.
August 24, 2012	1.00	1. Electrical Specification tables (pages 3-6), added specs on overshoot and rise/fall times. 2. Page 3 - Added Abs Max in a non radiation environment Changed ESD HBM from 3kV to 2kV Changed ESD CDM from 2kV to 750V
February 16, 2012	0.00	Initial Release

Package Outline Drawing

For the most recent package outline drawing, see K10.A.



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, Configuration B)
10 Lead Ceramic Metal Seal Flatpack Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

Rev. 0 3/07

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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