

ISL6421A

Single Output LNB Supply and Control Voltage Regulator with I<sup>2</sup>C Interface for Advanced Satellite Set-top Box Designs

FN9167  
Rev 3.00  
Mar 9, 2006

The ISL6421A is a highly integrated solution for providing power and control signals from advanced satellite set-top box (STB) modules to the low noise block (LNB). The internal architecture of this device contains a current-mode boost PWM and a low-noise linear regulator, along with the circuitry required for I<sup>2</sup>C device interfacing and for providing DiSEqC™ standard control signals to the LNB.

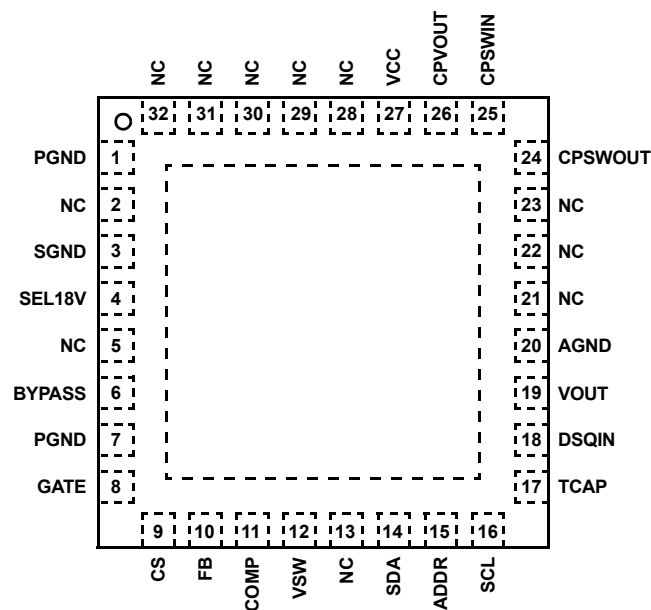
A regulated output voltage is available at the output terminal (VOUT) to support the operation of the antenna port in advanced satellite STB applications. The regulated output may be set to either 13V or 18V by use of the voltage select command bit (VSEL) through the I<sup>2</sup>C bus. Additionally, to compensate for the voltage drop in the coaxial cable, the voltage may be increased by 1V with the line length compensation bit (LLC) feature. The device can be put into a standby mode by means of the enable bit (EN), this disables the PWM and Linear regulator combination and helps conserve power.

The input to the linear regulator is derived from the current mode boost converter, such that the required voltage is the sum of the output voltage and the linear regulator drop (1.0V typical). This ensures that the power dissipation is minimized and maintains a constant voltage drop across the linear pass element, while permitting an adequate voltage range for tone injection.

The device is capable of providing 450mA (typical). The overcurrent limit is either digitally or resistor programmable.

Pinout

ISL6421A (QFN) TOP VIEW



Features

- Switch-Mode Power Converter for Lowest Dissipation
  - Boost PWM with >92% Efficiency
  - Selectable 13V or 18V Outputs
  - Digital Cable Length Compensation (1V)
  - Vsw tracks Vout ensures low dissipation
- I<sup>2</sup>C Compatible Interface for Remote Device Control
  - Registered Slave Address 0001 00XX
  - Fully Functional 3.3V, 5V Operation up to 400kHz
- Built-In Tone Oscillator Factory Trimmed to 22kHz
  - Facilitates DiSEqC™ (EUTELSAT) Encoding
  - External Modulation input DSQIN
- Internal Over Temperature Protection and Diagnostics
- Internal Overload and Over Temperature Flags (Visible on I<sup>2</sup>C)
- Output Back-Bias Protection to 24V
- LNB Short-Circuit Protection and Diagnostics
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint
- External Pins to Select 13V/18V Options
- Pb-Free Available (RoHS Compliant)

Applications

- LNB Power Supply and Control for Satellite Set-Top Box

References

- Tech Brief 389 (TB389) - "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"; Available on the Intersil website, www.intersil.com

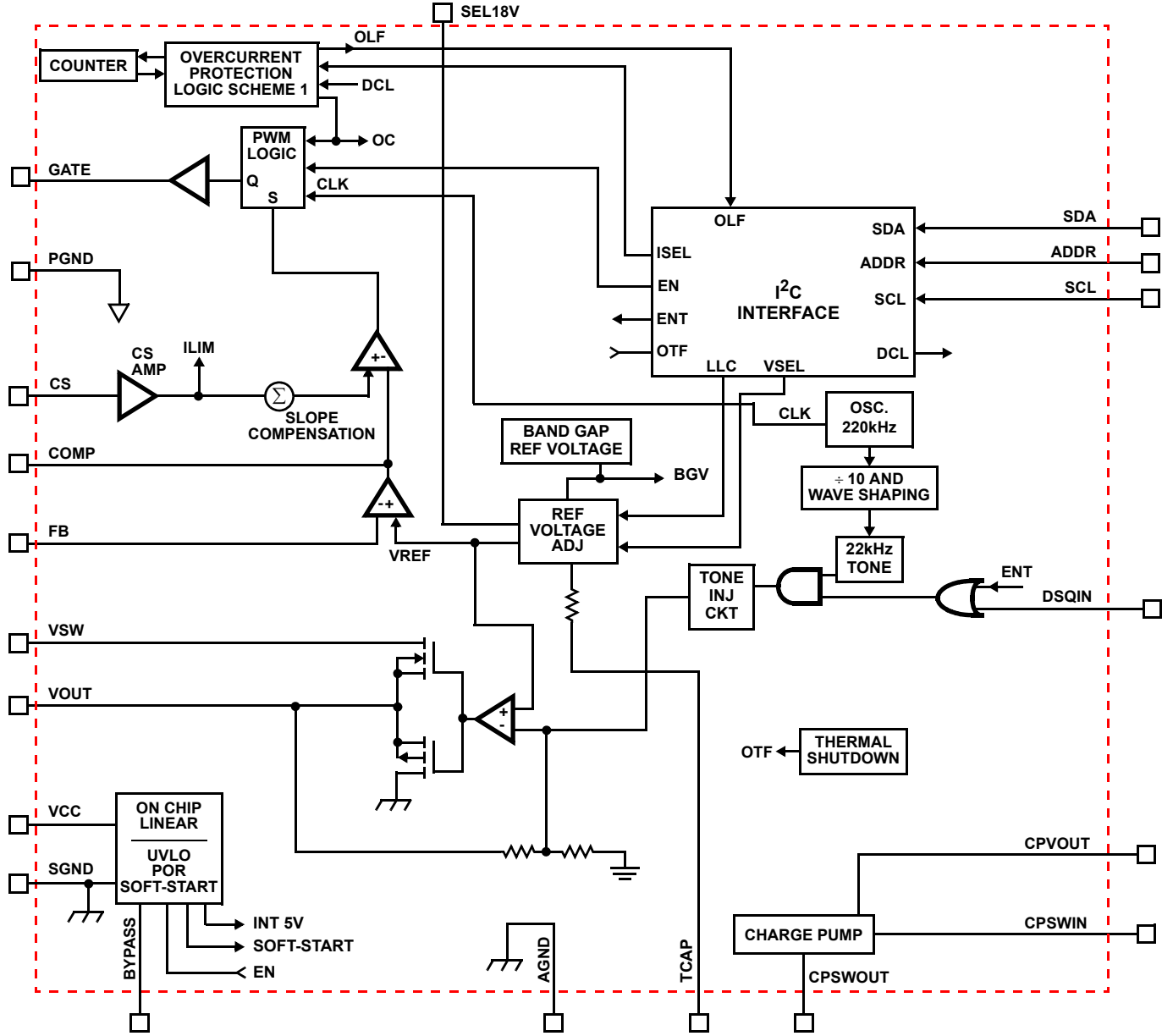
Ordering Information

PART NUMBER*	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6421AER	ISL6421AER	-20 to 85	32 Ld 5x5 QFN	L32.5x5
ISL6421AERZ (Note)	ISL6421AERZ	-20 to 85	32 Ld 5x5 QFN (Pb-free)	L32.5x5

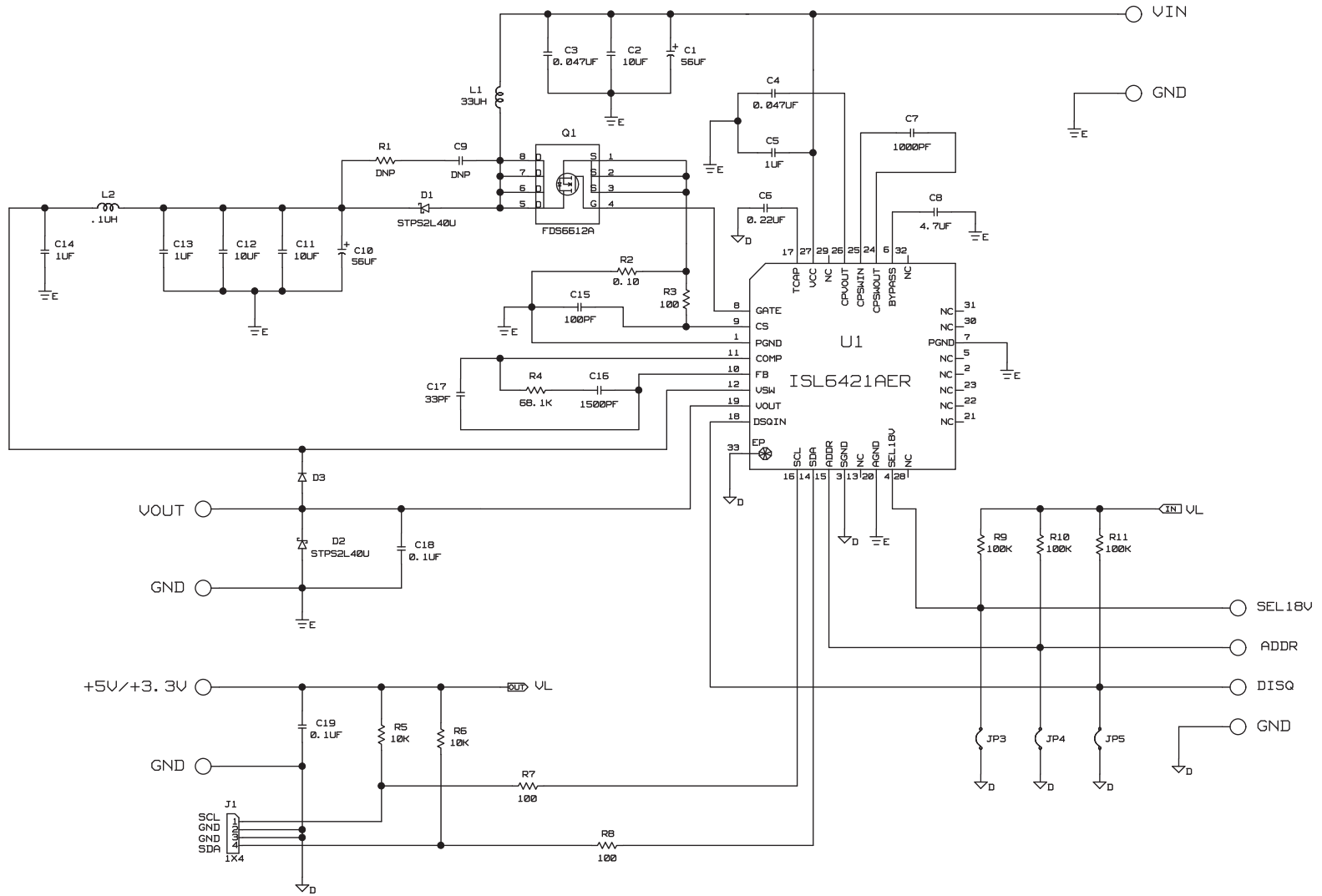
\*Add -T for tape and reel package.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

### Block Diagram



### Typical Application Schematic



NOTE: SGND and PGND to be shorted as close to U1 at layout

**Absolute Maximum Ratings**

Supply Voltage,  $V_{CC}$  ..... 8.0V to 18.0V  
 Logic Input Voltage Range (SDA, SCL, ENT) ..... -0.5V to 7V  
 Output Current ..... Externally/Internally Limited

**Thermal Information**

Thermal Resistance (Notes 1, 2)  $\theta_{JA}$  ( $^{\circ}\text{C}/\text{W}$ )  $\theta_{JC}$  ( $^{\circ}\text{C}/\text{W}$ )  
 QFN Package ..... 35 6  
 Maximum Junction Temperature ..... 150 $^{\circ}\text{C}$   
 Maximum Storage Temperature Range ..... -40 $^{\circ}\text{C}$  to 150 $^{\circ}\text{C}$

For recommended soldering conditions, see Tech Brief TB389.

NOTE: The device junction temperature should be kept below 150 $^{\circ}\text{C}$ . Thermal shut-down circuitry turns off the device if junction temperature exceeds +150 $^{\circ}\text{C}$  typically.

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTES:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

**Electrical Specifications**  $V_{CC} = 12\text{V}$ ,  $T_A = -20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}\text{C}$ . EN = H, LLC = L, ENT = L, DCL = L, DSQIN = L,  $I_{out} = 12\text{mA}$ , unless otherwise noted. See software description section for  $I^2\text{C}$  access to the system.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			8	12	14	V
Standby Supply Current		EN = L	-	1.5	3.0	mA
Supply Current	$I_{IN}$	EN = LLC = VSEL = ENT = H, No Load	-	4.0	8.0	mA
<b>UNDERVOLTAGE LOCKOUT</b>						
Start Threshold			7.5	-	7.95	V
Stop Threshold			7.0	-	7.55	V
Start to Stop Hysteresis			350	400	500	mV
<b>SOFT-START</b>						
COMP Rise Time (Note 3)		(Note 5)	-	1024	-	Cycles
<b>OUTPUT VOLTAGE</b>						
Output Voltage (Note 4)	$V_{OUT}$	VSEL = L, LLC = L	12.74	13.0	13.26	V
	$V_{OUT}$	VSEL = L, LLC = H	13.72	14.0	14.28	V
	$V_{OUT}$	VSEL = H, LLC = L	17.64	18.0	18.36	V
	$V_{OOU}$	VSEL = H, LLC = H	18.62	19.0	19.38	V
Line Regulation	$DV_{OUT}$	$V_{IN} = 8\text{V to }14\text{V}; V_{OUT} = 13\text{V}$	-	4.0	40.0	mV
		$V_{IN} = 8\text{V to }14\text{V}; V_{OUT} = 18\text{V}$	-	4.0	60.0	mV
Load Regulation	$DV_{OUT}$	$I_O = 12\text{mA to }450\text{mA}$	-	50	80	mV
Dynamic Output Current Limiting	$I_{MAX}$	DCL = L	500	-	625	mA
Dynamic Overload Protection Off Time	$T_{OFF}$	DCL = L, Output Shorted (Note 5)	-	900	-	ms
Dynamic Overload Protection On Time	$T_{ON}$		-	20	-	ms
Output Backward Current	$I_{OBK}$	EN = 0; $V_{OBK} = 24\text{V}$	-	2.0	3.0	mA
<b>22kHz TONE</b>						
Tone Frequency	$f_{tone}$	ENT = H	20.0	22.0	24.0	kHz
Tone Amplitude	$V_{tone}$	ENT = H	500	680	900	mV
Tone Duty Cycle	$dC_{tone}$	ENT = H	40	50	60	%
Tone Rise or Fall Time	$T_r, T_f$	ENT = H	5	8	14	$\mu\text{s}$

**Electrical Specifications** VCC = 12V, T<sub>A</sub> = -20°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = 25°C. EN = H, LLC = L, ENT = L, DCL = L, DSQIN = L, I<sub>out</sub> = 12mA, unless otherwise noted. See software description section for I<sup>2</sup>C access to the system. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>LINEAR REGULATOR</b>						
Drop-out Voltage		I <sub>out</sub> = 450mA (Note 5)	-	1.2	-	V
<b>DSQIN PIN</b>						
DSQIN pin logic Low			-	-	1.5V	V
DSQIN pin Logic HIGH			3.5	-	-	V
DSQIN pin Input Current			-	1	-	μA
<b>CURRENT SENSE</b>						
Input Bias Current	I <sub>BIAS</sub>		-	700	-	nA
Overcurrent Threshold		Static current mode, DCL = H	325	400	500	mV
<b>ERROR AMPLIFIER</b>						
Open Loop Voltage Gain	A <sub>OL</sub>	(Note 5)	70	88	-	dB
Gain Bandwidth Product	GBP	(Note 5)	10	-	-	MHz
<b>PWM</b>						
Maximum Duty Cycle			90	93	-	%
Minimum Pulse Width		(Note 5)	-	20	-	ns
<b>OSCILLATOR</b>						
Oscillator Frequency	f <sub>o</sub>	Fixed at (10)(f <sub>tone</sub> )	200	220	240	kHz
<b>THERMAL PROTECTION</b>						
<b>Thermal Shutdown</b>						
Temperature Shutdown Threshold		(Note 5)	-	150	-	°C
Temperature Shutdown Hysteresis		(Note 5)	-	20	-	°C

## NOTES:

- Internal digital soft-start.
- Voltage programming signals VSEL and LLC are implemented via the I<sup>2</sup>C bus.  
IO1 = IO2 = 500mA.
- Guaranteed by design.

**Functional Pin Description**

SYMBOL	FUNCTION
SDA	Bidirectional data from/to I <sup>2</sup> C bus.
SCL	Clock from I <sup>2</sup> C bus.
VSW	Input of the linear post-regulator.
PGND	Dedicated ground for the output gate driver of the PWM.
CS	Current sense input; connect Rsc at this pin for desired overcurrent value for the PWM.
SGND	Small signal ground for the IC.
AGND	Analog ground for the IC.
TCAP	Capacitor for setting rise and fall time of the output of the LNB. Use a capacitor value of 1μF or higher.
BYPASS	Bypass capacitor for internal 5V.
DSQIN	When HIGH this pin enables the internal 22kHz modulation for the LNB, Use this pin for tone enable function for the LNB.

**Functional Pin Description (Continued)**

SYMBOL	FUNCTION
VCC	Main power supply to the chip.
GATE	This is the device output of the PWM. This high current driver output is capable of driving the gate of a power FET. This output is actively held low when Vcc is below the UVLO threshold.
VOUT	Output voltage for the LNB.
ADDRESS	Address pin to select two different addresses per voltage level at this pin.
COMP	Error amp output used for compensation.
FB	Feedback pin for the PWM.
CPVOUT, CPSWIN, CPSWOUT	Charge pump connections.
SEL18V	When connected HIGH, this pin will change the output of the PWM to 18V. Only available on the QFN package option.

**Functional Description**

The ISL6421A is a single output voltage regulator controlled by an I<sup>2</sup>C bus, making it an ideal choice for advanced satellite set-top box and personal video recorder applications. Both supply and control voltage outputs for a low noise block (LNB) are available simultaneously in any output configuration. The device utilizes a built-in DC/DC step-converter which, from a single supply source ranging from 8V to 14V, generates the voltage that enables the linear post-regulator to work with a minimum of dissipated power. An undervoltage lockout circuit disables the circuit when V<sub>CC</sub> drops below a fixed threshold (7.5V typ).

**DiSEqC Encoding**

The internal oscillator is factory-trimmed to provide a tone of 22kHz in accordance with DiSEqC standards. No further adjustment is required. The 22kHz oscillator can be controlled either by the I<sup>2</sup>C interface (ENT bit) or by a dedicated pin (DSQIN) that allows immediate DiSEqC data encoding for the LNB. All the functions of this IC are controlled via the I<sup>2</sup>C bus by writing to the system registers (SR). The same registers can be read back, and two bits will report the diagnostic status. The internal oscillator operates the converters at ten times the tone frequency. The device offers full I<sup>2</sup>C compatible functionality, 3.3V or 5V, and up to 400kHz operation.

If the Tone Enable (ENT) bit is set LOW through I<sup>2</sup>C, then the DSQIN terminal activates the internal tone signal, modulating the dc output with a 0.3V, 22kHz, symmetrical waveform. The presence of this signal usually gives the LNB information about the band to be received.

Burst coding of the 22kHz tone can be accomplished due to the fast response of the DSQIN input and rapid tone response. This allows implementation of the DiSEqC (EUTELSAT) protocols.

When the ENT bit is set HIGH, a continuous 22kHz tone is generated regardless of the DSQIN pin logic status. The

ENT bit must be set LOW when the DSQIN pin is used for DiSEqC encoding.

**Linear Regulator**

The output linear regulator will sink and source current. This feature allows full modulation capability into capacitive loads as high as 0.25μF. In order to minimize the power dissipation, the output voltage of the internal step-up converter is adjusted to allow the linear regulator to work at minimum dropout.

When the device is put in the shutdown mode (EN = LOW), the PWM power block is disabled. When the regulator block is active (EN = HIGH), the output can be logic controlled to be 13V or 18V (typical) by means of the VSEL bit (Voltage Select) for remote controlling of non-DiSEqC LNBs. Additionally, it is possible to increment by 1V (typical) the selected voltage value to compensate for the excess voltage drop along the coaxial cable (LLC bit HIGH).

**Output Timing**

The programmed output voltage rise and fall times can be set by an external capacitor. The output rise and fall times will be approximately 3400 times the TCAP value. For the recommended range of 0.47μF to 2.2μF, the rise and fall time would be 1.6ms to 7.6ms. Using a 0.47μF capacitor insures the PWM stays below its overcurrent threshold when charging a 120μF VSW filter cap during the worst case 13V to 19V transition. A typical value of 1.0μF is recommended. This feature affects the programmed voltage rise and fall times.

**Current Limiting**

The current limiting block can operate either statically (simple current clamp) or dynamically. The threshold is between 500mA and 625mA. When the DCL (Dynamic Current Limiting) bit is set to LOW, the overcurrent protection circuit works dynamically. That is, as soon as an overload is detected, the output is shut down for a time T<sub>OFF</sub>, typically

900ms. Simultaneously the overload flag (OLF) bit of the system register is set to HIGH. After this time has elapsed, the output is resumed for a time  $T_{ON} = 20\text{ms}$ . During  $T_{ON}$ , the device output will be current limited to between 500mA and 625mA. At the end of  $T_{ON}$ , if the overload is still detected, the protection circuit will cycle again through  $T_{OFF}$  and  $T_{ON}$ . At the end of a full  $T_{ON}$ , during which no overload is detected, normal operation is resumed and the OLF bit is reset to LOW. Typical  $T_{ON} + T_{OFF}$  time is 920ms as determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in a short circuit condition, still ensuring excellent power-on start-up in most conditions.

However, there could be some cases in which a highly capacitive load on the output may cause a difficult start-up, when the dynamic protection is chosen. This can be solved by initiating a power start-up in static mode (DCL = HIGH) and then switching to the dynamic mode (DCL = LOW) after a chosen amount of time. When in static mode, the OLF bit goes HIGH when the current clamp limit is reached and returns LOW when the overload condition is cleared. The OLF bit will be LOW at the end of initial power-on soft-start.

The static mode limit serves only to limit the peak current through the switching FET and cannot precisely set an average current limit. The sense resistor is calculated by the equation

$$R_{SC} = \frac{0.4}{I_{PK}}$$

where  $I_{PK}$  is the peak current through the FET. This value should be greater than the normal operating peak current.

**Thermal Resistance**

This IC is protected against overheating. When the junction temperature exceeds 150°C (typical), the step-up converter and the linear regulator are shut off and the overtemp flag (OTF) bit of the SR is set HIGH. Normal operation is resumed and the OTF bit is reset LOW, when the junction is cooled down to 130°C (typical).

**External Output Voltage Selection**

The output voltage can be selected by the I<sup>2</sup>C bus. Additionally, the QFN package offers a pin (SEL18V) for independent 13V/18V output voltage selection. When using this pin, the I<sup>2</sup>C bits should be initialized to 13V status.

TABLE 1.

I <sup>2</sup> C BITS	SEL18V	O/P VOLTAGE
13V	Low	13V
13V	High	18V

**I<sup>2</sup>C Bus Interface for ISL6421A**

(Refer to Philips I<sup>2</sup>C Specification, Rev. 2.1)

Data transmission from the main microprocessor to the ISL6421A and vice versa takes place through the 2 wires I<sup>2</sup>C bus interfaces, which consists of the two lines SDA and SCL. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor. (Pull up resistors to positive supply voltage must be externally connected). When the bus is free, both lines are HIGH. The output stage of ISL6421A will have an open drain/open collector in order to perform the wired-AND function. Data on the I<sup>2</sup>C bus can be transferred up to 100kbts/s in the standard-mode or up to 400kbts/s in the fast-mode. The level of logic “0” and logic “1” is dependent of associated value of V<sub>dd</sub> as per electrical specification table. One clock pulse is generated for each data bit transferred.

**Data Validity**

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 1.

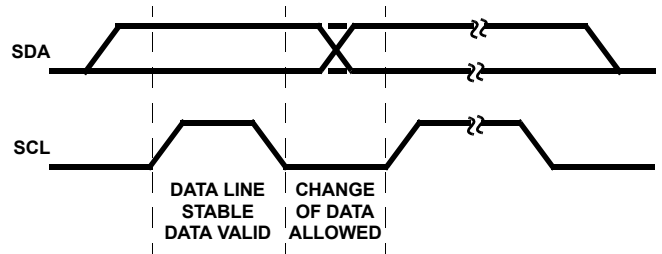


FIGURE 1. DATA VALIDITY

**START and STOP Conditions**

As shown in the Figure 2, START condition is a HIGH to LOW transition of the SDA line, while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line, while SCL is HIGH. A STOP condition must be sent before each START condition.

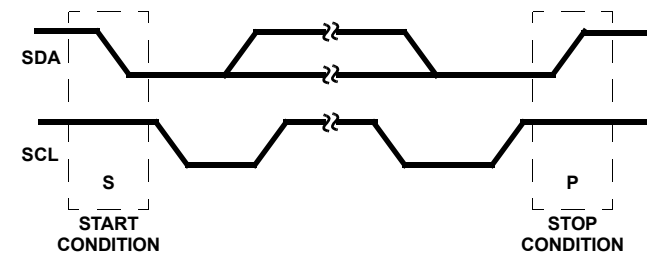


FIGURE 2. START AND STOP WAVEFORMS

**Byte Format**

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

**Acknowledge**

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (Figure 3). The peripheral that acknowledges has to pull the SDA line down (LOW) during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. (Of course, set-up and hold times must also be taken into account.)

The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case, the master transmitter can generate the STOP information in order to abort the transfer. The ISL6421A will not generate the acknowledge if the POWER OK signal from the UVLO is LOW.

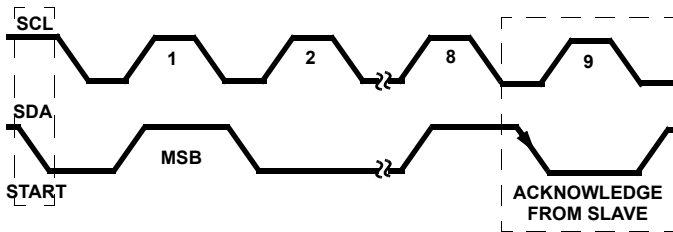


FIGURE 3. ACKNOWLEDGE ON THE I<sup>2</sup>C BUS

**Transmission Without Acknowledge**

Avoiding detection of the acknowledgement, the microprocessor can use a simpler transmission; it waits one clock without checking the slave acknowledging, and sends the new data.

This approach, though, is less protected from error and decreases the noise immunity.

**ISL6421A Software Description**

**Interface Protocol**

The interface protocol is comprised of the following, as shown below in Table 2:

- A start condition (S)
- A chip address byte (MSB on left; the LSB bit determines read (1) or write (0) transmission) (the assigned I<sup>2</sup>C slave address for the ISL6421A is 0001 00XX)
- A sequence of data (1 byte + Acknowledge)
- A stop condition (P)

TABLE 2. INTERFACE PROTOCOL

S	0	0	0	1	0	0	0	R/W	ACK	Data (8 bits)	ACK	P
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TABLE 3. SYSTEM REGISTER 1 (SR1)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R
SR1	DCL	X	ENT	LLC	VSEL	EN	OLF

TABLE 4. SYSTEM REGISTER 2 (SR2)

R, W	R, W	R, W	R, W	R, W	R, W	R	R
SR2	X	X	X	X	X	OTF	X

**System Register Format**

- R, W = Read and Write bit
- R = Read-only bit

All bits reset to 0 at Power-On

**Transmitted Data (I<sup>2</sup>C bus WRITE mode)**

When the R/W bit in the chip is set to 0, the main microprocessor can write on the system registers (SR1/SR2) of the ISL6421A via I<sup>2</sup>C bus. These will be written by the microprocessor as shown below. The spare bits of SR1/SR2 can be used for other functions.

TABLE 5. SYSTEM REGISTER (SR1 AND SR2) CONFIGURATION

SR	DCL	-	ENT	LLC	VSEL	EN	OLF	FUNCTION
0		X		0	0	1		SR1 is selected
0		X		0	0	1		Vout1 = 13V, Vboost1 = 13V + Vdrop
0		X		0	1	1		Vout1 = 18V, Vboost1 = 18V + Vdrop
0		X		1	0	1		Vout1 = 14V, Vboost1 = 14V + Vdrop
0		X		1	1	1		Vout1 = 19V, Vboost1 = 19V + Vdrop
0		X	0			1		22kHz tone is controlled by the DSQIN pin input
0		X	1			1		22kHz tone is ON, DSQIN pin input is disabled
0	1	X				1		Dynamic current limit NOT selected
0	0	X				1		Dynamic current limit selected
0	X	X	X	X	X	0		PWM and Linear for channel 1 disabled

SR	-	-	-	-	-	OTF	-	FUNCTION
1	X	X	X	X	X	X	X	SR2 is selected; to read OTF flag.



**Received Data (I<sup>2</sup>C Bus Read Mode)**

The ISL6421A can provide to the master a copy of the System Register information via the I<sup>2</sup>C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following Master generated clock bits, the ISL6421A issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

- Acknowledge the reception, starting in this way the transmission of another byte from the ISL6421A.
- Not acknowledge, stopping the read mode communication.

While the whole register is read back by the microprocessor, only the two read-only bits, OLF and OTF, convey diagnostic information about the ISL6421A.

**TABLE 6. READING SYSTEM REGISTERS**

DCL	ISEL	ENT	LLC	VSEL	EN	OTF	OLF	FUNCTION
These bits are read as they were after the last write operation.						0		T <sub>j</sub> ≤ 130°C, Normal operation
						1		T <sub>j</sub> > 150°C, Power blocks disabled
							0	I <sub>out</sub> < I <sub>max</sub> , Normal operation
							1	I <sub>out</sub> > I <sub>max</sub> , Overload protection triggered

**I<sup>2</sup>C Electrical Specifications****TABLE 8. I<sup>2</sup>C SPECIFICATIONS**

PARAMETER	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Input Logic High, V <sub>IH</sub>	SDA, SCL		0.7 × V <sub>DD</sub>	
Input Logic Low, V <sub>IL</sub>	SDA, SCL		0.3 × V <sub>DD</sub>	
Input Logic Current, I <sub>IL</sub>	SDA, SCL; 0.4V < V <sub>in</sub> < 4.5V			10μA
SCL Clock Frequency		0	100kHz	400kHz

NOTE: V<sub>DD</sub> = 5.0V/3.3V.

**Power-On I<sup>2</sup>C Interface Reset**

The I<sup>2</sup>C interface built into the ISL6421A is automatically reset at power-on. The I<sup>2</sup>C interface block will receive a Power OK logic signal from the UVLO circuit. This signal will go HIGH when chip power is OK. As long as this signal is LOW, the interface will not respond to any I<sup>2</sup>C commands and the system register SR is initialized to all zeros, thus keeping the power blocks disabled.

Once V<sub>cc</sub> rises above the UVLO level, the POWER OK signal given to the I<sup>2</sup>C interface block will be HIGH, the I<sup>2</sup>C interface becomes operative and the SR can be configured by the main microprocessor. About 400mV of hysteresis is provided in the UVLO threshold to avoid false triggering of the Power-On reset circuit.

(I<sup>2</sup>C comes up with EN = 0, EN goes HIGH at the same time as (or later than) all other I<sup>2</sup>C data for the PWM becomes valid).

**ADDRESS Pin**

Connecting this pin to GND forces the chip I<sup>2</sup>C interface address to 0001000; applying a voltage >2.7V forces the address to 0001001, as shown below.

**TABLE 7. ADDRESS PIN CHARACTERISTICS**

V <sub>addr</sub>	MIN	TYP	MAX
V <sub>addr-1</sub> "0001000"	0V	-	2.0V
V <sub>addr-2</sub> "0001001"	2.7V	-	5.0V

**Typical Performance Curves**

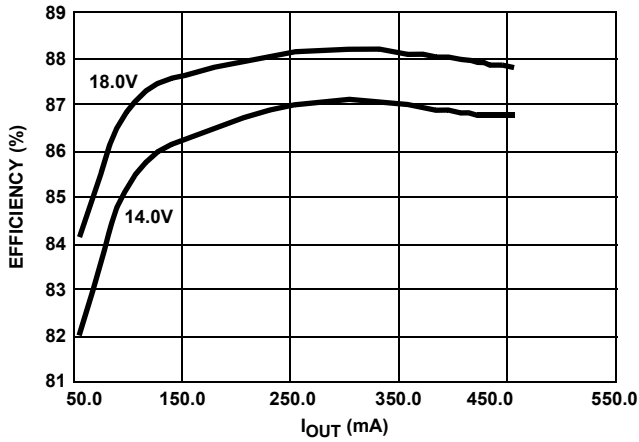


FIGURE 4. EFFICIENCY vs LOAD CURRENT

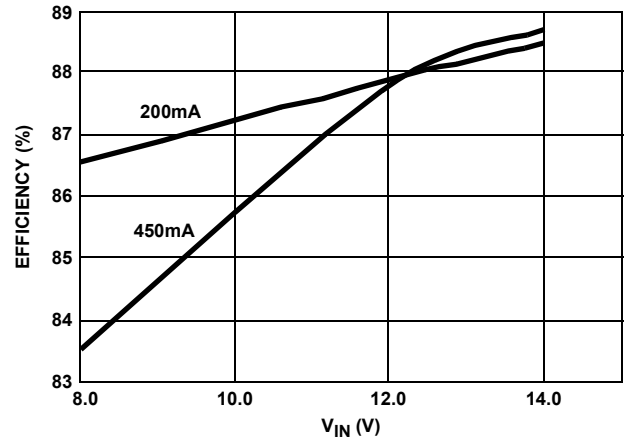


FIGURE 5. EFFICIENCY vs VIN

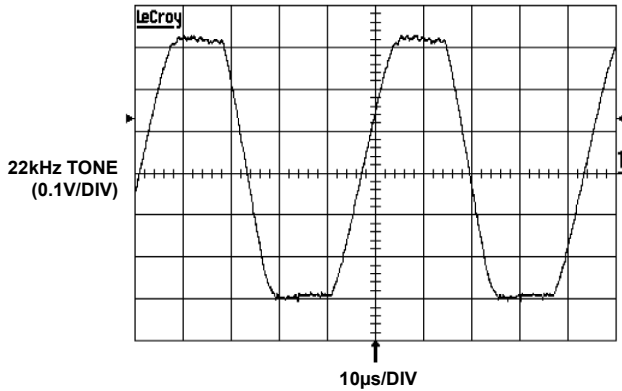


FIGURE 6. 22kHz TONE

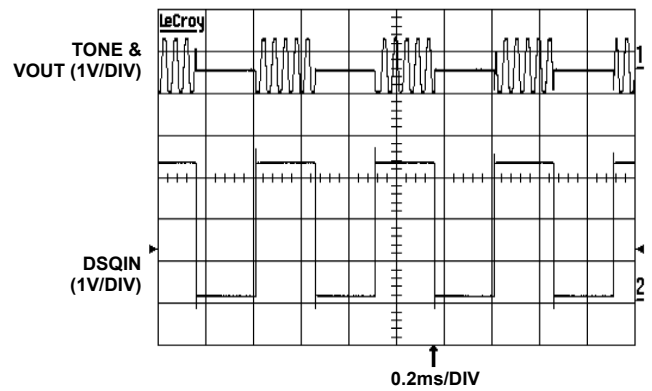


FIGURE 7. 22kHz TONE MODULATED BY DSQIN

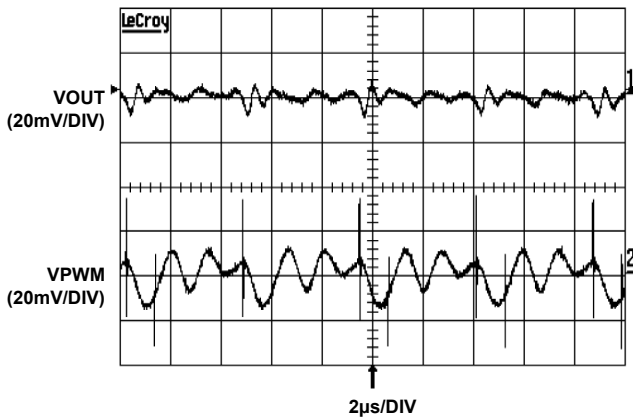


FIGURE 8. RIPPLE VOUT = 14.0V

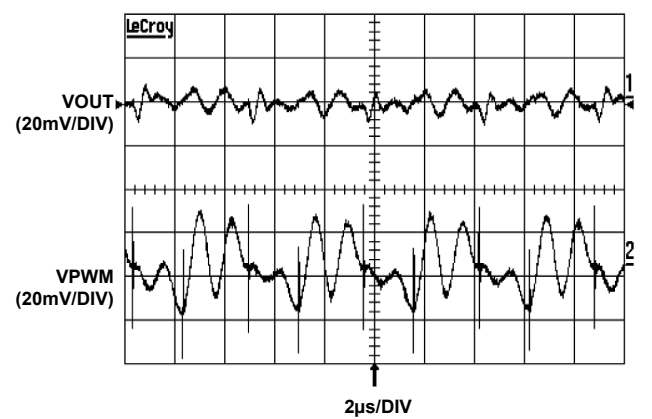


FIGURE 9. RIPPLE VOUT = 18.0V

**Typical Performance Curves** (Continued)

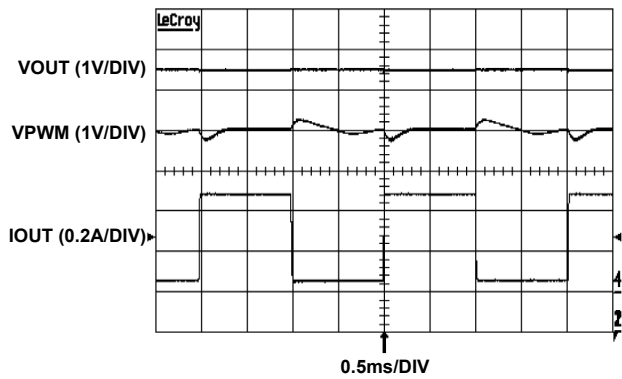


FIGURE 10. DYNAMIC RESPONSE VOUT = 19.0V

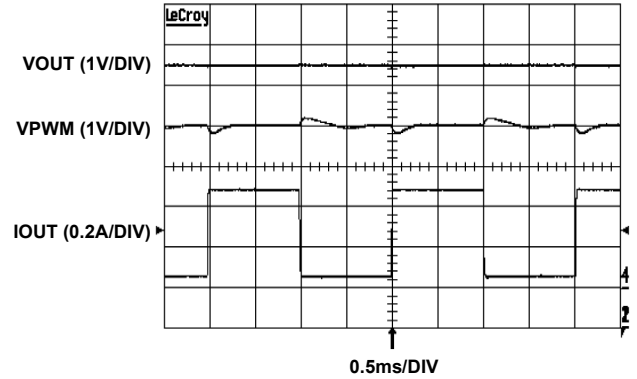


FIGURE 11. DYNAMIC RESPONSE VOUT = 14.0V

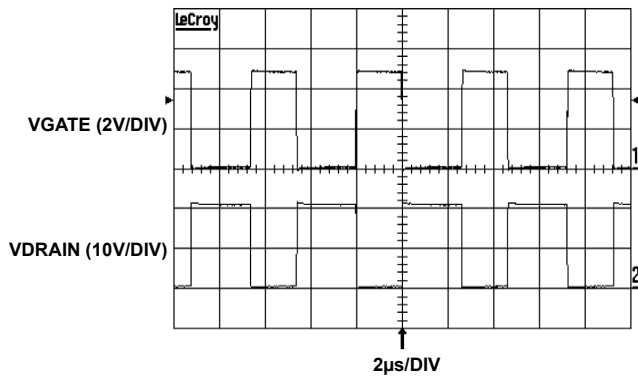


FIGURE 12. GATE AND DRAIN WAVEFORMS VOUT = 19.0V

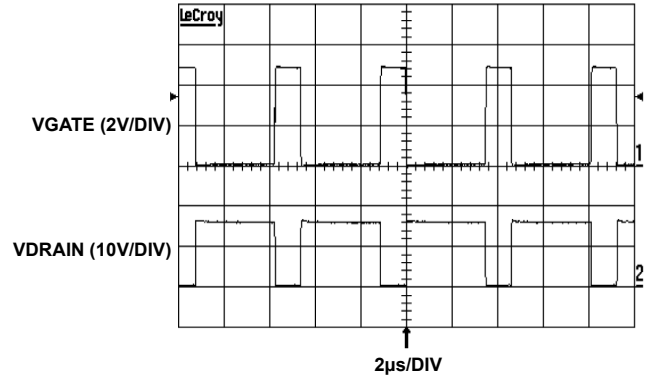


FIGURE 13. GATE AND DRAIN WAVEFORMS VOUT = 14.0V

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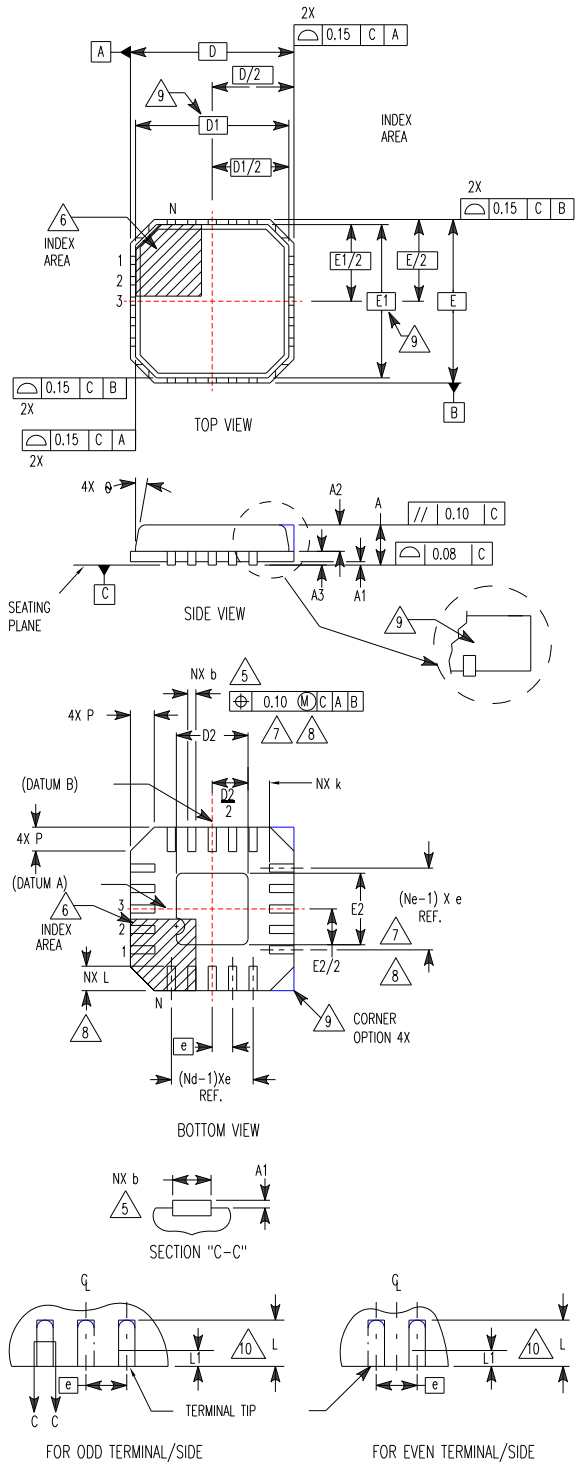
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**Quad Flat No-Lead Plastic Package (QFN)  
Micro Lead Frame Plastic Package (MLFP)**



**L32.5x5**

**32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE  
(COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C**

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5,8
D	5.00 BSC			-
D1	4.75 BSC			9
D2	2.95	3.10	3.25	7,8
E	5.00 BSC			-
E1	4.75 BSC			9
E2	2.95	3.10	3.25	7,8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N	32			2
Nd	8			3
Ne	8	8	-	3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

**NOTES:**

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.