ISL6267

Multiphase PWM Regulator for AMD Fusion™ Mobile CPUs

FN7801
Rev 1.00
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The ISL6267 is designed to be completely compliant with AMD Fusion™ specifications. The ISL6267 controls two Voltage Regulators (VRs), with three integrated gate drivers. The first VR can be configured as 3-, 2-, or 1-phase VR, while the second output can be configured as 2- or 1-phase VR, providing maximum flexibility. The two VRs share the serial control bus to communicate with the CPU and achieve lower cost and smaller board area compared with two-chip solutions.

The PWM modulator of the ISL6267 is based on Intersil's R3 (Robust Ripple Regulator) Technology™. Compared with the traditional multi-phase buck regulator, the R3 modulator commands variable switching frequency during load transients, achieving faster transient response. With the same modulator, it naturally goes into pulse frequency modulation in light load conditions, which achieves higher light load efficiency and extends battery life.

The ISL6267 has several other key features. Both outputs support DCR current sensing with a single NTC thermostat for DCR temperature compensation or accurate resistor current sensing. Both of the outputs utilize remote voltage sense, adjustable switching frequency, current monitor, OC protection, independent power-good indicators, temperature monitors, and a common thermal alert.

Applications

- AMD fusion CPU/GPU core power
- Notebook computer

Features

- Supports AMD SVI 1.0 serial data bus interface
- Dual output controller with integrated drivers
  - Core VR configurable 3-, 2-, 1-phase with two integrated drivers
  - Northbridge VR configurable 2- or 1-phase with one integrated driver
- Precision voltage regulation
  - 0.5% system accuracy over-temperature
  - 0V to 1.55V in 12.5mV steps
  - Enhanced load line accuracy
- Supports multiple current sensing methods
  - Lossless inductor DCR current sensing
  - Precision resistor current sensing
- Programmable 1-, 2- or 3-phase for the core output and 1- or 2-phase for the northbridge output
- Adaptive body diode conduction time reduction
- Superior noise immunity and transient response
- Output current monitor and thermal monitor
- Differential remote voltage sensing
- High efficiency across entire load range
- Programmable +VID offset for both core and NB
- Programmable switching frequency for both outputs
- Excellent dynamic current balance between phases
- OCP/WOC, OVP, PGOOD, and thermal monitor
- Small footprint 48 Ld 6x6 QFN package
- Pb-free (RoHS compliant)

Core Performance on ISL6267EVAL1Z

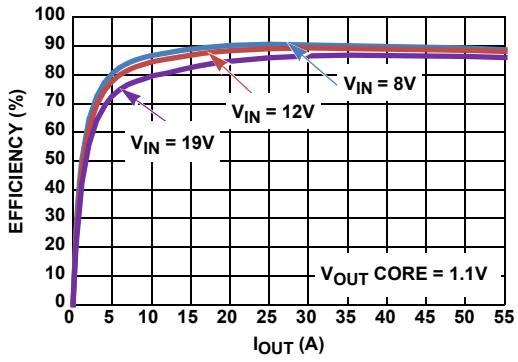


FIGURE 1. EFFICIENCY vs LOAD

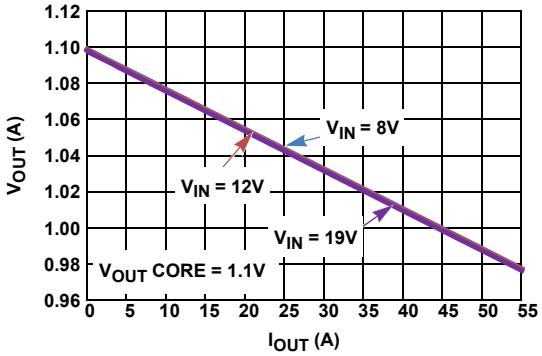


FIGURE 2. V_{OUT} vs LOAD

Simplified Application Circuit For High Power CPU Core

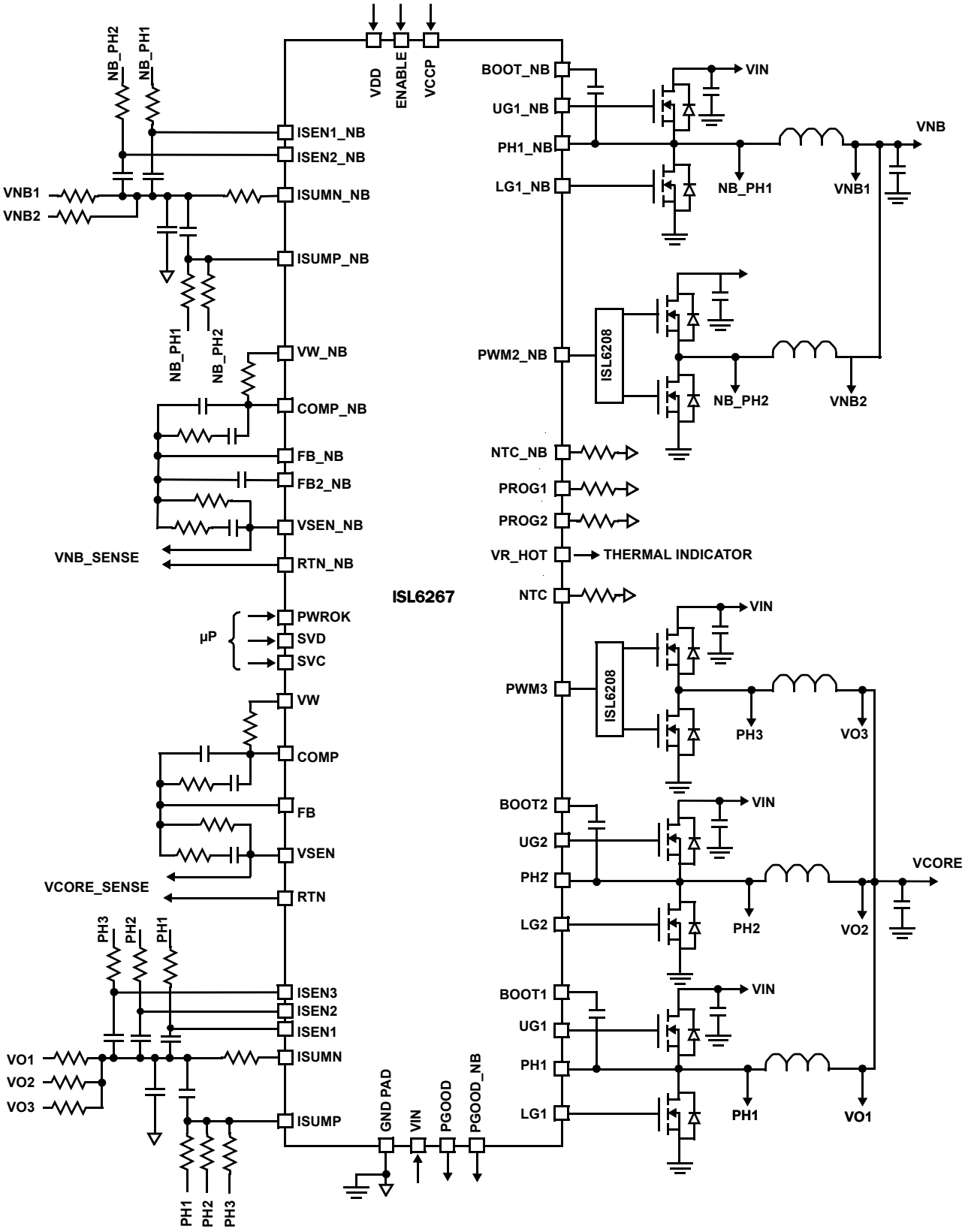


FIGURE 3. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit For AMD Torpedo Platform

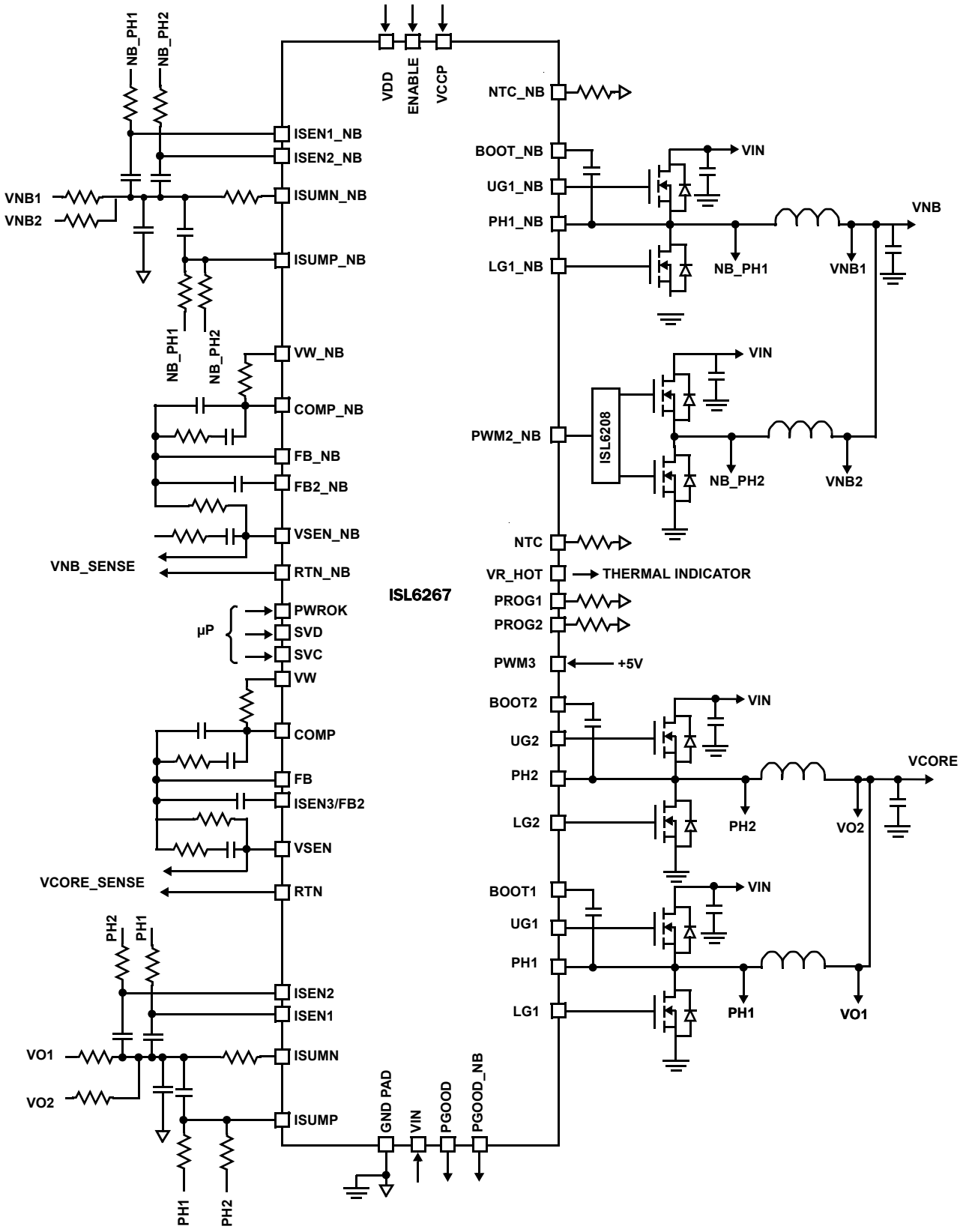


FIGURE 4. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit For Low Power CPU Core And NB

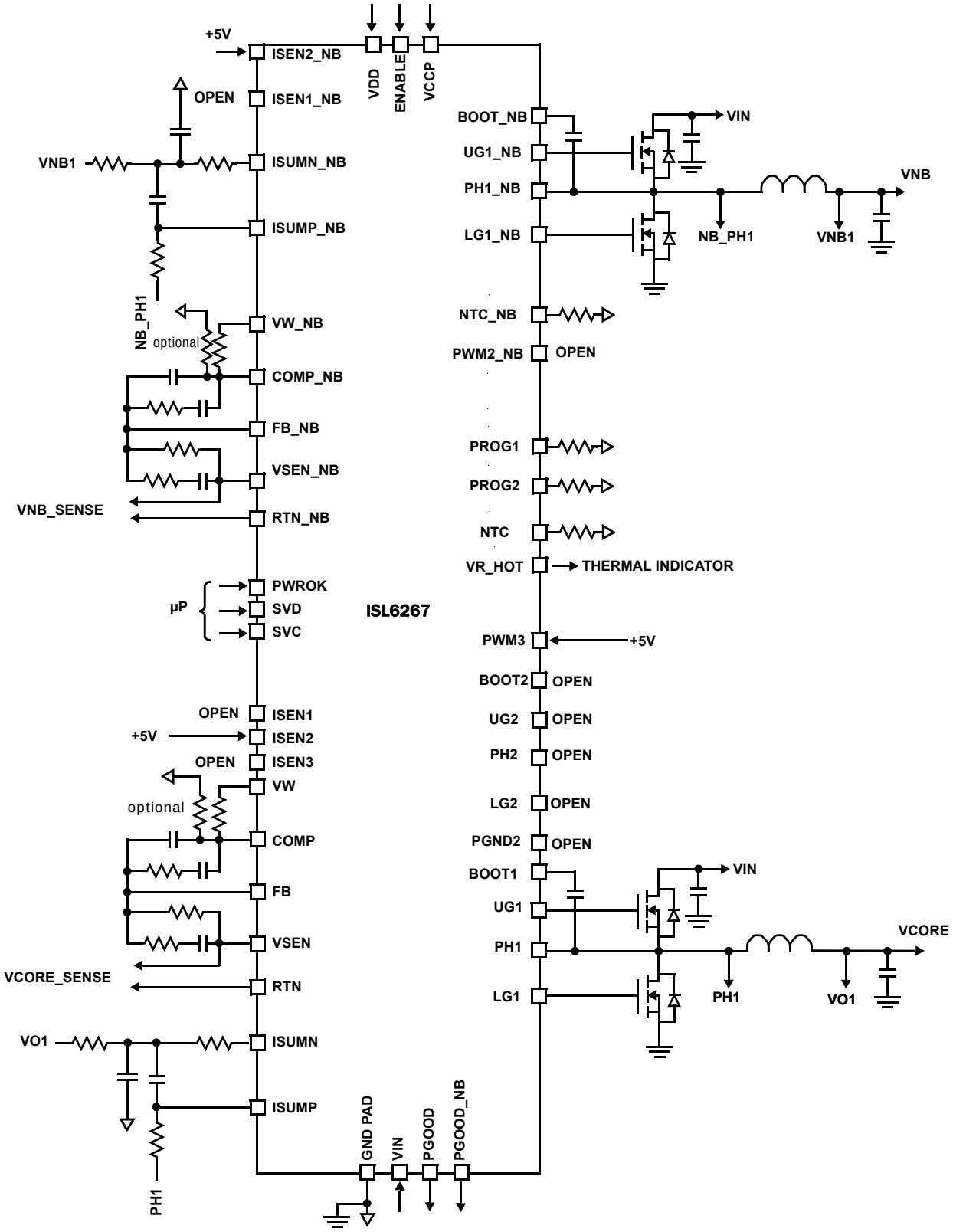


FIGURE 5. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit Showing Resistor Sensing

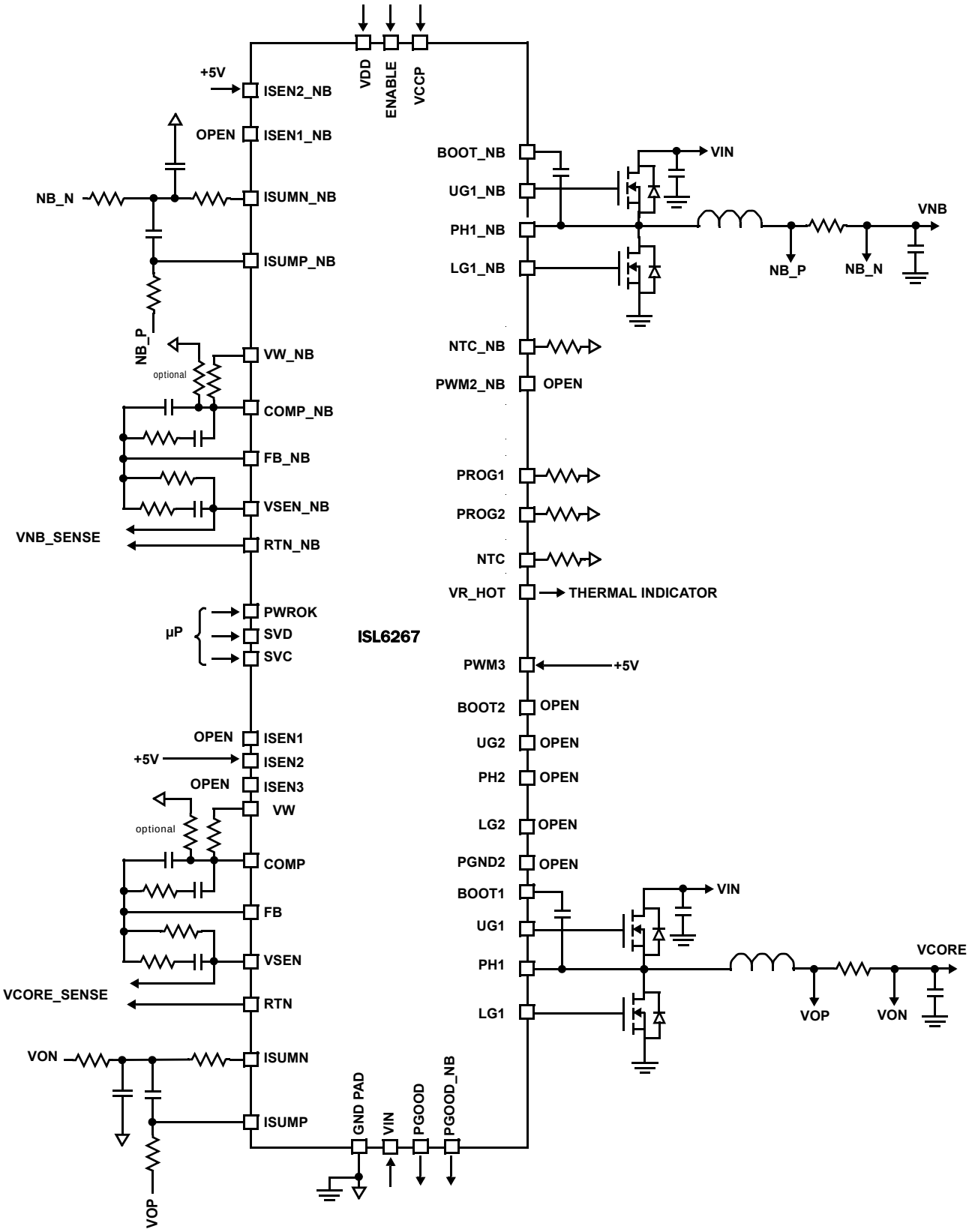
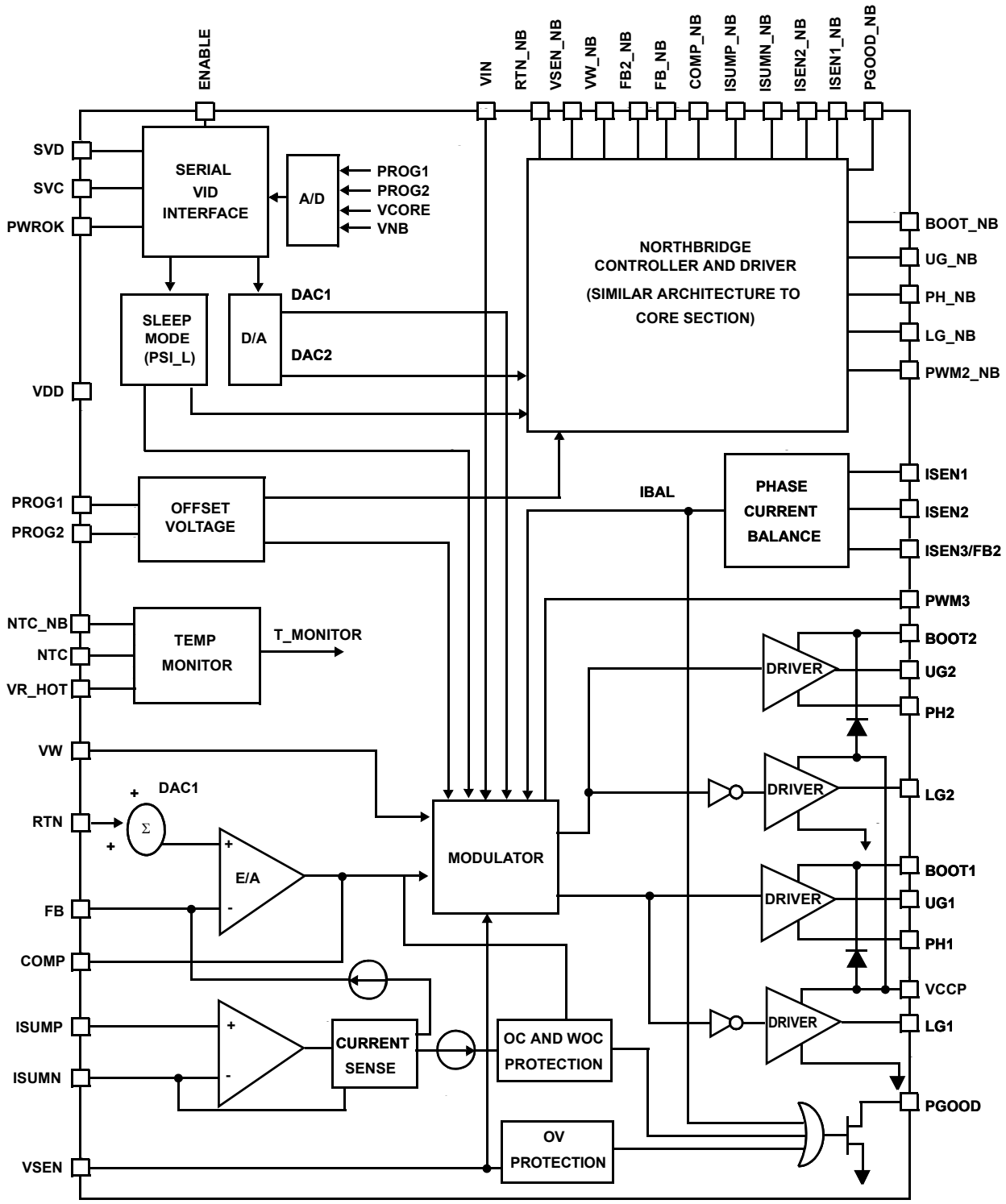
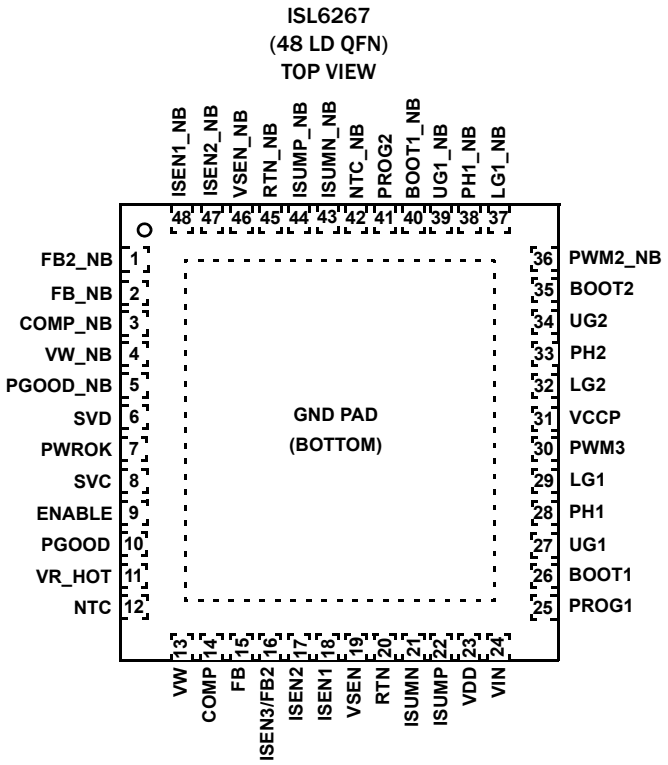


FIGURE 6. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Block Diagram



Pin Configuration



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	FB2_NB	The components connecting to FB2_NB are used to adjust the compensation in 1-phase mode to achieve optimum performance.
2	FB_NB	Output voltage feedback to the inverting input of the Northbridge controller error amplifier.
3	COMP_NB	Northbridge VR error amplifier output.
4	VW_NB	Window voltage set pin used to set the switching frequency for the Northbridge controller. A resistor from this pin to COMP_NB programs the switching frequency (8kΩ gives approximately 300kHz).
5	PGOOD_NB	Open-drain output to indicate the Northbridge portion of the IC is ready to supply regulated voltage. Pull-up externally to VCCP or 3.3V.
6	SVD	Serial VID data bi-directional signal from the CPU processor master device to the VR.
7	PWROK	System power good input. When this pin is high, the SVI interface is active and the I^2C protocol is running. While this pin is low, the SVC and SVD input states determine the pre-PWROK metal VID. This pin must be low prior to the ISL6267 PGOOD output going high per the AMD SVI Controller Guidelines.
8	SVC	Serial VID clock input from the CPU processor master device.
9	ENABLE	Enable input. A high level logic on this pin enables both VRs.
10	PGOOD	Open-drain output to indicate the Core portion of the IC is ready to supply regulated voltage. Pull-up externally to VCCP or 3.3V.
11	VR_HOT	Thermal overload open drain output indicator active LOW.
12	NTC	Thermistor input to VR_HOT circuit to monitor Core VR temperature.
13	VW	Window voltage set pin used to set the switching frequency for the Core controller. A resistor from this pin to COMP programs the switching frequency (8kΩ gives approximately 300kHz).
14	COMP	Error amplifier output.
15	FB	Output voltage feedback to the inverting input of the Core controller error amplifier.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
16	ISEN3/FB2	When the Core VR of ISL6267 is configured in 3-phase mode, this pin is ISEN3. ISEN3 is the individual current sensing for Channel 3. When the Core VR of ISL6267 is configured in 2-phase mode, this pin is FB2. There is a switch between the FB2 pin and the FB pin. The switch is on in 2-phase mode and is off in 1-phase mode. The components connecting to FB2 are used to adjust the compensation in 1-phase mode to achieve optimum performance.
17	ISEN2	Individual current sensing for Channel 2 of the Core VR. When ISEN2 is pulled to 5V VDD, the controller disables Channel 2, and the Core VR runs in single-phase mode.
18	ISEN1	Individual current sensing for Channel 1 of the Core output.
19	VSEN	Output voltage sense pin for the Core controller. Connect to the +sense pin of the microprocessor die.
20	RTN	Output voltage sense return pin for the Core controller. Connect to the -sense pin of the microprocessor die.
21	ISUMN	Inverting input of the transconductance amplifier for current monitor and load line of Core output.
22	ISUMP	Non-inverting input of the transconductance amplifier for current monitor and load line of Core output.
23	VDD	5V bias power.
24	VIN	Battery supply voltage, used for feed-forward.
25	PROG1	Program pin for setting output voltage offset for Core VR.
26	BOOT1	Connect an MLCC capacitor across the BOOT1 and the phase (PH1) pin. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT1 pin, each time the PH1 pin drops below VCCP minus the voltage dropped across the internal boot diode.
27	UG1	Output of the Phase 1 high-side MOSFET gate driver of the Core VR. Connect the UG1 pin to the gate of the Phase 1 high-side MOSFET.
28	PH1	Current return path for the Phase 1 high-side MOSFET gate driver of VR1. Connect the PH1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 1.
29	LG1	Output of the Phase 1 low-side MOSFET gate driver of the Core VR. Connect the LG1 pin to the gate of the Phase 1 low-side MOSFET.
30	PWM3	PWM output for Channel 3 of the Core VR. When PWM3 is pulled to 5V VDD, the controller disables Phase 3 and runs in 2-phase mode.
31	VCCP	Input voltage bias for the internal gate drivers. Connect +5V to the VCCP pin. Decouple with at least 1µF of capacitance to GND. A high quality, X7R dielectric MLCC capacitor is recommended.
32	LG2	Output of the Phase 2 low-side MOSFET gate driver of VR1. Connect the LG2 pin to the gate of the Phase 2 low-side MOSFET.
33	PH2	Current return path for the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the PH2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 2.
34	UG2	Output of the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the UG2 pin to the gate of the Phase 2 high-side MOSFET.
35	BOOT2	Connect an MLCC capacitor across the BOOT2 and PH2 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT2 pin, each time the PH2 pin drops below VCCP minus the voltage dropped across the internal boot diode.
36	PWM2_NB	PWM output for Channel 2 of the Northbridge VR.
37	LG1_NB	Output of the low-side MOSFET gate driver of the Northbridge VR. Connect the LG1_NB pin to the gate of the low-side MOSFET of VR2.
38	PH1_NB	Current return path for the high-side MOSFET gate driver of the Northbridge VR. Connect the PH1_NB pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of the Northbridge VR.
39	UG1_NB	Output of the high-side MOSFET gate driver of the Northbridge VR. Connect the UG1_NB pin to the gate of the high-side MOSFET.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
40	BOOT1_NB	Connect an MLCC capacitor across the BOOT1_NB and the PH1_NB pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT1_NB pin, each time the PH1_NB pin drops below VCCP minus the voltage dropped across the internal boot diode.
41	PROG2	Program pin for setting output voltage offset for Northbridge VR.
42	NTC_NB	Thermistor input to VR_HOT circuit to monitor Northbridge VR temperature.
43	ISUMN_NB	Inverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
44	ISUMP_NB	Non-inverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
45	RTN_NB	Output voltage sense return pin for the Northbridge controller. Connect to the -sense pin of the microprocessor die.
46	VSEN_NB	Output voltage sense pin for the Northbridge controller. Connect to the +sense pin of the microprocessor die.
47	ISEN2_NB	Individual current sensing for Channel 2 of the Northbridge VR. When ISEN2 is pulled to 5V VDD, the controller will disable Channel 2 and the Northbridge VR will run single-phase.
48	ISEN1_NB	Individual current sensing for Channel 1 of the Northbridge VR.
	GND (Bottom Pad)	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6267HRZ	ISL6267 HRZ	-10 to +100	48 Ld 6x6 QFN	L48.6x6B
ISL6267IRZ	ISL6267 IRZ	-40 to +100	48 Ld 6x6 QFN	L48.6x6B
ISL6267EVAL1Z	Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6267. For more information on MSL please see tech brief TB363.

Table of Contents

Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.3V to +7V
Battery Voltage, V_{IN} . . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE) . . . . . -0.3V to +7V(DC)
. . . . . -0.3V to +9V(<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE - 0.3V (DC) to BOOTPHASE - 5V
. . . . . (<20ns Pulse Width, 10µJ) to BOOT LGATE Voltage
. . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
All Other Pins . . . . . -0.3V to (VDD + 0.3V)
Open Drain Outputs, PGOOD, VR_HOT . . . . . -0.3V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN Package (Notes 4, 5)	28	1

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . +5V ±5%
Battery Voltage, V_{IN} . . . . . 4.5V to 25V
Ambient Temperature
HRZ . . . . . -10°C to +100°C
IRZ . . . . . -40°C to +100°C
Junction Temperature
HRZ . . . . . -10°C to +125°C
IRZ . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	ENABLE = 1V		9	**10.5**	mA
		ENABLE = 0V			**1**	µA
Battery Supply Current	I_{VIN}	ENABLE = 0V			**1**	µA
V_{IN} Input Resistance	R_{VIN}	ENABLE = 1V		550		kΩ
POWER-ON-RESET THRESHOLDS						
VDD POR Threshold	VDD_POR_r	V_{DD} rising		4.35	**4.5**	V
	VDD_POR_f	V_{DD} falling	**4.00**	4.15		V
VIN POR Threshold	VIN_POR_r	V_{IN} rising		4.00	**4.35**	V
	VIN_POR_f	V_{IN} falling	**2.8**	3.30		V
SYSTEM AND REFERENCES						
System Accuracy	HRZ% Error (V_{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.55V	-0.5		+0.5	%
		VID = 0.50V to 0.7375V	-8		+8	mV
		VID = 0.25V to 0.4875V	-15		+15	mV
	IRZ% Error (V_{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.55V	-0.8		+0.8	%
		VID = 0.50V to 0.7375V	-10		+10	mV
		VID = 0.25V to 0.4875V	-18		+18	mV
Maximum Output Voltage	$V_{CC\_CORE(max)}$	VID = [0000000]		1.55		V
Minimum Output Voltage	$V_{CC\_CORE(min)}$	VID = [1111111]		0.0		V

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CHANNEL FREQUENCY						
Nominal Channel Frequency	HRZ, $f_{SW(nom)}$		280	300	320	kHz
	IRZ, $f_{SW(nom)}$		275	300	325	kHz
Adjustment Range			**200**		**500**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset		I_{FB} = 0A	**-0.15**		**+0.15**	mV
Error Amp DC Gain	A_{v0}			90		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		18		MHz
ISEN						
Imbalance Voltage		Maximum of ISENs - Minimum of ISENs			**1**	mV
Input Bias Current				20		nA
POWER-GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.26	**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	**-1**		**1**	µA
PGOOD Delay	t_{PGD}			460		µs
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA Source Current		1.0	**1.5**	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance	R_{UGPD}	250mA Sink Current		1.0	**1.5**	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA Source Current		1.0	**1.5**	Ω
LGATE Source Current	I_{LGSRC}	LGATE - VSSP = 2.5V		2.0		A
LGATE Sink Resistance	R_{LGPD}	250mA Sink Current		0.5	**0.9**	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - VSSP = 2.5V		4.0		A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load		23		ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load		28		ns
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 2mA		0.58		V
Reverse Leakage	I_R	V_R = 25V		0.2		µA
PROTECTION						
Overvoltage Threshold	OV_H	VSEN rising above setpoint for > 1ms	**200**	270	**330**	mV
Severe Overvoltage Threshold	OV_{HS}	V_O rising above threshold > 0.5 µs		1.800		V
Undervoltage Threshold	OV_H	VSEN falls below setpoint for > 1ms	**260**	330	**400**	mV
Current Imbalance Threshold		One ISEN above another ISEN for > 1.2ms		9		mV
Core OCP Current Threshold	HRZ	3-Phase CCM, 2-Phase CCM, 1-Phase	50	60	70	µA
		3-Phase DE	16	20	24	µA
		2-Phase DE	24	30	36	µA
	IRZ	3-Phase CCM, 2-Phase CCM, 1-Phase	49.5	60	70	µA
		3-Phase DE	16	20	24	µA
		2-Phase DE	23.5	30	36	µA
Northbridge OCP Current Threshold	HRZ	2-Phase CCM, 1-Phase	50	60	70	µA
		2-Phase DE	24	30	36	µA
	IRZ	2-Phase CCM, 1-Phase	49.5	60	70	µA
		2-Phase DE	23.5	30	36	µA

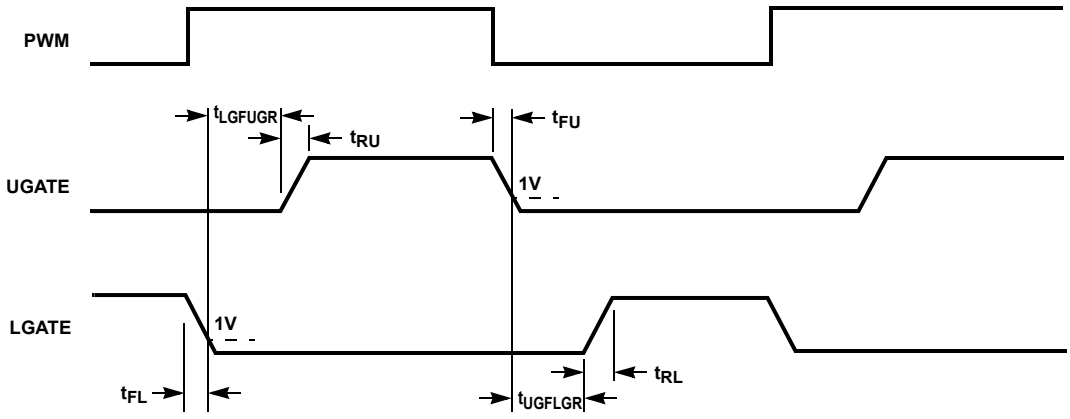
Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
LOGIC THRESHOLDS						
ENABLE Input Low	V_{IL}				**0.3**	V
ENABLE Input High	V_{IH}		**0.7**			V
PWM						
PWM Output Low	V_{0L}	Sinking 5mA			**1.0**	V
PWM Output High	V_{0H}	Sourcing 5mA	**3.5**			V
PWM Tri-State Leakage		PWM = 2.5V		2		µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	**57**		**67**	µA
NTC_NB Source Current		NTC_NB = 1.3V	**57**		**67**	µA
Thermal Monitor Trip Voltage		Falling Threshold	**0.87**	0.88	**0.89**	V
Thermal Monitor Reset Voltage		Rising Threshold	**0.91**	0.92	**0.93**	V
INPUTS						
ENABLE Leakage Current	I_{ENABLE}	EN = 0V	**-1**	0		µA
		EN = 1V		18	**36**	µA
Slew Rate (for VID Change)	SR		**5**	7.5	**10**	mV/µs
Soft-Start Slew Rate	SSR		**1.25**	1.875	**2.5**	mV/µs
SVI INTERFACE						
PWROK, SVC, SVD Input Logic High	V_{IH}		**0.798**			V
PWROK, SVC, SVD Input Logic Low	V_{IL}				**0.57**	V
SVC, SVD Leakage		EN = 0V, SVC and SVD = 0V			**1**	µA
		EN = 5V, SVC and SVD = 1.8V			**1**	µA

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Gate Driver Timing Diagram



Theory of Operation

Multiphase R^{3}™ Modulator

The ISL6267 is a multiphase regulator implementing two voltage regulators, V_{DD} and VDDNB, on one chip controlled by AMD's™ SVI1™ protocol. V_{DD} can be programmed for 1-, 2- or 3-phase operation. VDDNB can be configured for 1-phase or 2-phase operation. Both regulators use the Intersil patented R^{3}™ (Robust Ripple Regulator) modulator. The R^{3}™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 7 conceptually shows the multiphase R^{3}™ modulator circuit, and Figure 8 shows the operation principles.

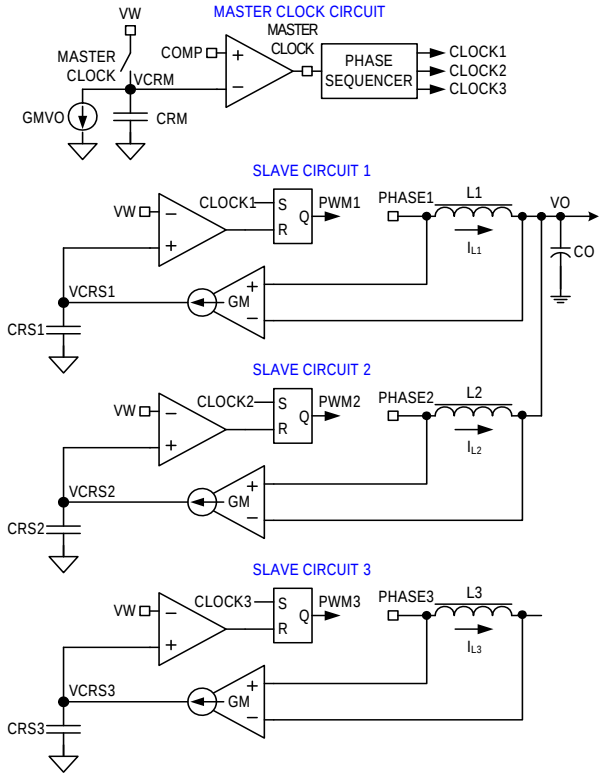


FIGURE 7. R^{3}™ MODULATOR CIRCUIT

A current source flows from the VW pin to the COMP pin, creating a voltage window set by the resistor between the two pins. This voltage window is called "VW window" in the following discussion.

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. C_{rm} voltage V_{CRM} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If V_{DD} is in 3-phase mode, the master clock signal is distributed to the three phases, and the Clock 1~3 signals will be 120° out-of-phase. If VR1 is in 2-phase mode, the master clock signal is distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If VR1 is in 1-phase mode, the master clock signal will be distributed to Phase 1 only and be the Clock1 signal.

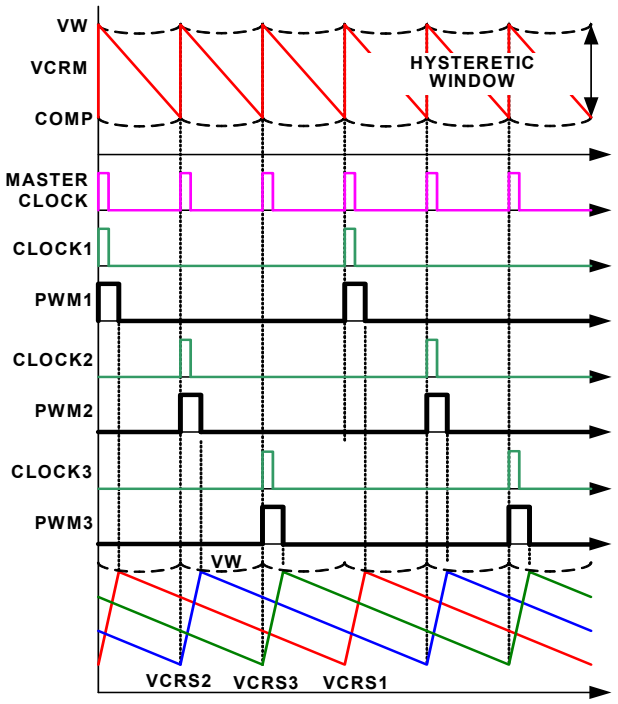


FIGURE 8. R^{3}™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

Each slave circuit has its own ripple capacitor C_{rs}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{rs}. When C_{rs} voltage V_{Crs} hits VW, the slave circuit turns off the PWM pulse, and the current source discharges C_{rs}.

Since the controller works with V_{crs}, which are large amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the error amplifier allows the ISL6267 to maintain a 0.5% output voltage accuracy.

Figure 9 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency. This allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL6267 excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

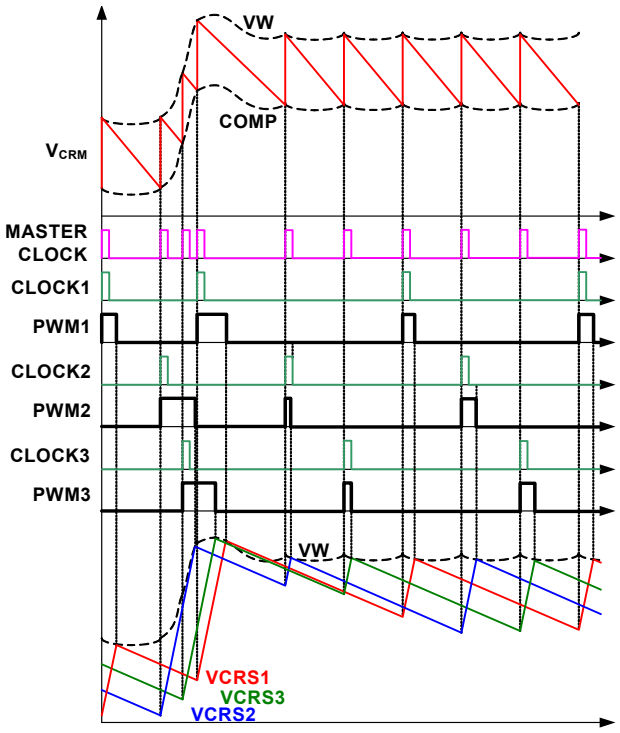


FIGURE 9. R^{3}™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

Diode Emulation and Period Stretching

The ISL6267 can operate in diode emulation (DE) mode to improve light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and does not allow reverse current, thus emulating a diode. As Figure 10 shows, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL6267 monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss. If the load current is light enough, (see Figure 10). The inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current will never reaches 0A, and the regulator is in CCM, although the controller is in DE mode.

Figure 11 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, making the inductor current triangle the same in the three cases. The ISL6267 clamps the ripple capacitor voltage V_{CRS} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{CRS}, naturally stretching the switching period. The inductor current triangles move farther apart such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

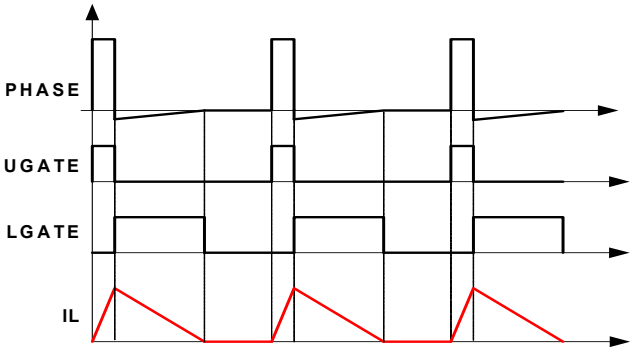


FIGURE 10. DIODE EMULATION

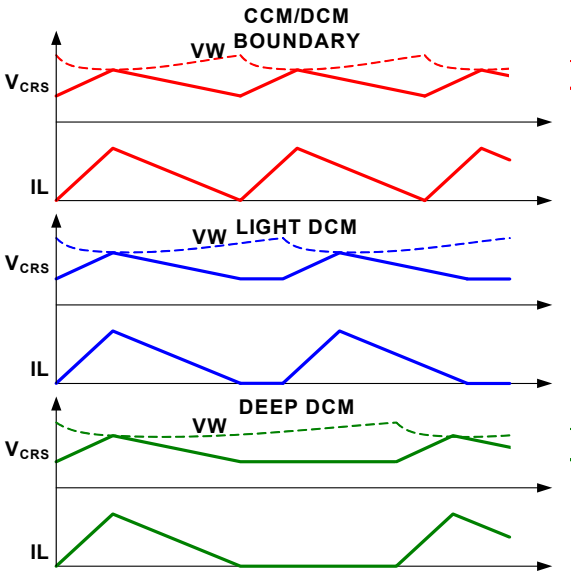


FIGURE 11. PERIOD STRETCHING

Start-up Timing

With the controller's V_{DD} and V_{IN} voltages above their POR threshold, the start-up sequence begins when ENABLE exceeds the logic high threshold. Figure 12 shows the typical start-up timing of VR1 and VR2. The ISL6267 uses digital soft-start to rampup DAC to the voltage programmed by the Metal VID. PGOOD is asserted high and low at the end of the rampup. Similar results occur if ENABLE is tied to V_{DD}, with the soft-start sequence starting 800µs after V_{DD} crosses the POR threshold.

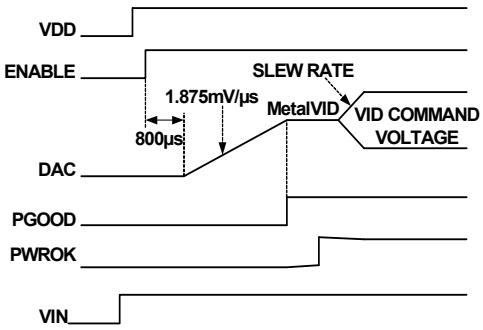


FIGURE 12. TYPICAL SOFT-START WAVEFORMS

Power-On Reset

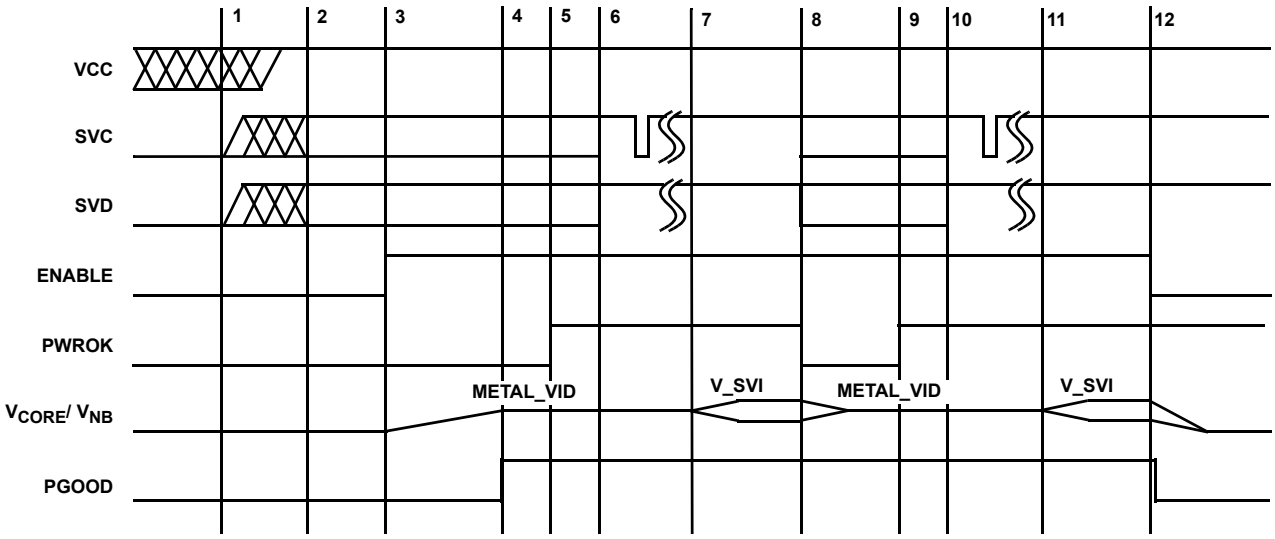
Before the controller has sufficient bias to guarantee proper operation, the ISL6267 requires both a +5V input supply tied to V_{CC} and PV_{CC}, as well as a battery or other input supply tied to V_{IN}, to exceed their respective rising power-on reset (POR) thresholds. Once these thresholds are reached or exceeded, the ISL6267 has enough bias to begin checking SVI inputs. Hysteresis between the rising and the falling thresholds assure the ISL6267 does not inadvertently turn off unless the bias voltage drops substantially (see "Electrical Specifications" on page 11).

Serial VID Interface

The on-board Serial VID Interface (SVI) circuitry allows the processor to directly control the Core and Northbridge voltage reference levels within the ISL6267. The SVC and SVD states are decoded according to the PWROK inputs as described in the following sections. The ISL6267 uses a digital-to-analog converter (DAC) to generate a reference voltage based on the decoded SVI value. See Figure 13 for a simple SVI interface timing diagram.

Pre-PWROK Metal VID

Typical motherboard start-up begins with the controller decoding the SVC and SVD inputs to determine the pre-PWROK Metal VID setting (see Table 1). Once the ENABLE input exceeds the rising threshold, the ISL6267 decodes and locks the decoded value in an on-board hold register.



Interval 1 to 2: ISL6267 waits to POR.

Interval 2 to 3: SVC and SVD are externally set to pre-Metal VID code.

Interval 3 to 4: ENABLE locks pre-Metal VID code. All outputs soft-start to this level.

Interval 4 to 5: PGOOD signal goes HIGH, indicating proper operation.

Interval 5 to 6: CPU detects PGOOD high, and drives PWROK high, to allow ISL6267 to prepare for SVI commands.

Interval 6 to 7: SVC and SVD data lines communicate change in VID code.

Interval 7 to 8: ISL6267 responds to VID-ON-THE-FLY code change.

Interval 8 to 9: PWROK is driven low, and ISL6267 returns all outputs to pre-PWROK Metal VID level.

Interval 9 to 10: PWROK driven high once again by CPU, and ISL6267 prepares for SVI commands.

Interval 10 to 11: SVC and SVD data lines communicate new VID code.

Interval 11 to 12: ISL6267 drives outputs to new VID code level.

Post 12: Enable falls, all internal drivers are tri-stated, and PGOOD is driven low.

FIGURE 13. SVI INTERFACE TIMING DIAGRAM: TYPICAL PRE-PWROK METAL VID START-UP

TABLE 1. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

The internal DAC circuitry begins to ramp Core and Northbridge VRs to the decoded pre-PWROK Metal VID output level. The digital soft-start circuitry ramps the internal reference to the target gradually at a fixed rate of approximately 2mV/µs. The controlled ramp of all output voltage planes reduces in-rush current during the soft-start interval. At the end of the soft-start interval, the PGOOD output transitions high, indicating all output planes are within regulation limits.

If the ENABLE input falls below the enable falling threshold, the ISL6267 tri-states both outputs. PGOOD is pulled low with the loss of ENABLE. The Core and Northbridge planes decay, based on output capacitance and load leakage resistance. If bias to V_{CC} falls below the POR level, the ISL6267 responds in the manner previously described. Once V_{CC} and ENABLE rise above their respective rising thresholds, the internal DAC circuitry reacquires a pre-PWROK metal VID code, and the controller soft-starts.

VFIX Mode

The ISL6267 does not support VFIX Mode. In the event a CPU is not present on a motherboard and the ISL6267 is powered on, the state of SVC and SVD sets the pre-PWROK metal VID as the “Pre-PWROK Metal VID” on page 16 and begins soft-starting.

SVI Mode

Once the controller has successfully soft-starts and PGOOD and PGOOD_NB transition high, the processor can assert PWROK to signal the ISL6267 to prepare for SVI commands. The controller actively monitors the SVI interface for set VID commands to move the plane voltages to start-up VID values. Details of the SVI Bus protocol are provided in the “AMD Design Guide for Voltage Regulator Controllers Accepting Serial VID Codes” specification.

Once a set VID command is received, the ISL6267 decodes the information to determine which VR is affected and which VID target is required (see Table 2). The internal DAC circuitry steps the output voltage of the VR commanded to the new VID level. During this time, one or more of the VR outputs could be targeted. In the event either VR is commanded to power-off by serial VID commands, the PGOOD signal remains asserted.

If the PWROK input is de-asserted, then the controller steps both the Core and the Northbridge VRs back to the stored pre-PWROK metal VID level in the holding register from initial soft-start. No attempt is made to read the SVC and SVD inputs during this time. If PWROK is re-asserted, then the on-board SVI interface waits for a set VID command.

If ENABLE goes low during normal operation, all internal drivers are tri-stated and PGOOD is pulled low. This event clears the pre-PWROK metal VID code and forces the controller to check SVC and SVD upon restart.

A POR event on either VCC or VIN during normal operation shuts down both regulators, and both PGOOD outputs are pulled low. The pre-PWROK metal VID code is not retained.

VID-on-the-Fly Transition

Once PWROK is high, the ISL6267 detects this flag and begins monitoring the SVC and SVD pins for SVI instructions. The microprocessor follows the protocol outlined in the following sections to send instructions for the VID-on-the-fly transitions. The ISL6267 decodes the instruction and acknowledges the new VID code. For the VID codes higher than the current VID level, the ISL6267 begins stepping the commanded VR outputs to the new VID target with a typical slew rate of 7.5mV/µs, which meets the AMD requirements.

When the VID codes are lower than the current VID level, the ISL6267 checks the state of PSI_L. If PSI_L is high, the controller begins stepping the regulator output to the new VID target with a typical slew rate of -7.5mV/µs. If PSI_L is low, the controller allows the output voltage to decay and slowly steps the DAC down with the natural decay of the output. This allows the controller to quickly recover and move to a high VID code if commanded. AMD requirements under these conditions do not require the regulator to meet the minimum slew rate specification of -5mV/µs. In either case, the slew rate is not allowed to exceed 10mV/µs. The ISL6267 does not change the state of PGOOD (VCCPWRGD in AMD specifications), when a VID-on-the-fly transition occurs.

SVI WIRE Protocol

The SVI WIRE protocol is based on the I^2C bus concept. Two wires [serial clock (SVC) and serial data (SVD)], carry information between the AMD processor (master) and the VR controller (slave) on the bus. The master initiates and terminates SVI transactions and drives the clock, SVC, during a transaction. The AMD processor is always the master, and the voltage regulators are the slaves. The slave receives the SVI transactions and acts accordingly. Mobile SVI WIRE protocol timing is based on high-speed mode I^2C. See AMD publication #40182 for additional details.

TABLE 2. SERIAL VID CODES

SVID [6:0]	VOLTAGE (V)	SVID [6:0]	VOLTAGE (V)	SVID [6:0]	VOLTAGE (V)	SVID [6:0]	VOLTAGE (V)
000_0000b	1.5500	010_0000b	1.1500	100_0000b	0.7500	110_0000b	0.3500*
000_0001b	1.5375	010_0001b	1.1375	100_0001b	0.7375	110_0001b	0.3375*
000_0010b	1.5250	010_0010b	1.1250	100_0010b	0.7250	110_0010b	0.3250*
000_0011b	1.5125	010_0011b	1.1125	100_0011b	0.7125	110_0011b	0.3125*
000_0100b	1.5000	010_0100b	1.1000	100_0100b	0.7000	110_0100b	0.3000*
000_0101b	1.4875	010_0101b	1.0875	100_0101b	0.6875	110_0101b	0.2875*
000_0110b	1.4750	010_0110b	1.0750	100_0110b	0.6750	110_0110b	0.2750*
000_0111b	1.4625	010_0111b	1.0625	100_0111b	0.6625	110_0111b	0.2625*
000_1000b	1.4500	010_1000b	1.0500	100_1000b	0.6500	110_1000b	0.2500*
000_1001b	1.4375	010_1001b	1.0375	100_1001b	0.6375	110_1001b	0.2375*
000_1010b	1.4250	010_1010b	1.0250	100_1010b	0.6250	110_1010b	0.2250*
000_1011b	1.4125	010_1011b	1.0125	100_1011b	0.6125	110_1011b	0.2125*
000_1100b	1.4000	010_1100b	1.0000	100_1100b	0.6000	110_1100b	0.2000*
000_1101b	1.3875	010_1101b	0.9875	100_1101b	0.5875	110_1101b	0.1875*
000_1110b	1.3750	010_1110b	0.9750	100_1110b	0.5750	110_1110b	0.1750*
000_1111b	1.3625	010_1111b	0.9625	100_1111b	0.5625	110_1111b	0.1625*
001_0000b	1.3500	011_0000b	0.9500	101_0000b	0.5500	111_0000b	0.1500*
001_0001b	1.3375	011_0001b	0.9375	101_0001b	0.5375	111_0001b	0.1375*
001_0010b	1.3250	011_0010b	0.9250	101_0010b	0.5250	111_0010b	0.1250*
001_0011b	1.3125	011_0011b	0.9125	101_0011b	0.5125	111_0011b	0.1125*
001_0100b	1.3000	011_0100b	0.9000	101_0100b	0.5000	111_0100b	0.1000*
001_0101b	1.2875	011_0101b	0.8875	101_0101b	0.4875*	111_0101b	0.0875*
001_0110b	1.2750	011_0110b	0.8750	101_0110b	0.4750*	111_0110b	0.0750*
001_0111b	1.2625	011_0111b	0.8625	101_0111b	0.4625*	111_0111b	0.0625*
001_1000b	1.2500	011_1000b	0.8500	101_1000b	0.4500*	111_1000b	0.0500*
001_1001b	1.2375	011_1001b	0.8375	101_1001b	0.4375*	111_1001b	0.0375*
001_1010b	1.2250	011_1010b	0.8250	101_1010b	0.4250*	111_1010b	0.0250*
001_1011b	1.2125	011_1011b	0.8125	101_1011b	0.4125*	111_1011b	0.0125*
001_1100b	1.2000	011_1100b	0.8000	101_1100b	0.4000*	111_1100b	OFF
001_1101b	1.1875	011_1101b	0.7875	101_1101b	0.3875*	111_1101b	OFF
001_1110b	1.1750	011_1110b	0.7750	101_1110b	0.3750*	111_1110b	OFF
001_1111b	1.1625	011_1111b	0.7625	101_1111b	0.3625*	111_1111b	OFF

NOTE: *Indicates a VID not required for AMD Family 10h processors.

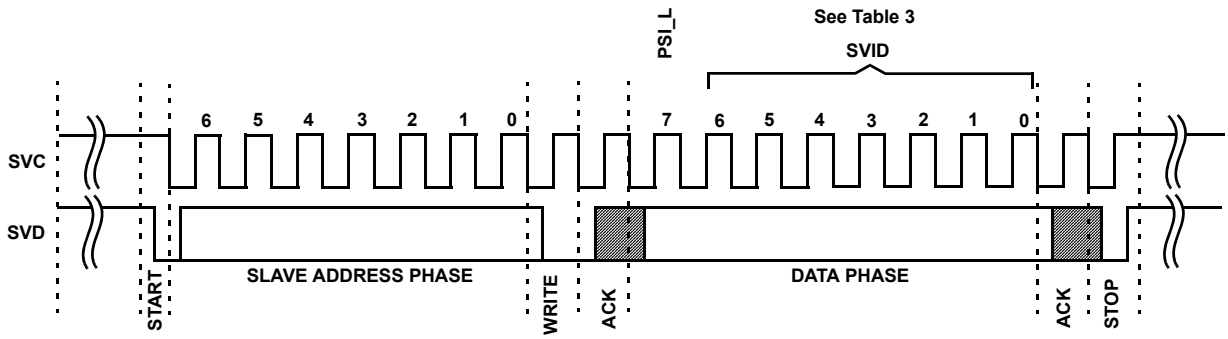


FIGURE 14. SEND BYTE EXAMPLE

SVI Bus Protocol

The AMD processor bus protocol is compliant with SMBus send byte protocol for VID transactions (see Figure 14). During a send byte transaction, the processor sends the start sequence followed by the slave address of the VR for which the VID command applies. The address byte must be configured according to Table 3. The processor then sends the write bit. After the write bit, if the ISL6267 receives a valid address byte, it sends the acknowledge bit. The processor then sends the PSI-L bit and VID bits during the data phase. The Serial VID 8-bit data field encoding is outlined in Table 4. If the ISL6267 receives a valid 8-bit code during the data phase, it sends the acknowledge bit. Finally, the processor sends the stop sequence. After the ISL6267 has detected the stop, it can then proceed with the VID-on-the-fly transition.

TABLE 3. SVI SEND BYTE ADDRESS DESCRIPTION

BITS	DESCRIPTION
6:4	Always 110b
3	Reserved by AMD for future use
2	VDD1; if set, then the following data byte contains the VID for VDD1 [Note: The ISL6267 does not support VDD1]
1	VDD0; if set, then the following data byte contains the VID for VID0
0	VDDNB; if set then the following data byte contains the VID for VIDNB

TABLE 4. SERIAL VID 8-BIT DATA FIELD ENCODING

BITS	DESCRIPTION
7	PSI_L: =0 means the processor is at an optimal load for the regulators to enter power-saving mode =1 means the processor is not at an optimal load for the regulators to enter power-saving mode
6:0	SVID[6:0] as defined in Table 2.

Operation

After the start-up sequence, the ISL6267 begins regulating the Core and Northbridge output voltages to the pre-PWROK metal VID programmed. The controller monitors SVI commands to determine when to enter power-saving mode, implement dynamic VID changes, and shut down individual outputs.

VR Offset Programming

A positive or negative offset is programmed for the Core VR using a resistor to ground from the PROG1 pin and the Northbridge in a similar manner from the PROG2 pin. Table 5 provides the resistor value to select the desired output voltage offset

TABLE 5. PROGx PIN RESISTOR VALUE

RESISTOR VALUE [Ω]	PROG1 $V_{CORE\ OFFSET}$ [mV]	PROG1 VNBOFFSET [mV]
0	50	50
590	43.75	43.75
1100	37.50	37.50
1690	31.25	31.25
2260	25.00	25.00
3160	18.75	18.75
4320	12.50	12.50
5620	6.25	6.25
6650	0.00	0.00
7870	-6.25	-6.25
9530	-12.50	-12.50
11500	-18.75	-18.75
14000	-25.00	-25.00
16500	-31.25	-31.25
18700	-37.50	-37.50
OPEN	-43.75	-43.75

Voltage Regulation and Load Line Implementation

After the start sequence, the ISL6267 regulates the output voltage to the value set by the VID information, per Table 2. The ISL6267 controls the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.55V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

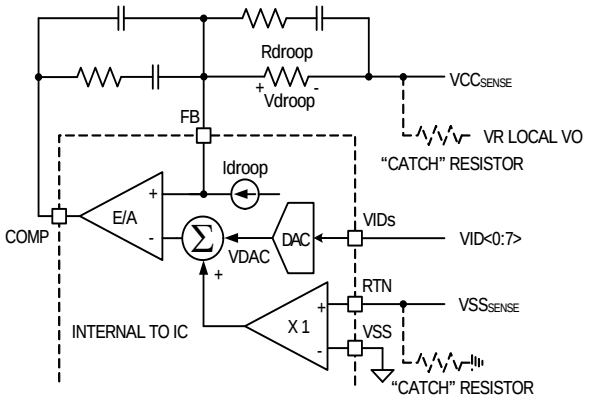


FIGURE 15. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage droops from the VID table value by an amount proportional to the load current, to achieve the load line. The ISL6267 can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors, as shown in Figures 15 and 16, or through resistors in series with the inductors as shown in Figure 17. In both methods, capacitor C_n voltage represents the inductor total currents. A droop amplifier converts C_n voltage into an internal current source with the gain set by resistor R_i. The current source is used for load line implementation, current monitoring and overcurrent protection.

Figure 15 shows the load-line implementation. The ISL6267 drives a current source (I_{droop}) out of the FB pin, as described by Equation 1.

$$I_{droop} = \frac{2xV_{Cn}}{R_i} \quad \text{(EQ. 1)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding, thus sustaining the load-line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 2.

$$V_{droop} = R_{droop} \times I_{droop} \quad \text{(EQ. 2)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can change the load line slope. Since I_{droop} sets the overcurrent protection level, it is recommended to first scale I_{droop} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Sensing

Figure 15 shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. The error amplifier regulates the inverting and non-inverting input voltages to be equal as shown in Equation 3:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 3)}$$

Rewriting Equation 3 and substituting Equation 2 gives Equation 4 is the exact equation required for load-line implementation.

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 4)}$$

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback is an open circuit in the absence of the processor. As Figure 15 shows, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and to add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, provide voltage feedback if the system is powered up without a processor installed.

Phase Current Balancing

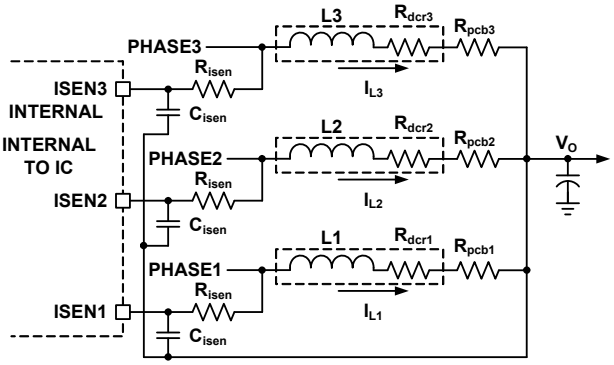


FIGURE 16. CURRENT BALANCING CIRCUIT

The ISL6267 monitors individual phase average current by monitoring the ISEN1, ISEN2, and ISEN3 voltages. Figure 16 shows the current balancing circuit recommended for the ISL6267. Each phase node voltage is averaged by a low-pass filter consisting of R_{isen} and C_{isen}, and is presented to the corresponding ISEN pin. R_{isen} should be routed to the inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 5 through 7 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 5)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 6)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 7)}$$

where R_{dcr1}, R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2} and I_{L3} are inductor average currents.

The ISL6267 adjusts the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using the same components for L1, L2 and L3 provides a good match of R_{dcr1}, R_{dcr2} and R_{dcr3}. Board layout determines R_{pcb1}, R_{pcb2} and R_{pcb3}. It is recommended to have symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

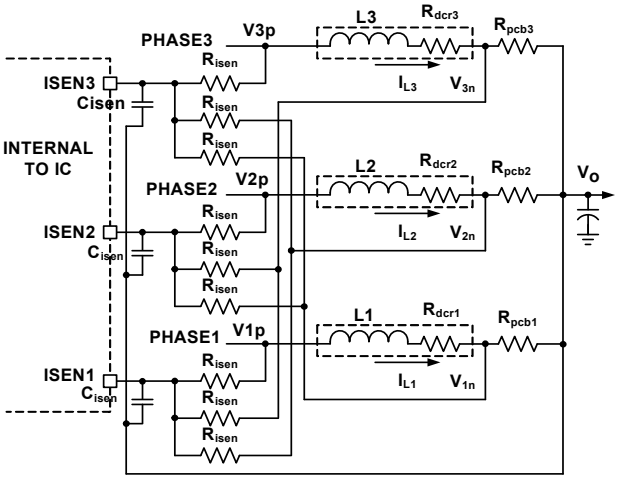


FIGURE 17. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes, it is difficult to implement symmetrical layout. For the circuit shown in Figure 16, asymmetric layout causes different R_{pcb1}, R_{pcb2} and R_{pcb3} values, thus creating a current imbalance. Figure 17 shows a differential sensing current balancing circuit recommended for the ISL6267. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own, phase inductor phase-node pad, and the other two phases inductor output side pads. Equations 8 through 10 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad \text{(EQ. 8)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 9)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 10)}$$

The ISL6267 will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as shown in Equations 11 and 12:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 11)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 12)}$$

Rewriting Equation 11 gives Equation 13:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 13)}$$

Rewriting Equation 12 gives Equation 14:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 14)}$$

Combining Equations 13 and 14 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 15)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 16)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) is achieved when $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2} and R_{pcb3} do not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, the R^{3}™ modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 18 shows the current balancing performance of the evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at a low repetition rate, but cannot keep up when the repetition rate gets into the hundred-kHz range, where it is out of the control loop bandwidth. The controller achieves excellent current balancing in all cases installed.

CCM Switching Frequency

The R_{fset} resistor between the COMP and the VW pins sets the VW windows size and therefore sets the switching frequency. When the ISL6267 is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the R^{3}™ modulator. As explained in the “Multiphase R3™ Modulator” on page 14, the effective switching frequency increases during load insertion and decreases during load release to achieve fast response. Thus, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 15% and does not have any significant effect on output voltage ripple magnitude. Equation 17 gives an estimate of the frequency-setting resistor (R_{fset}) value. A value of 8kΩ R_{fset} gives approximately 300kHz switching frequency. Lower resistance gives higher switching frequency.

$$R_{fset}(k\Omega) = (\text{Period}(\mu s) - 0.29) \times 2.65 \quad \text{(EQ. 17)}$$

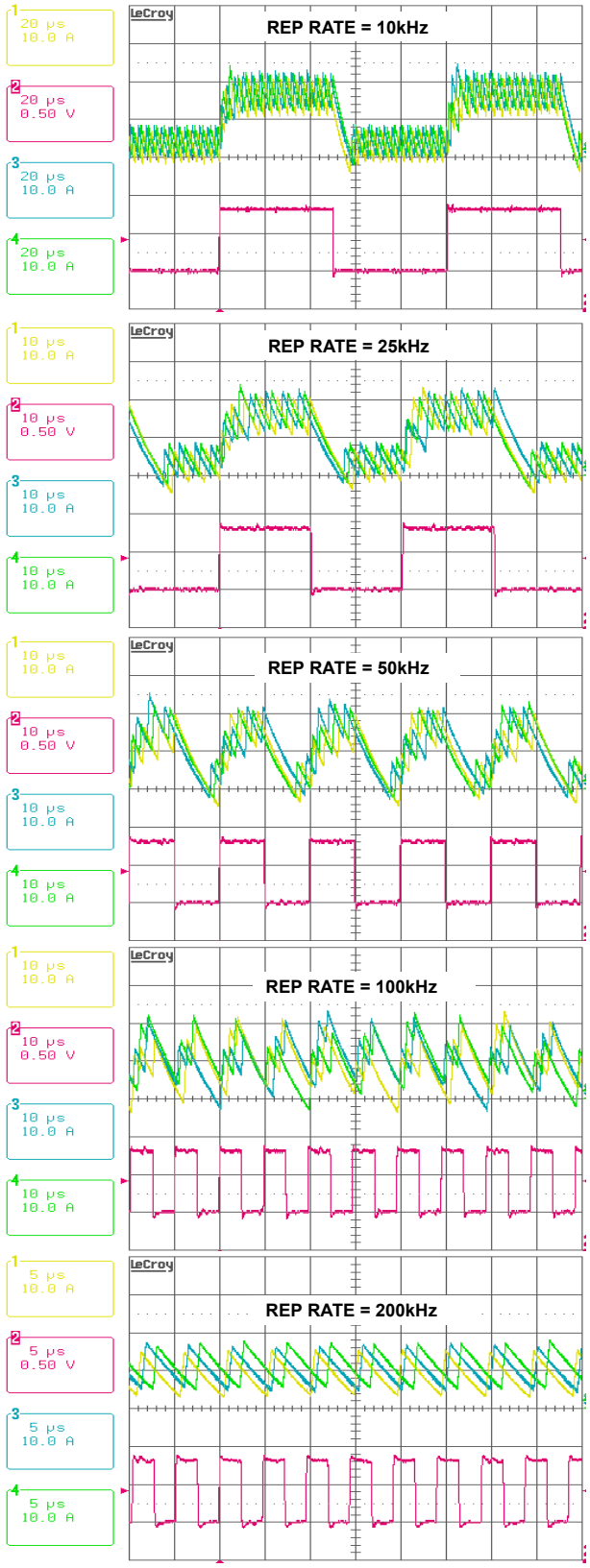


FIGURE 18. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: I_{L1}, CH2: I_{LOAD}, CH3: I_{L2}, CH4: I_{L3}

Modes of Operation

TABLE 6. CORE VR MODES OF OPERATION

PWM3	ISEN2	CONFIG.	PSI_L	MODE	OCP THRESHOLD (µA)
To External Driver	To Power Stage	3-phase CPU VR Config.	1	3-phase CCM	60
			0	1-phase DE	20
Tied to 5V		2-phase CPU VR Config.	1	2-phase CCM	60
			0	1-phase DE	30
	Tied to 5V	1-phase CPU VR Config.	X	1-phase DE	60

The Core VR can be configured for 3, 2- or 1-phase operation. Table 6 shows Core VR configurations and operational modes, programmed by the PWM3 and ISEN2 pin status and the PS command. For 2-phase configuration, tie the PWM3 pin to 5V. In this configuration, phases 1 and 2 are active. For 1-phase configuration, tie the PWM3 pin and the ISEN2 pin to 5V. In this configuration, only phase-1 is an active, the controller operates in DE mode and the PSI_L input been ignored.

In 3-phase configuration, Core VR operates in 3-phase CCM, with PSI_L high. It enters 1-phase DE mode when PSI_L is low, dropping phases 3 and 2, and reduces the overcurrent and the way-overcurrent protection levels to one-third of the initial values.

In 2-phase configuration, Core VR operates in 2-phase CCM with PSI_L high. It enters 1-phase DE mode with PSI_L low, by dropping phase 2 and reduces the overcurrent and the way overcurrent protection levels to one-half of the initial values.

In 1-phase configuration, the Core VR operates in 1-phase DE and ignores the PSI_L input. If a resistor is placed from COMP pin to GND with a value less than 150kΩ, then the Core VR operates in 1-phase CCM with PSI_L high and enters 1-phase DE mode when PSI_L is low. A resistor value of 100kΩ is recommended.

TABLE 7. NORTHBRIDGE VR MODES OF OPERATION

ISEN2_NB	CONFIG.	PSI_L	MODE	OCP THRESHOLD (µA)
To Power Stage	2-phase NB VR Config.	1	2-phase CCM	60
		0	1-phase DE	30
Tied to 5V	1-phase NB VR Config.	X	1-phase DE	60

ISL6267 Northbridge (NB) VR can be configured for 2- or 1-phase operation. Table 7 shows the Northbridge VR configurations and operational modes, which are programmed by the ISEN2 pin status and the PSI_L command. For 1-phase configuration, tie the ISEN2_NB pin to 5V. In 1-phase configuration, the Northbridge VR operates in 1-phase DE and ignores the PSI_L input. If a resistor is placed from COMP_NB pin to GND with a value less than 150kΩ, then the Northbridge VR operates in 1-phase CCM with PSI_L high and enters 1-phase DE mode when PSI_L is low. A resistor value of 100kΩ is recommended.

The Northbridge VR can be disabled completely by tying ISUMN_NB to 5V.

Dynamic Operation

Core VR and Northbridge VR behave the same during dynamic operation. The controller responds to VID-on-the-fly changes by slewing to the new voltage at the fixed 7.5mV/µs slew rate. During negative VID transitions, the output voltage decays to the lower VID value at the slew rate determined by the load.

SVI_L low command prompts the controller to enter DE mode. Overvoltage protection is blanked during VID down transition in DE mode until the output voltage is within 60mV of the VID value.

During load insertion response, the Fast Clock function increases the PWM pulse response speed. The controller monitors the VSEN pin voltage and compares it to 100ns-filtered version. When the unfiltered version is 20mV below the filtered version, the controller knows there is a fast voltage dip due to load insertion, and it issues an additional master clock signal to deliver a PWM pulse immediately.

The R^{3}™ modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

Protections

Core VR and Northbridge VR both provide overcurrent, current-balance and overvoltage fault protections. The controller also provides over-temperature protection. The following discussion is based on Core VR and also applies to Northbridge VR.

The controller determines overcurrent protection (OCP) by comparing the average value of the droop current (I_{droop}) with an internal current source threshold as Table 6 shows. It declares OCP when I_{droop} is above the threshold for 120µs.

For overcurrent conditions above 1.5x the OCP level, the PWM outputs immediately shuts off and PGOOD goes low to maximize protection. This protection is also referred to as way-overcurrent protection or fast overcurrent protection for short-circuit protections.

The controller monitors the ISEN pin voltages to determine current-balance protection. If the ISEN pin voltage difference is greater than 9mV for 1ms, the controller will declare a fault and latch off.

The controller takes the same actions for all of the previously describe fault protections: de-assertion of PGOOD and turn-off of the high-side and low-side power MOSFETs. Any residual inductor current decays through the MOSFET body diodes.

The controller declares an overvoltage fault and de-asserts PGOOD if the output voltage exceeds the VID set value by +250mV. The ISL6267 immediately declares an OV fault, de-asserts PGOOD, and turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value when all power MOSFETs are turned off. If the output voltage rises above the VID set value +250mV again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground.

All of the previously described fault conditions can be reset by bringing ENABLE low or by bringing V_{DD} below the POR threshold. When ENABLE and V_{DD} return to their high operating levels, a soft-start occurs.

Table 8 summarizes the fault protections.

TABLE 8. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs	PWM tri-state, PGOOD latched low	ENABLE toggle or V_{DD} toggle
Phase Current Unbalance	1ms		
Way-Overcurrent (1.5xOC)	Immediately		
Overvoltage +200mV		PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-state.	
Over-Temperature		400µs	N/A

FB2 Function

The FB2 function is only available for Core VR or Northbridge VR in 2-phase configuration.

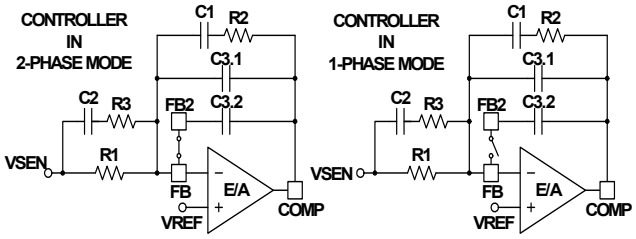


FIGURE 19. FB2 FUNCTION

Figure 19 shows the FB2 function. A switch (called FB2 switch) turns on to short the FB and the FB2 pins when the controller is in 2-phase mode. Capacitors C3.1 and C3.2 are in parallel, serving as part of the compensator. When the controller enters 1-phase mode, the FB2 switch turns off, removing C3.2 and leaving only C3.1 in the compensator. The compensator gain increases with the removal of C3.2. By properly sizing C3.1 and C3.2, the compensator can be optimal for both 2-phase mode and 1-phase mode.

When the FB2 switch is off, C3.2 is disconnected from the FB pin. However, the controller still actively drives the FB2 pin voltage to follow the FB pin voltage such that C3.2 voltage always follows C3.1 voltage. When the controller turns on the FB2 switch, C3.2 is reconnected to the compensator smoothly.

The FB2 function ensures excellent transient response in both 2-phase and 1-phase mode. If the FB2 function is not used, populate C3.1 only.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative, and the amount is the

MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it will flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it will flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET. To minimize the body diode-related loss, the controller also adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns.

Key Component Selection

Inductor DCR Current-Sensing Network

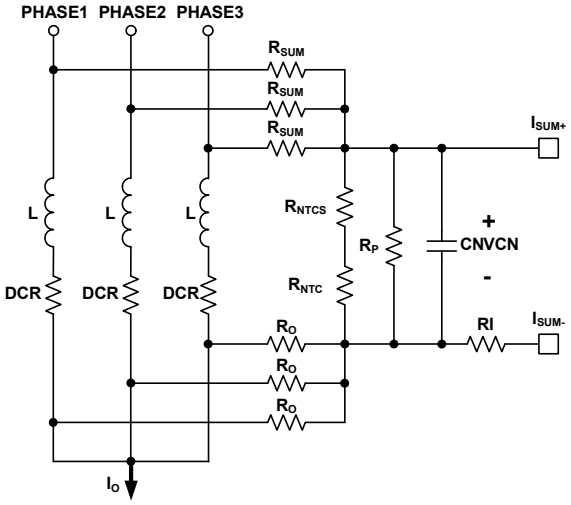


FIGURE 20. DCR CURRENT-SENSING NETWORK

Figure 20 shows the inductor DCR current-sensing network for a 3-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown, and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to temperature compensate the inductor DCR change.

The inductor output side pads are electrically shorted in the schematic but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use 1Ω~10Ω R_o to create quality signals. Since R_o value is much smaller than the rest of the current sensing circuit, the following analysis ignores it.

The summed inductor current information is presented to the capacitor C_n. Equations 18 thru 22 describe the frequency domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 18)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 19)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 20)}$$

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 21)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 22)}$$

where N is the number of phases.

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC R_{ntc} value decrease as its temperature decreases. Proper selection of R_{sum}, R_{ntcs}, R_p and R_{ntc} parameters ensures that V_{Cn} represents the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of V_{cn} to the inductor DCR voltage so the droop circuit has a higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole w_{sns} and a zero w_L. One needs to match w_L and w_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing w_L equal to w_{sns} and solving for the solution. Equation 23 gives Cn value.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 23)}$$

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ and L = 0.36µH, Equation 23 gives C_n = 0.406µF.

Assuming the compensator design is correct, Figure 21 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{core} also has a square response.

If C_n value is too large or too small, $V_{Cn}(s)$ does not accurately represent real-time $I_o(s)$ and worsens the transient response. Figure 22 shows the load transient response when C_n is too small. V_{core} sags excessively upon load insertion and may create a system failure. Figure 23 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value. There is excessive overshoot if load insertion occurs during this time, which may negatively affect the CPU reliability.

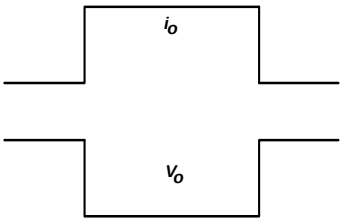


FIGURE 21. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

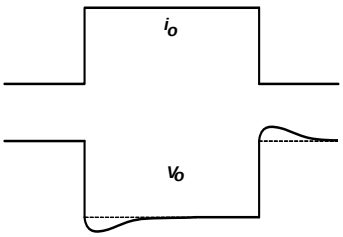


FIGURE 22. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

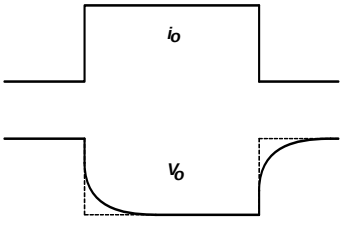


FIGURE 23. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

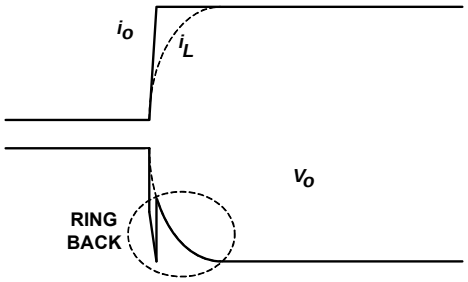


FIGURE 24. OUTPUT VOLTAGE RING-BACK PROBLEM

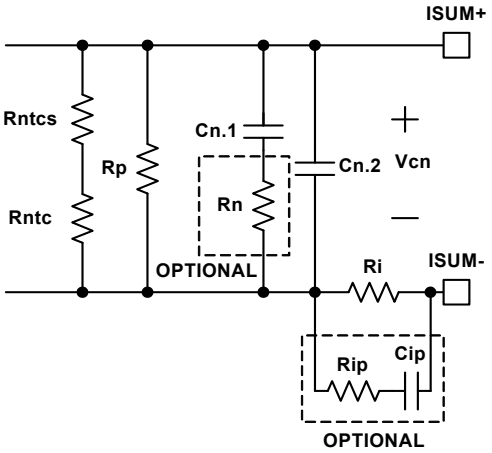


FIGURE 25. OPTIONAL CIRCUITS FOR RING-BACK REDUCTION

Figure 24 shows the output voltage ring-back problem during load transient response. The load current i_o has a fast step change, but the inductor current i_L cannot accurately follow. Instead, i_L responds in first-order system fashion due to the nature of the current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_o dip quickly upon load current change. However, the controller regulates V_o according to the droop current i_{droop}, which is a real-time representation of i_L; therefore, it pulls V_o back to the level dictated by i_L, causing the ring-back problem. This phenomenon is not observed when the output capacitor has very low ESR and ESL, as is the case with all ceramic capacitors.

Figure 25 shows two optional circuits for reduction of the ring-back. C_n is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 25 shows that two capacitors ($C_{n.1}$ and $C_{n.2}$) are in parallel. Resistor R_n is an optional component to reduce the V_o ring-back. At steady state, $C_{n.1}$ + $C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 22 shows, V_o tends to dip when C_n is too small, and this effect reduces the V_o ring-back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. R_n value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and R_n values should be determined through tuning the load transient response

waveforms on an actual board. R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of i_o change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L, and V_o will not ring back. The recommended value for R_{ip} is 100Ω. C_{ip} should be determined through tuning the load transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF. However, it should be noted that the R_{ip} -C_{ip} branch may distort the i_{droop} waveform. Instead of being triangular as the real inductor current, i_{droop} may have sharp spikes, which may adversely affect i_{droop} average value detection and therefore may affect OCP accuracy. User discretion is advised.

Resistor Current-Sensing Network

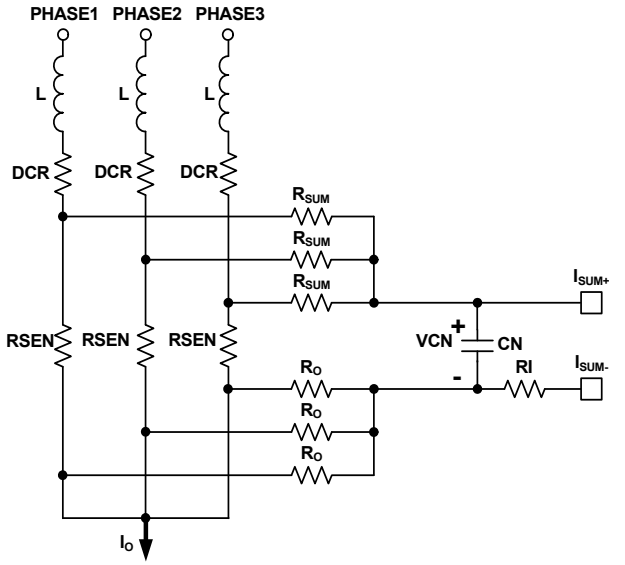


FIGURE 26. RESISTOR CURRENT-SENSING NETWORK

Figure 26 shows the resistor current-sensing network for a 2-phase solution. Each inductor has a series current sensing resistor, R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a filter for noise attenuation. Equations 24 thru 26 give the $V_{Cn}(s)$ expression.

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 24)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 25)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 26)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor R_{sen} value does not have significant variation over-temperature, so there is no need for the NTC network. The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

Overcurrent Protection

Refer to Equation 1 on page 20 and Figures 20, 24 and 26; resistor R_i sets the droop current, I_{droop}. Tables 6 and 7 show the internal OCP threshold. It is recommended to design I_{droop} without using the R_{comp} resistor.

For example, the OCP threshold is 60µA for 3-phase solution. I_{droop} is designed to be 40.9µA at full load. Therefore the OCP trip level is 1.5x of the full load current.

For inductor DCR sensing, Equation 27 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$:

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 27)}$$

Substitution of Equation 27 into Equation 1 gives Equation 28:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 28)}$$

Therefore:

$$R_i = \frac{2R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{droop}} \quad \text{(EQ. 29)}$$

Substitution of Equation 19 and application of the OCP condition in Equation 29 gives Equation 30:

$$R_i = \frac{2 \times \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{droopmax}} \quad \text{(EQ. 30)}$$

where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ, I_{omax} = 51A and $I_{droopmax}$ = 40.9µA. Equation 30 gives R_i = 606Ω.

For resistor sensing, Equation 31 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 31)}$$

Substitution of Equation 31 into Equation 1 gives Equation 32:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 32)}$$

Therefore:

$$R_i = \frac{2R_{sen} \times I_o}{N \times I_{droop}} \quad \text{(EQ. 33)}$$

Substitution of Equation 33 and application of the OCP condition in Equation 29 gives Equation 34:

$$R_i = \frac{2R_{sen} \times I_{omax}}{N \times I_{droopmax}} \quad \text{(EQ. 34)}$$

where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sen} = 1mΩ, I_{omax} = 51A and $I_{droopmax}$ = 40.9µA, Equation 34 gives R_i = 831Ω.

Load Line Slope

See Figure 15 for load-line implementation.

For inductor DCR sensing, substitution of Equation 28 into Equation 2 gives the load-line slope expression in Equation 35:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \quad \text{(EQ. 35)}$$

For resistor sensing, substitution of Equation 32 into Equation 2 gives the load line slope expression in Equation 36:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{sen} \times R_{droop}}{N \times R_i} \quad \text{(EQ. 36)}$$

Substitution of Equation 29 and rewriting Equation 35, or substitution of Equation 33 and rewriting Equation 36, gives the same result as in Equation 37:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad \text{(EQ. 37)}$$

One can use the full-load condition to calculate R_{droop}. For example, given I_{omax} = 51A, $I_{droopmax}$ = 40.9µA and LL = 1.9mΩ, Equation 37 gives R_{droop} = 2.37kΩ.

It is recommended to start with the R_{droop} value calculated by Equation 37 and fine-tune it on the actual board to get accurate load-line slope. One should record the output voltage readings at no load and at full load for load-line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Compensator

Figure 21 shows the desired load transient response waveforms. Figure 27 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load-line slope LL, i.e., a constant output impedance, then in the entire frequency range, V_o will have a square response when I_o has a square change.

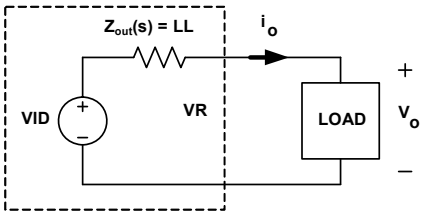


FIGURE 27. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network so that VR achieves constant output impedance as a stable system.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop, which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 28 conceptually shows T1(s) measurement set-up, and Figure 29 conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load-line slope, adds it on top of the sensed output voltage, and then feeds it to the compensator. T1 is measured after the summing node, and T2 is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can actually be measured on an ISL6267 regulator.

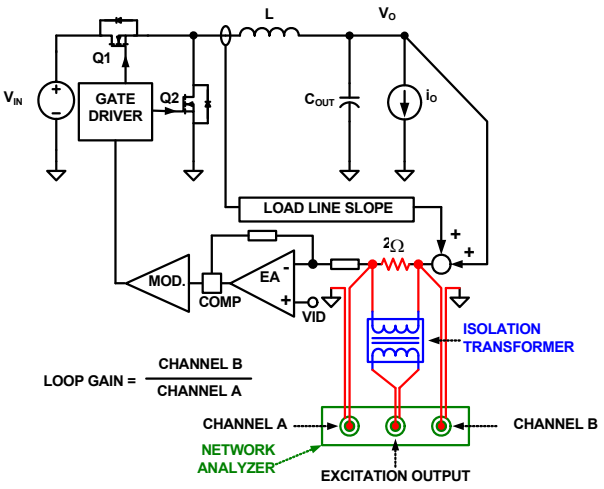


FIGURE 28. LOOP GAIN T1(s) MEASUREMENT SET-UP

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s), therefore has a higher impact on system stability.

T2(s) is the voltage loop gain with closed droop loop, thus having a higher impact on output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin and an output impedance equal to or smaller than the load-line slope.

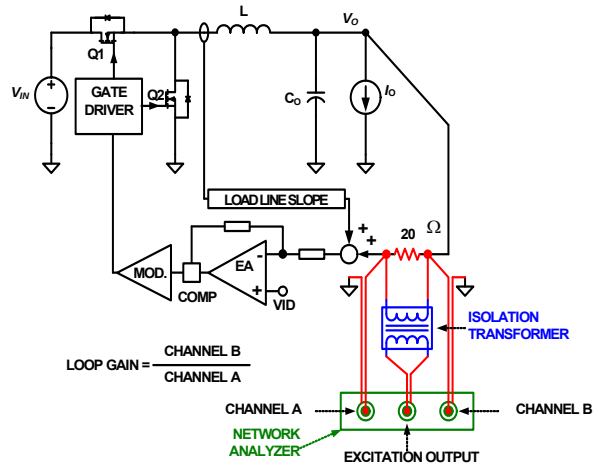


FIGURE 29. LOOP GAIN T2(s) MEASUREMENT SET-UP

Current Balancing

Refer to Figures 16 through 20 for information on current balancing. The ISL6267 achieves current balancing through matching the ISEN pin voltages. R_{isen} and C_{isen} form filters to remove the switching ripple of the phase node voltages. It is recommended to use a rather long $R_{isen}C_{isen}$ time constant such

that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are R_S = 10kΩ and C_S = 0.22µF.

NTC Thermal Monitors and VR_HOT Function

The ISL6267 features three pins (NTC, NTC_NB, and VR_HOT) which are allow the IC to monitor board temperature and alert the AMD CPU of a thermal issue. Figure 30 shows the thermal monitor feature of the ISL6267. An NTC network is connected between the NTC and NTC_NB pins and GND. The controller drives a 60µA current source out of the NTC pin and the NTC_NB pin alternatively at 1kHz frequency with 50% duty cycle. The pulsed current flows through the respective NTC resistor network on the pins and creates a voltage that is compared to an over-temperature trip threshold. If the voltage on both NTC pins is higher than the over-temperature trip threshold, then VR_HOT is pulled up by an external resistor on the pin.

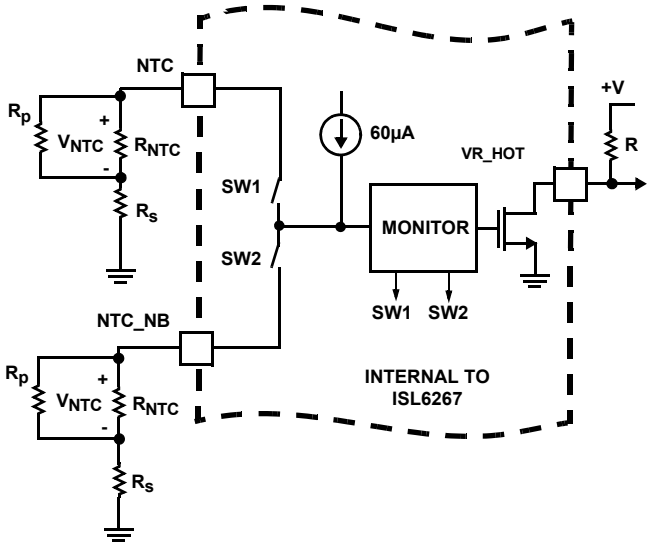


FIGURE 30. CIRCUITRY ASSOCIATED WITH THE THERMAL MONITOR FEATURE OF THE ISL6267

As the board temperature rises, the NTC thermistor resistance decreases and the voltage at the NTC pin drops. When the voltage on the NTC pin drops below the over-temperature trip threshold, then VR_HOT is pulled low. The VR_HOT signal is used to change the CPU operation and decrease power consumption. With the reduction in power consumption by the CPU, the board temperature decreases and the NTC thermistor voltage rises. Once the over-temperature threshold is tripped and VR_HOT is taken low, the over-temperature threshold changes to the reset level. The addition of hysteresis to the over-temperature threshold prevents nuisance trips. Once both pin voltages exceed the over-temperature reset threshold, the pull-down on VR_HOT is released. The signal changes state and the CPU resumes normal operation. The over-temperature threshold returns to the trip level.

Selection of the NTC components can vary depending on how the resistor network is configured. The equivalent resistance at the typical over-temperature threshold voltage of 0.88V, to change the state of VR_HOT, is defined in Equation 38.

$$\frac{0.88V}{60\mu A} = 14.7k \quad \text{(EQ. 38)}$$

The equivalent resistance at the typical reset threshold voltage of 0.92V required to change the state of VR_HOT back low, is defined in Equation 39

$$\frac{0.92V}{60\mu A} = 15.3k \quad \text{(EQ. 39)}$$

The NTC thermistor value correlates this resistance change to the required temperature hysteresis. A standard 1% resistor is typically needed to meet the NTC pin threshold voltage.

For example, a Panasonic NTC thermistor with B = 4700 has a resistance ratio of 0.03322 of its nominal value at +105°C and 0.03956 of its nominal value at +100°C. The required resistance of the NTC is defined in Equation 40.

$$\frac{(15.3k\Omega - 14.7k\Omega)}{(0.03956 - 0.03322)} = 94.6k\Omega \quad \text{(EQ. 40)}$$

The closest, larger thermistor value for B = 4700 is 100kΩ. The NTC thermistor part number is ERTJ1VV104.

At +105°C, a 100kΩ NTC resistance drops to (0.03322 x 100kΩ) = 3.322kΩ. With a 60µA current flowing out of the NTC pin, the voltage drop across the resistor is only (3.322kΩ x 60µA) = 0.199V. This value is much lower than the threshold voltage of 0.88V. A standard resistor, 1% tolerance, added in series with the thermistor is required to raise the voltage on the pin. The resistance required to meet the trip threshold is calculated in Equation 41.

$$\frac{0.88V}{60\mu A} - 3.322k\Omega = 11.34k\Omega \quad \text{(EQ. 41)}$$

The closest, standard 1% tolerance resistor is 11.3kΩ.

The NTC thermistor is placed in a hot spot on the board, typically near the upper MOSFET of channel 1 of the respective output. The standard resistor is placed next to the controller.

Layout Guidelines

Table 9 shows layout considerations for the ISL6267 controller. Refer to the reference designators shown in Figure 31.

TABLE 9. LAYOUT CONSIDERATIONS FOR THE ISL6267 CONTROLLER

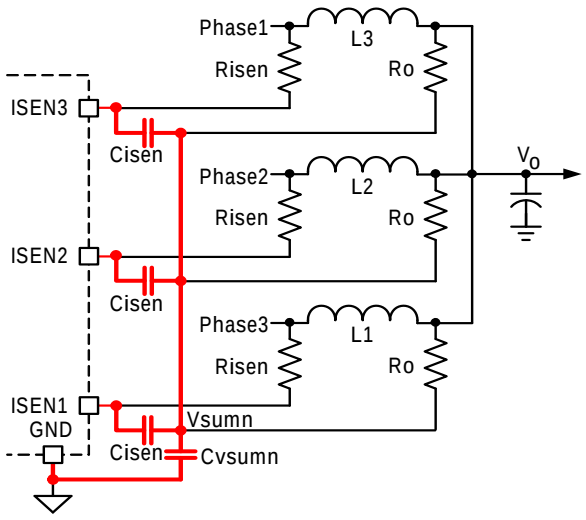
ISL6267	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Create analog ground plane underneath the controller and the analog signal processing components. Do not let the power ground plane overlap with the analog ground plane. Avoid allowing noisy planes/traces (e.g., phase node) to crossover/overlap the analog plane.
1	FB2_NB	Place the compensator components (R25, R9, R24, C88, C51, C86, and C153) close to the controller.
2	FB_NB	
3	COMP_NB	
4	VW_NB	Place the capacitor (C85) across VW, and place COMP close to the controller.
5	PGOOD_NB	No special consideration.
6, 7, 8	SVD, PWROK, SVC	Use good signal integrity practices.
9	ENABLE	No special consideration.
10	PGOOD	No special consideration.
11	VR_HOT	No special consideration.
12	NTC	Place the NTC thermistor (R46) close to the thermal source that is monitored to determine CPU V_{CORE} thermal throttling. Usually it is placed close to Core VR phase-1 high-side MOSFET.
13	VW	Place the capacitor (C4) across VW and COMP close to the controller.
14	COMP	Place the compensator components (R7, R10, R11, C3, C6, C11 and C5) in general proximity to the controller.
15	FB	
16	FB2	
	ISEN3	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN and then through another capacitor (C_{vsumn}) to GND. Place Cisen capacitors as close as possible to the controller and keep the following loops small: 1. Any ISEN pin to another ISEN pin 2. Any ISEN pin to GND The red traces in the following drawing show the loops to be minimized. 
17	ISEN2	
18	ISEN1	
19	VSEN	Place the VSEN/RTN filter (C12, C13) close to the controller for good decoupling.
20	RTN	

TABLE 9. LAYOUT CONSIDERATIONS FOR THE ISL6267 CONTROLLER (Continued)

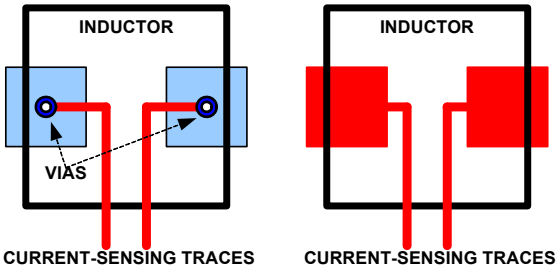
ISL6267	SYMBOL	LAYOUT GUIDELINES
21	ISUMN	Place the current sensing circuit in general proximity of the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to VR1 phase-1 inductor (L1) so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUMP and VSUMN signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. Route R63 and R71 to Core VR phase-1 side pad of inductor L1. Route R88 to the output side pad of inductor L1. Route R65 and R72 to Core VR phase-2 side pad of inductor L2. Route R90 to the output side pad of inductor L2. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. 
22	ISUMP	
23	VDD	A capacitor (C16) decouples it to GND. Place it in close proximity to the controller.
24	VIN	A capacitor (C17) decouples it to GND. Place it in close proximity to the controller.
25	PROG1	No special consideration.
26	BOOT1	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
27	UGATE1	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE1 trace to VR1 phase-1 high-side MOSFET (Q2 and Q8) source pins instead of general copper.
28	PHASE1	
29	LGATE1	Use decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
30	PWM3	No special consideration.
31	VCCP	A capacitor (C22) decouples it to GND. Place it in close proximity to the controller.
32	LGATE2	Use decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
33	PHASE2	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE2 trace to VR1 phase-2 high-side MOSFET (Q4 and Q10) source pins instead of general copper.
34	UGATE2	
35	BOOT2	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
36	PWM2_NB	No special consideration.
37	LGATE1_NB	Use decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
38	PHASE1_NB	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE1G trace to VR2 phase-1 high-side MOSFET source pins instead of general copper.
39	UGATE1_NB	
40	BOOT1_NB	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
41	PROG2	No special consideration.
42	NTC_NB	Place the NTC thermistor close to the thermal source that is monitored to determine GT V_{CORE} thermal throttling. Usually it is placed close to Northbridge VR phase-1 high-side MOSFET.
43	ISUMN_NB	Place the current sensing circuit in general proximity to the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to Northbridge VR phase-1 inductor (L1) so it senses the inductor temperature correctly. See ISUMN and ISUMP pins for layout guidelines of current-sensing trace routing.
44	ISUMP_NB	

TABLE 9. LAYOUT CONSIDERATIONS FOR THE ISL6267 CONTROLLER (Continued)

ISL6267	SYMBOL	LAYOUT GUIDELINES
45	RTN_NB	Place the VSEN/RTN filter (C89, C90) in close proximity to the controller for good decoupling.
46	VSEN_NB	
47	ISEN2_NB	See ISEN1, ISEN2 and ISEN3 pins for layout guidelines of current-balancing circuit trace routing.
48	ISEN1_NB	

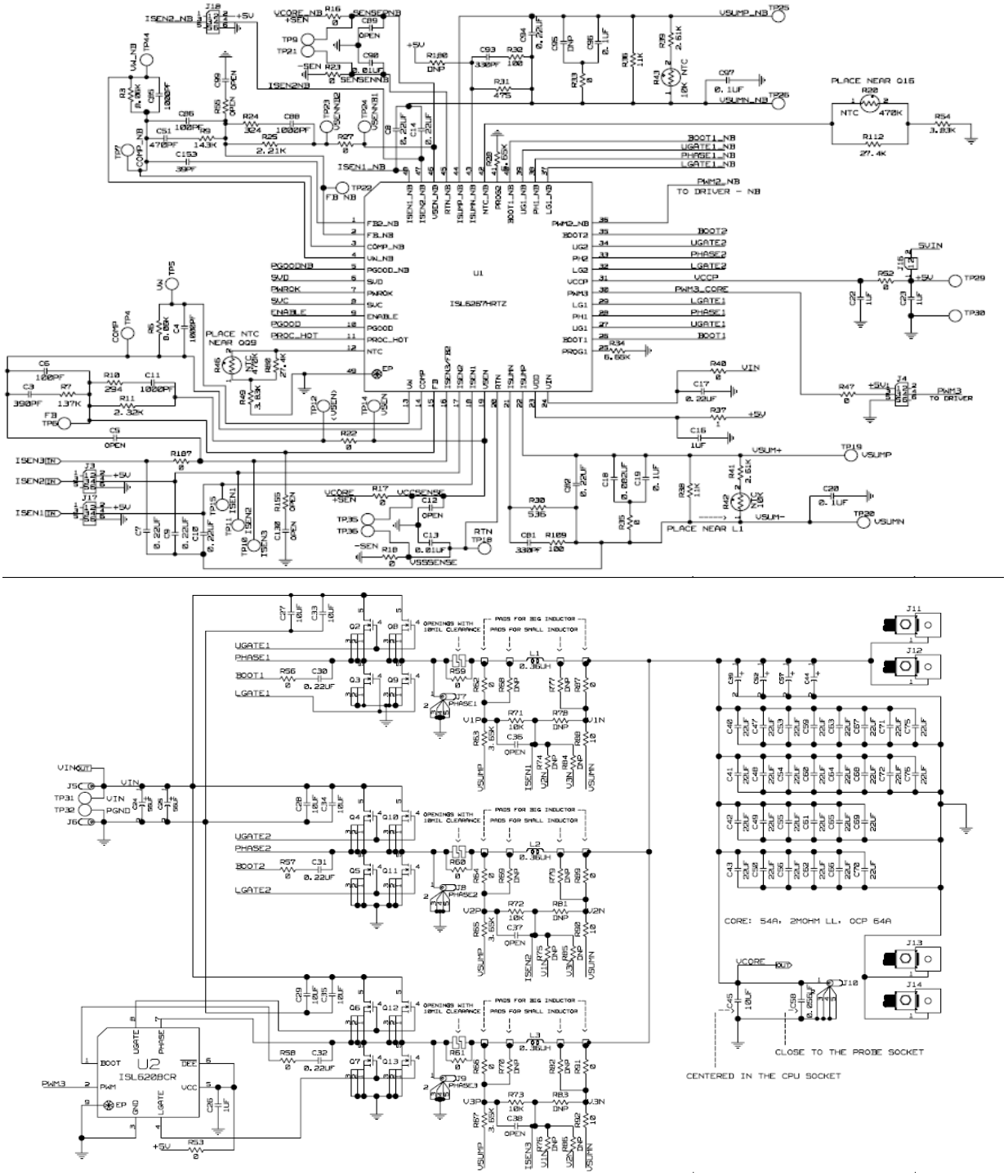


FIGURE 31. PORTION OF ISL6267EVAL1Z EVALUATION BOARD SCHEMATIC

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
1/31/11	FN7801.0	Initial Release.
November 5, 2012	FN7801.1	Page 9: Added IRZ parts to ordering information table.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL6267

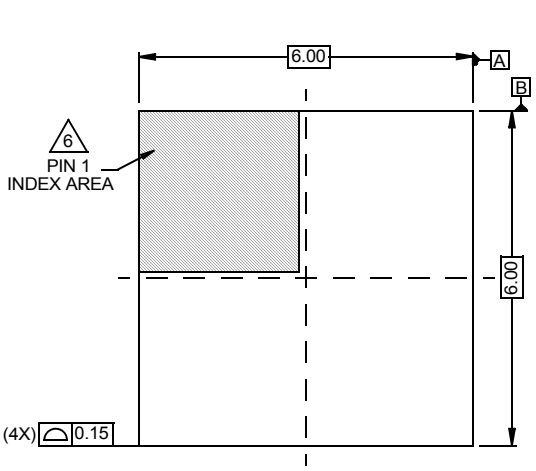
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

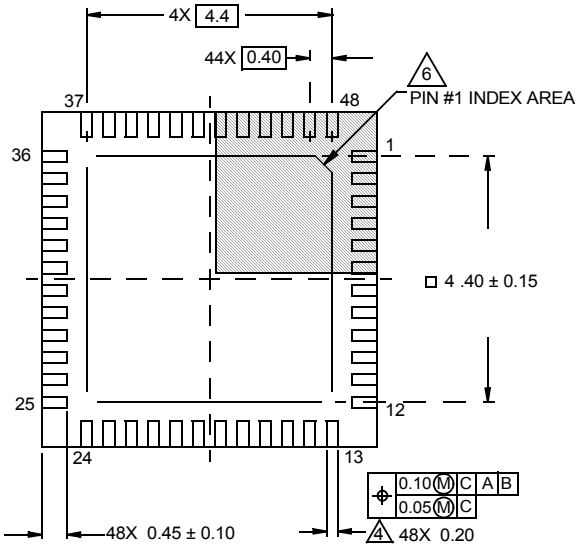
Package Outline Drawing

L48.6x6B

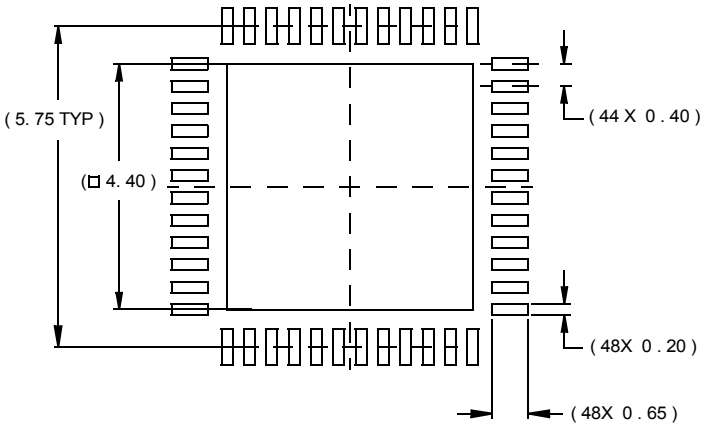
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 9/09



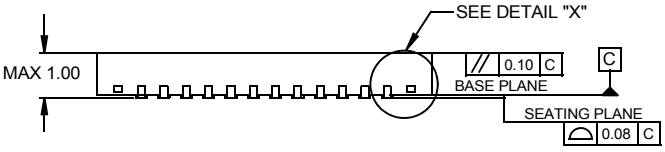
TOP VIEW



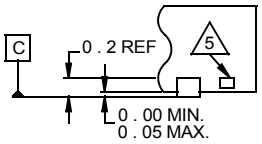
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.