ISL43485

3.3V, Low Power, 30Mbps, RS-485/RS-422 Transceiver

FN6071
Rev.2.00
Sep 19, 2018

The Renesas ISL43485 is a high speed BiCMOS 3.3V powered, single transceiver that meets both the RS-485 and RS-422 standards for balanced communication. Unlike some competitive devices, this transceiver is specified for 10% tolerance supplies (3V to 3.6V).

Data rates up to 30Mbps are achievable by using this transceiver, which features higher slew rates.

Logic inputs (for example, DI and DE) accept signals in excess of 5.5V, making them compatible with 5V logic families.

The receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high output if Rx inputs are floating. The ISL43485 presents a “single unit load” to the RS-485 bus, which allows up to 32 transceivers on the network.

The driver (Tx) outputs are short-circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

Related Literature

For a full list of related documents, visit our website:

- ISL43485 product page

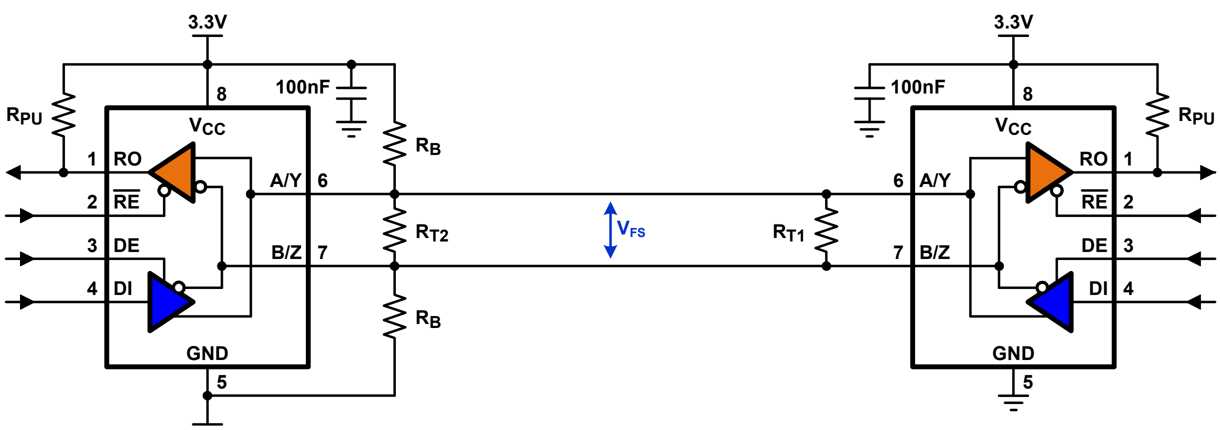
Features

- High data rate. . . . . up to 30Mbps
- Operates from a single +3.3V supply (10% tolerance)
- Interoperable with 5V logic
- Single unit load allows up to 32 devices on the bus
- Low current shutdown mode 15nA
- -7V to +12V common-mode input voltage range
- Three state Rx and Tx outputs
- 10ns propagation delay, 1ns skew
- Half duplex pinout
- Current limiting and thermal shutdown for driver overload protection
- Pb-free available (RoHS compliant)

Applications

- SCSI “Fast 20” drivers and receivers
- Factory automation
- Data loggers
- Security networks
- Building environmental control systems
- Industrial/process control networks
- Level translators

Typical Operating Circuit



To calculate the resistor values, refer to TB509.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL43485IBZ	43485IBZ	-40 to +85	-	8 Ld SOIC	M8.15
ISL43485IBZ-T	43485IBZ	-40 to +85	2.5k	8 Ld SOIC	M8.15

NOTES:

1. Refer to TB347 for details about reel specifications.
2. Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL43485 product information page. For more information about MSL, see TB363.

Pinout

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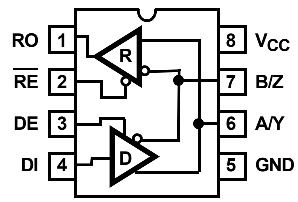
TOP VIEW



Pin Descriptions

PIN	FUNCTION
RO	Receiver output: RO is high if A > B by at least 0.2V; RO is low if A < B by 0.2V or more; RO is high if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	Noninverting receiver input and noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
B/Z	Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
V_{CC}	System power supply input (3V to 3.6V).

Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z *	High-Z *

NOTE: *Shutdown Mode

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs Open	1
1	0	X	High-Z *
1	1	X	High-Z

NOTE: *Shutdown Mode

Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . -0.5V to +7V
Input/Output Voltages
A/Y, B/Z . . . . -8V to +12.5V
RO . . . . -0.5V to (V_{CC} +0.5V)
Short-Circuit Duration
Y, Z . . . . Continuous

Operating Conditions

Temperature Range . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
8 Ld SOIC Package 170
Maximum Junction Temperature (Plastic Package) . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . +300°C
(Lead Tips Only)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V; unless otherwise specified. Typicals are at V_{CC} = 3.3V, T_A = +25°C, Note 5

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS								
Driver Differential V_{OUT} (no load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with load)	V_{OD2}	R_L = 100Ω (RS-422) (Figure 1A)		Full	2	2.7	-	V
		R_L = 54Ω (RS-485) (Figure 1A)		Full	1.5	2.3	V_{CC}	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 1B)		Full	1.5	2.6	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	1.8	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DE, DI		Full	-2	-	2	µA
		$\overline{RE}$		Full	-25	-	25	µA
Input Current (A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	0.6	1	mA
			V_{IN} = -7V	Full	-	-0.3	-0.8	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		+25	-	50	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	V_{CC} - 0.4	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = 200mV		Full	-	-	0.4	V

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V; unless otherwise specified. Typicals are at V_{CC} = 3.3V, T_A = +25°C, Note 5 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
Three-State (high impedance) Receiver Output Current	I_{OZR}	$0.4V \le V_O \le 2.4V$		Full	-1	-	1	µA
Receiver Input Resistance	R_{IN}	$-7V \le V_{CM} \le 12V$		Full	12	19	-	kΩ
No-Load Supply Current (Note 3)	I_{CC}	DI = 0V or V_{CC}	DE = V_{CC}, $\overline{RE}$ = 0V or V_{CC}	Full	-	0.75	1.2	mA
			DE = 0V, $\overline{RE}$ = 0V	Full	-	0.65	1	mA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	15	100	nA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, $-7V \le V_Y$ or $V_Z \le 12V$ (Note 7)		Full	-	-	250	mA
Receiver Short-Circuit Current	I_{OSR}	$0V \le V_O \le V_{CC}$		Full	8	-	60	mA
DRIVER SWITCHING CHARACTERISTICS								
Maximum Data Rate	f_{MAX}	(Figure 2A)		Full	30	50	-	Mbps
Driver Differential Output Delay	t_{DD}	R_{DIFF} = 60Ω, C_L = 15pF (Figure 2A)		Full	3	10	25	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 60Ω, C_L = 15pF (Figure 2A)		Full	3	6	12	ns
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_L = 27Ω, C_L = 15pF (Figure 2C)		Full	6	10	22	ns
Driver Output Skew	t_{SKEW}	R_L = 27Ω, C_L = 15pF (Figure 2C)		Full	-	1	5	ns
Driver Enable to Output High	t_{ZH}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 3), (Note 8)		Full	-	45	90	ns
Driver Enable to Output Low	t_{ZL}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 3), (Note 8)		Full	-	45	90	ns
Driver Disable from Output High	t_{HZ}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 3)		Full	-	60	90	ns
Driver Disable from Output Low	t_{LZ}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 3)		Full	-	70	100	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 3), (Notes 10, 11)		Full	-	115	150	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 3), (Notes 10, 11)		Full	-	115	150	ns
RECEIVER SWITCHING CHARACTERISTICS								
Maximum Data Rate	f_{MAX}	$V_{ID} \ge 1.5V$ with t_r/t_f = 10ns, RO t_H & $t_L \ge 60\%$ t_{UI} (Figure 4)		Full	27	35	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 4)		Full	25	45	80	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 4)		Full	-	2	12	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 5), (Note 9)		Full	-	11	25	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 5), (Note 9)		Full	-	11	25	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 5)		Full	-	7	20	ns

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V; unless otherwise specified. Typicals are at V_{CC} = 3.3V, T_A = +25°C, Note 5 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNIT
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 5)	Full	-	7	20	ns
Time to Shutdown	t_{SHDN}	(Note 10)	Full	80	190	300	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 5), (Notes 10, 12)	Full	-	240	400	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 5), (Notes 10, 12)	Full	-	240	400	ns

NOTES:

5. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
6. Supply current specification is valid for loaded drivers when DE = 0V.
7. Applies to peak current. See “Typical Performance Curves” on page 9 for more information.
8. When testing this parameter, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
9. When testing this parameter, the $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
10. The ISL43485 is put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 80ns, the parts are ensured not to enter shutdown. If the inputs are in this state for at least 300ns, the parts are ensured to have entered shutdown. See “Low Power Shutdown Mode” on page 8.
11. Keep $\overline{RE}$ = VCC, and set the DE signal low time >300ns to ensure that the device enters SHDN.
12. Set the $\overline{RE}$ signal high time >300ns to ensure that the device enters SHDN.

Test Circuits and Waveforms

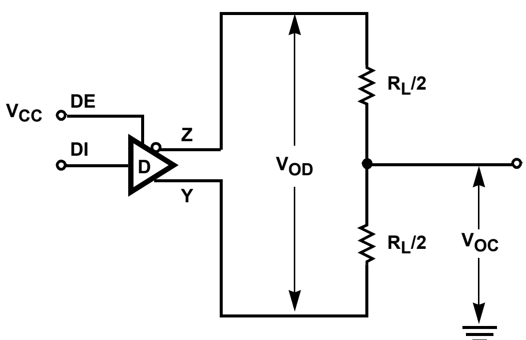


FIGURE 1A. V_{OD} AND V_{OC}

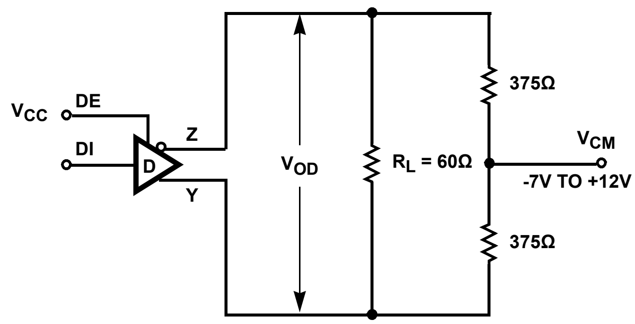


FIGURE 1B. V_{OD} WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

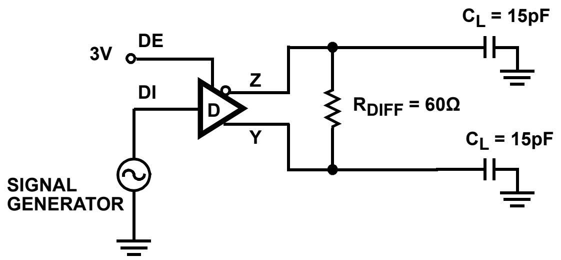
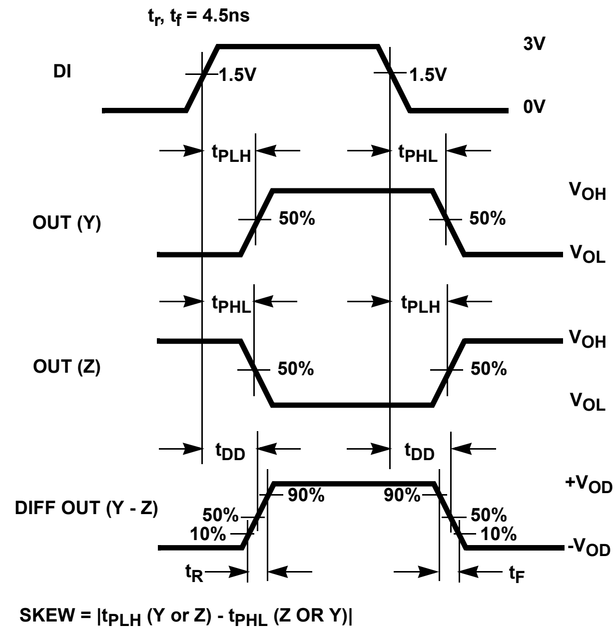


FIGURE 2A. DIFFERENTIAL TEST CIRCUIT



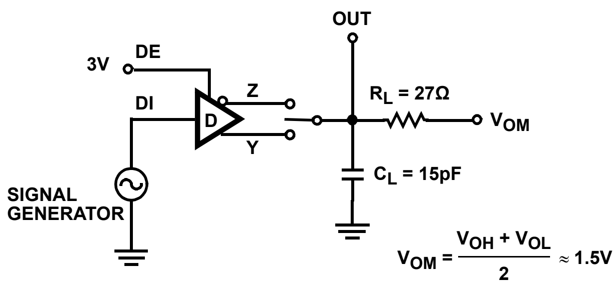
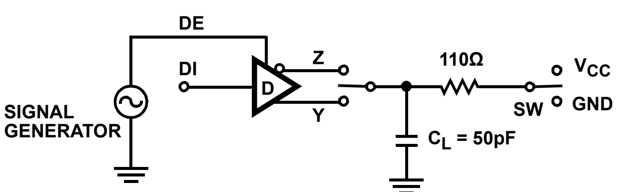


FIGURE 2C. SINGLE ENDED TEST CIRCUIT

FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER DATA RATE, PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW
t_{HZ}	Y/Z	X	1/0	GND
t_{LZ}	Y/Z	X	0/1	V_{CC}
t_{ZH}	Y/Z	0 (Note 8)	1/0	GND
t_{ZL}	Y/Z	0 (Note 8)	0/1	V_{CC}
$t_{ZH(SHDN)}$	Y/Z	1 (Note 11)	1/0	GND
$t_{ZL(SHDN)}$	Y/Z	1 (Note 11)	0/1	V_{CC}

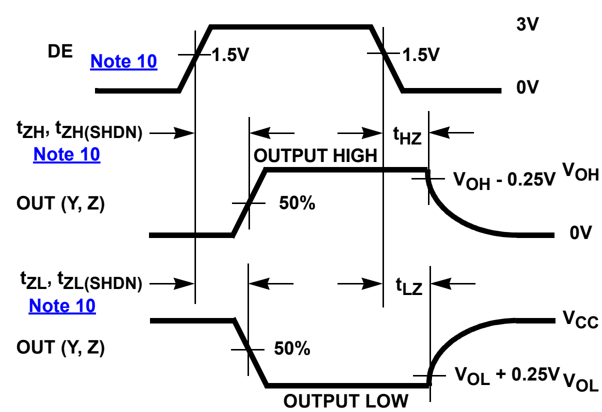


FIGURE 3A. TEST CIRCUIT

FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

Test Circuits and Waveforms (Continued)

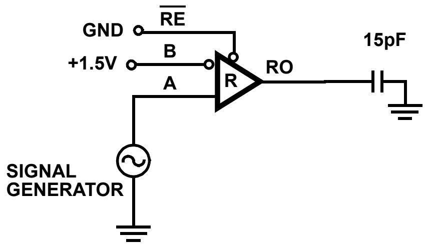


FIGURE 4A. TEST CIRCUIT

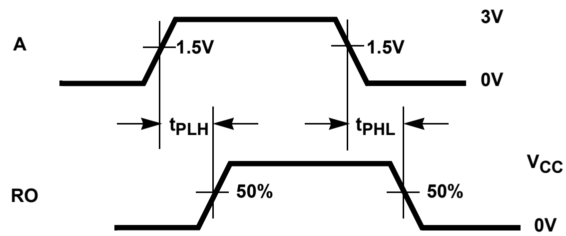
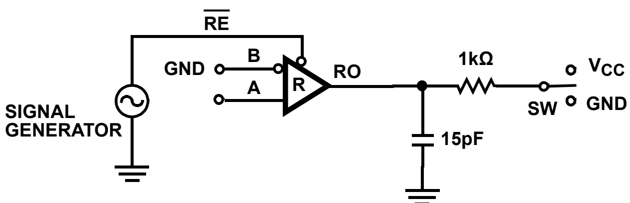


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER DATA RATE AND PROPAGATION DELAY



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 9)	0	+1.5V	GND
t_{ZL} (Note 9)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 12)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 12)	0	-1.5V	V_{CC}

FIGURE 5A. TEST CIRCUIT

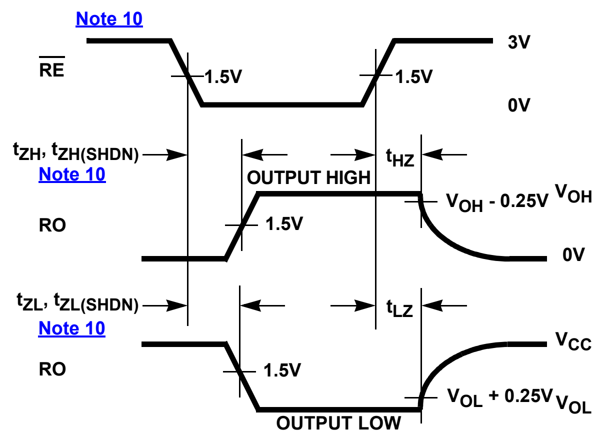


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus assuming one unit load devices. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

An important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000ft, so the wide CMR is necessary to handle ground potential differences and voltages induced in the cable by external fields.

Receiver Features

This device uses a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS422 and RS-485 specifications.

Receiver input impedance surpasses the RS-422 specification of 4kΩ and meets the RS-485 “Unit Load” requirement of 12kΩ minimum.

Receiver inputs function with common-mode voltages as great as +9V/-7V outside the power supplies (such as +12V and -7V), making them ideal for long networks in which induced voltages are a realistic concern.

All the receivers include a “fail-safe if open” function that ensures a high level receiver output if the receiver inputs are unconnected (floating).

The receiver easily meets the data rate supported by the driver, and the receiver output is tri-statable through the active low $\overline{RE}$ input.

Driver Features

The RS-485, RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422) even with V_{CC} = 3V. The driver features low propagation delay skew to maximize bit width and to minimize EMI, and it is tri-statable using the active high DE input.

Outputs of the ISL43485 driver are not slew rate limited, so faster output transition times allow data rates of at least 30Mbps.

Data Rate, Cables, and Terminations

Twisted pair cable is the cable of choice for RS-485, RS-422 networks. Twisted pair cables pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in this IC.

RS-485, RS-422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. Devices operating at 30Mbps are often limited to lengths of less than 100ft. Figure 6 on page 9 details the ISL43485's 30Mbps performance driving 200ft of "CAT5" cable terminated in 120Ω at both ends. Note that the differential signal delivered to the receiver at the end of the cable (A-B) still exceeds the 1.5V peak. Longer cable lengths are possible by reducing the data rate, as shown in Figure 7 on page 9 for a data rate of 20Mbps.

To minimize reflections, proper termination is imperative when using this 30Mbps device. In point-to-point or point-to-multipoint (single driver on bus) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, keep stubs connecting receivers to the main cable as short as possible. In multipoint (multi-driver) systems, terminate the main cable in its characteristic impedance at both ends. Keep stubs connecting a transceiver to the main cable as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. The ISL43485 meets this requirement through the driver output short-circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. Additionally, it uses a foldback circuit which reduces the short-circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short-circuit condition, this device's thermal shutdown feature disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically reenable after the die temperature drops about 15°. If the contention persists, the thermal shutdown/reenable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode

This BiCMOS transceiver uses a fraction of the power required by its bipolar counterparts. However, the ISL43485 includes a shutdown feature that reduces the already low quiescent I_{CC} to a 15nA trickle. They enter shutdown whenever the receiver and driver are ***simultaneously*** disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 300ns. Disabling both the driver and the receiver for less than 80ns ensures that shutdown is not entered.

Note that receiver and driver enable times increase when these devices enable from shutdown. Refer to Notes 8 through 12 on page 5 at the end of the Electrical Specification table for more information.

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C; unless otherwise specified

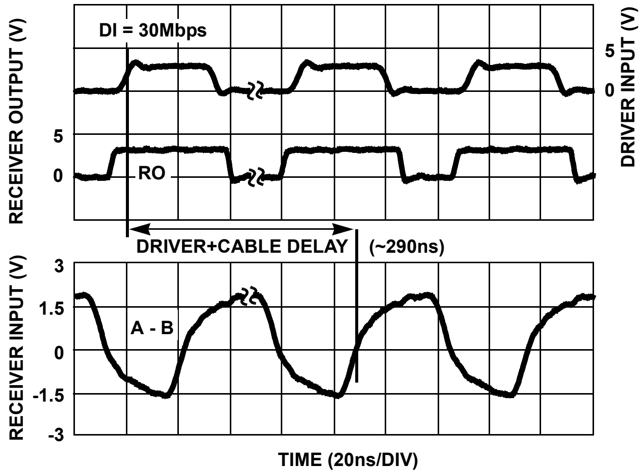


FIGURE 6. DRIVER AND RECEIVER WAVEFORMS DRIVING 200 FEET OF CAT5 CABLE (DOUBLE TERMINATED WITH 120Ω)

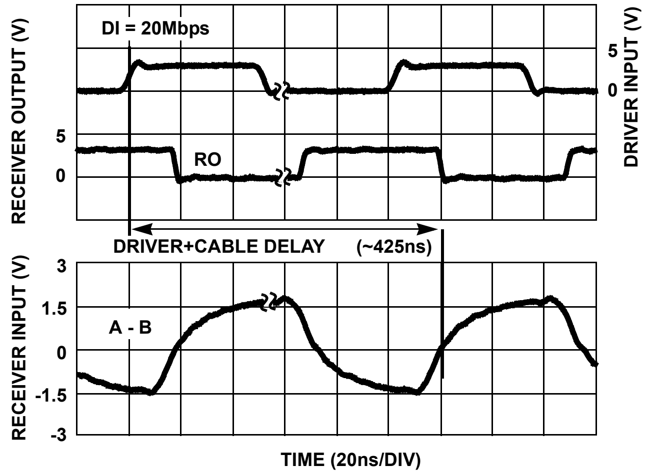


FIGURE 7. DRIVER AND RECEIVER WAVEFORMS DRIVING 300 FEET OF CAT5 CABLE (DOUBLE TERMINATED WITH 120Ω)

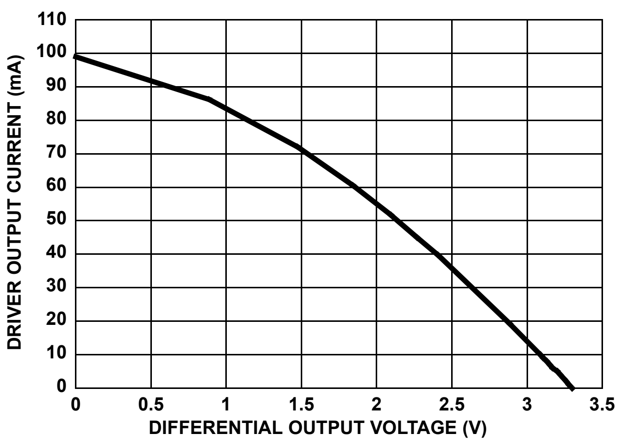


FIGURE 8. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

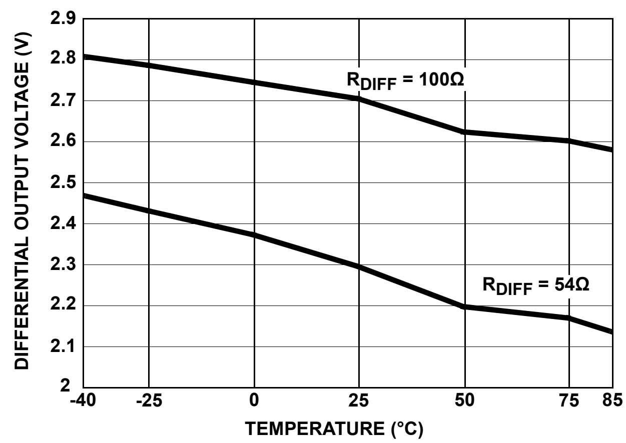


FIGURE 9. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

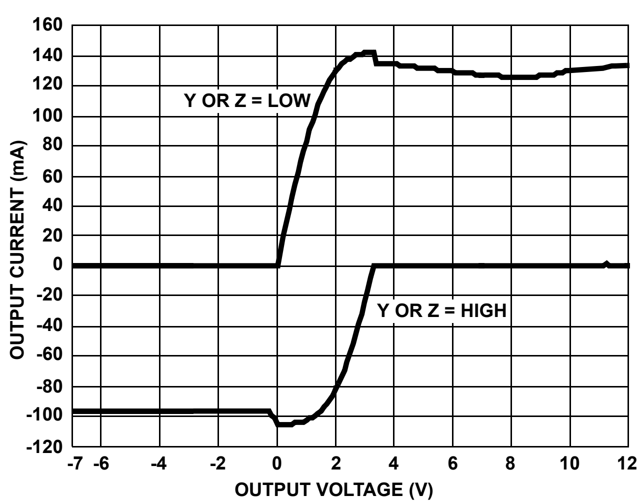


FIGURE 10. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

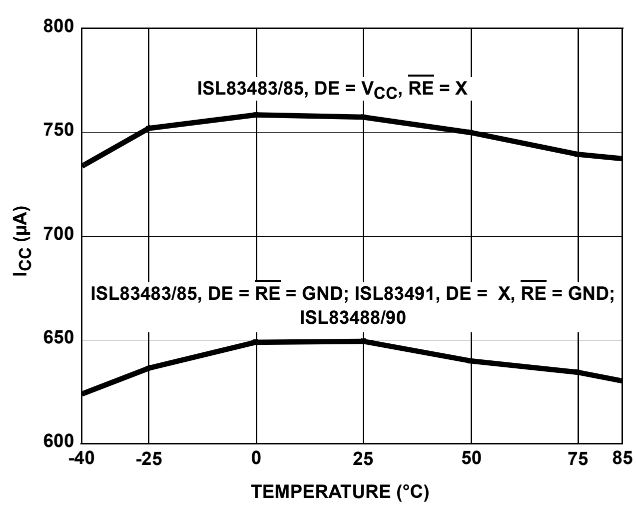


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C; unless otherwise specified **(Continued)**

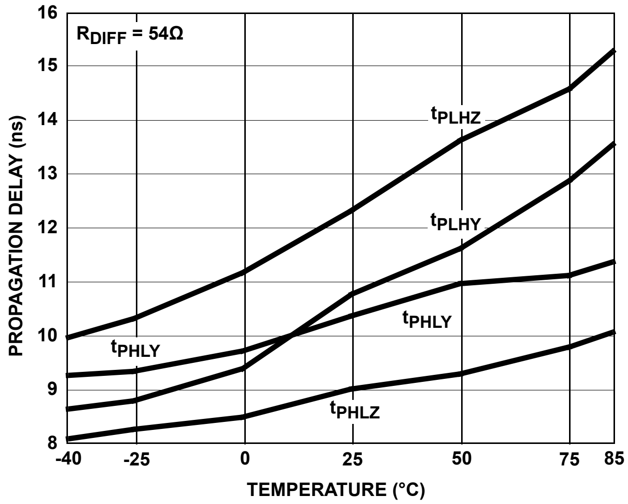


FIGURE 12. DRIVER PROPAGATION DELAY vs TEMPERATURE

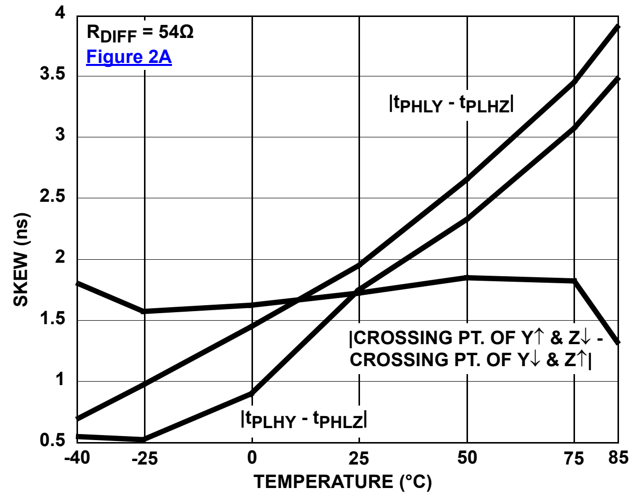


FIGURE 13. DRIVER SKEW vs TEMPERATURE

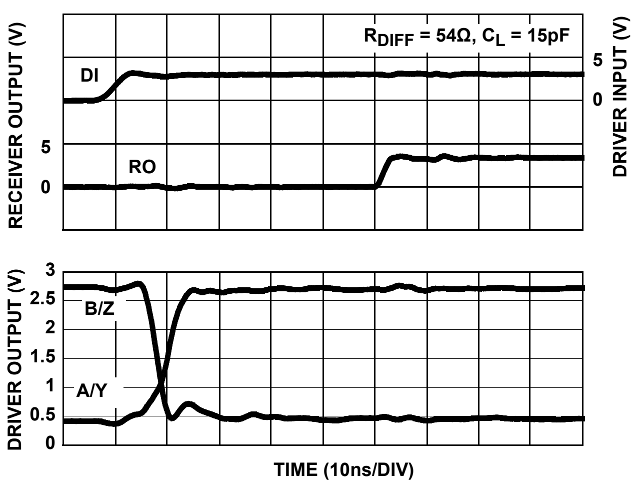


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH

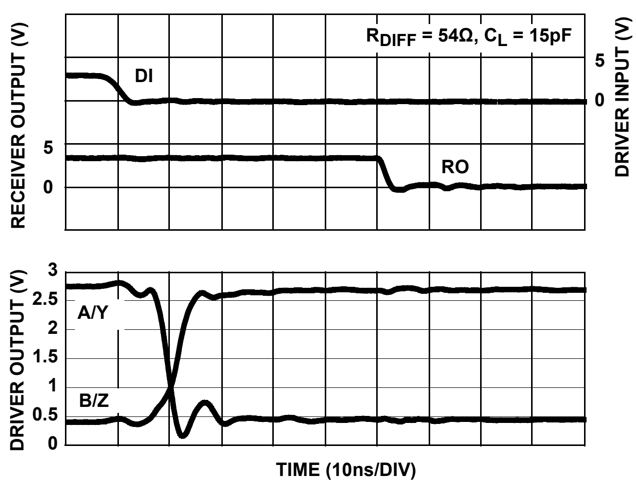


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

528

PROCESS:

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Sep 19, 2018	FN6071.2	Added Related Literature section. Updated Typical Application drawing and moved to page 1. Updated Ordering Information table by removing retired parts, adding Notes 1 and 3, adding Part Marking column, and adding Tape and Reel column. Moved Pinouts next to Pin Descriptions. Added Revision History and updated disclaimer. Updated POD M8.15 to latest revision changes are as follows: -Remove "u" symbol from drawing (overlaps the "a" on Side View). -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. -Changed the following in Typical Recommended Land Pattern: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Changed Note 1 “1982” to “1994”

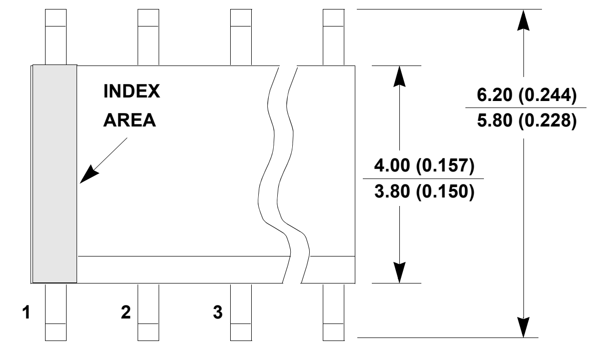
Package Outline Drawing

For the most recent package outline drawing, see [M8.15](M8.15).

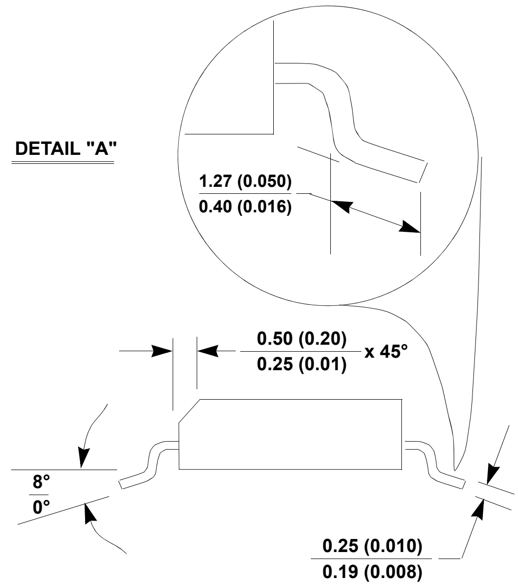
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

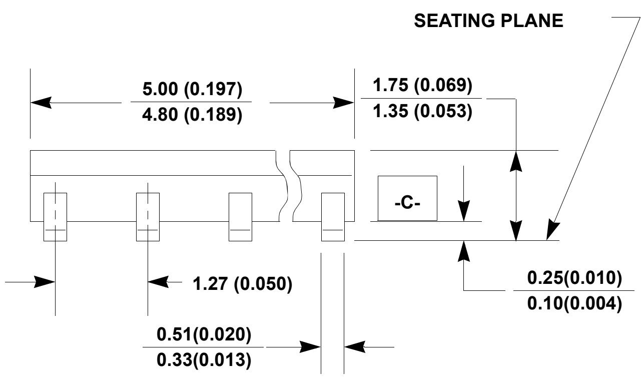
Rev 4, 1/12



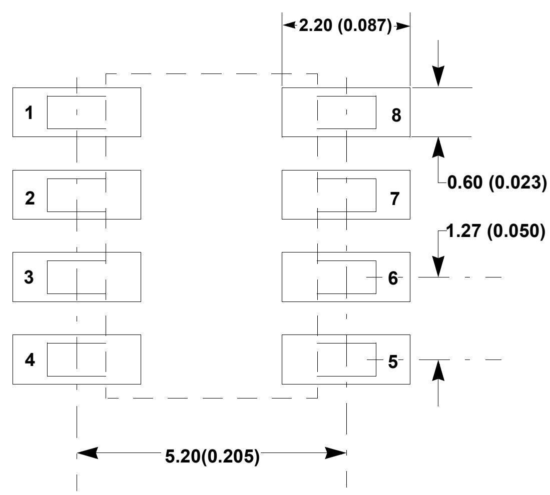
TOP VIEW



SIDE VIEW “B”



SIDE VIEW “A



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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Colophon 7.2