

ISL23315

Single, Low Voltage Digitally Controlled Potentiometer (XDCP)

Description

The ISL23315 is a volatile, low voltage, low noise, low power, I²C Bus™, 256 Taps, single digitally controlled potentiometer (DCP), which integrates DCP core, wiper switches and control logic on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers is controlled by the user through the I²C bus interface. The potentiometer has an associated volatile Wiper Register (WR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. When powered on, the ISL23315's wiper will always commence at mid-scale (128 tap position).

The low-voltage, low-power consumption, and small package of the ISL23315 make it an ideal choice for use in battery operated equipment. In addition, the ISL23315 has a VLOGIC pin allowing down to 1.2V bus operation, independent from the V_{CC} value. This allows for low logic levels to be connected directly to the ISL23315 without passing through a voltage level shifter.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 256 resistor taps
- I²C serial interface
 - No additional level translator for low bus supply
 - Two address pins allow up to four devices per bus
- Power supply
 - V_{CC} = 1.7V to 5.5V analog power supply
 - V_{LOGIC} = 1.2V to 5.5V I²C bus/logic power supply
- Wiper resistance: 70Ω typical at V_{CC} = 3.3V
- Shutdown Mode - forces the DCP into an end-to-end open circuit and RW is connected to RL through ~2kΩ internally
- Power-on preset to mid-scale (128 tap position)
- Shutdown and standby current 2.8μA max
- DCP terminal voltage from 0V to V_{CC}
- 100kΩ total resistance
- Extended industrial temperature range: -40°C to +125°C
- 10 Ld MSOP or 10 Ld uTQFN packages
- Pb-free (RoHS compliant)

Applications

- Power supply margining
- RF power amplifier bias compensation
- LCD bias compensation
- Laser diode bias compensation

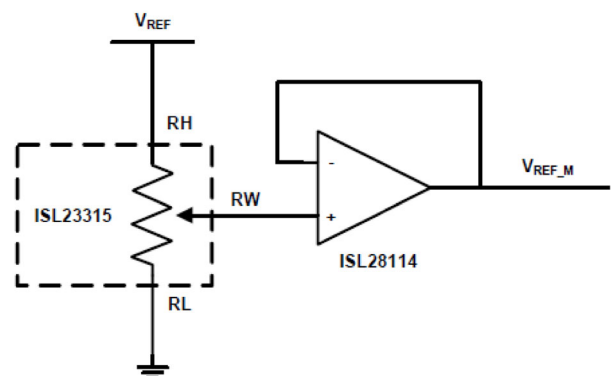


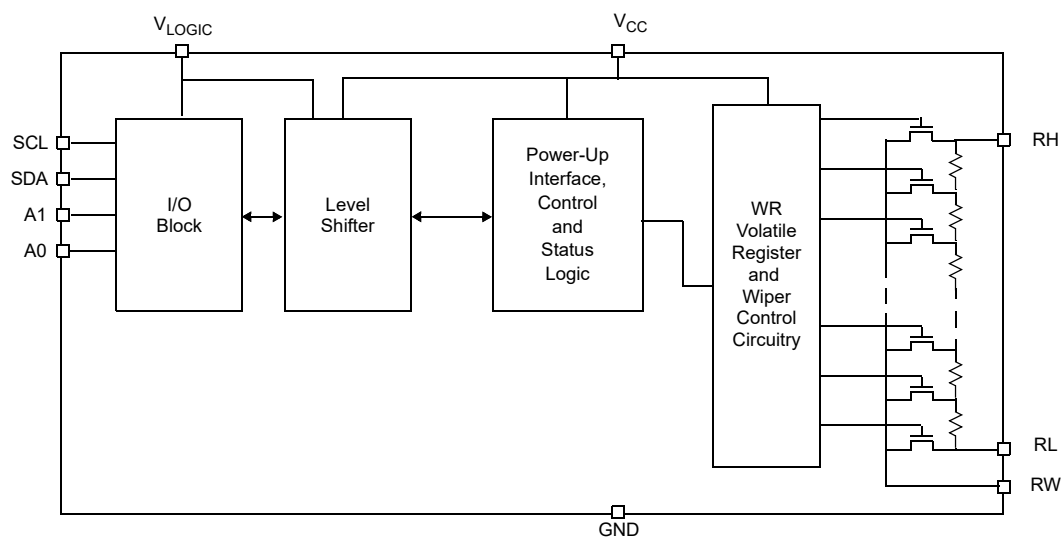
Figure 1. V_{REF} Adjustment

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1. Overview

1.1 Block Diagram



2. Pin Information

2.1 Pin Assignments

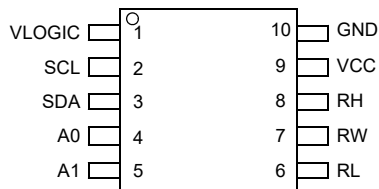


Figure 2. Pin Assignments - 10 Ld MSOP Top View

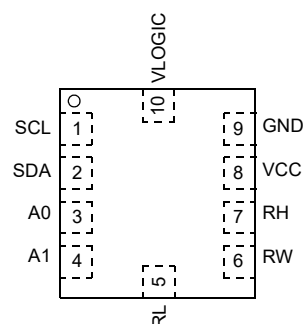


Figure 3. Pin Assignments - 10 Ld uTQFN Top View

2.2 Pin Descriptions

Pin Number		Pin Name	Description
MSOP	μTQFN		
1	10	VLOGIC	I ² C bus /logic supply. Range 1.2V to 5.5V
2	1	SCL	Logic Pin - Serial bus clock input
3	2	SDA	Logic Pin - Serial bus data input/open drain output
4	3	A0	Logic Pin - Hardwire slave address pin for I ² C serial bus. Range: V _{LOGIC} or GND
5	4	A1	Logic Pin - Hardwire slave address pin for I ² C serial bus. Range: V _{LOGIC} or GND
6	5	RL	DCP low terminal
7	6	RW	DCP wiper terminal
8	7	RH	DCP high terminal
9	8	VCC	Analog power supply. Range 1.7V to 5.5V
10	9	GND	Ground pin

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC	-0.3	+6.0	V
VLOGIC	-0.3	+6.0	V
Voltage on Any DCP Terminal Pin	-0.3	+6.0	V
Voltage on Any Digital Pins	-0.3	+6.0	V
Wiper current I_W (10s)	-6	6	mA
All Other Pins	GND - 0.3	$V_{CC} = 0.3$	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JESD22-A114E)	-	6500	V
Charged Device Model (Tested per JESD22-C101)	-	1000	V
Machine Model (Tested per JESD22-A115-A)	-	200	V
Latch-Up (Tested per JESD78B; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Operating Temperature Range	-40	125	°C
VCC Supply Voltage	1.7	5.5	V
VLOGIC Supply Voltage	1.2	5.5	V
DCP Terminal Voltage	0	VCC	V
Max Wiper Current	-3	3	mA

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	10 Ld MSOP Package	$\theta_{JA}^{[1]}$	Junction to ambient	170	°C/W
		$\theta_{JC}^{[2]}$	Junction to case	70	°C/W
Thermal Resistance	10 Ld uTQFN Package	$\theta_{JA}^{[1]}$	Junction to ambient	145	°C/W
		$\theta_{JC}^{[2]}$	Junction to case	90	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See [TB379](#) for details.

2. For θ_{JC} , the case temperature location is the center top of the package.

3.4 Analog Specifications

$V_{CC} = 2.7V$ to $5.5V$, $V_{LOGIC} = 1.2V$ to $5.5V$ across recommended operating conditions unless otherwise stated. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+125^{\circ}C$.**

Parameter	Symbol	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
R_H to R_L Resistance	R_{TOTAL}	T option	-	100	-	k Ω
R_H to R_L Resistance Tolerance		T option	-20	± 2	+20	%
End-to-End Temperature Coefficient		T option	-	70	-	ppm/ $^{\circ}C$
DCP Terminal Voltage	V_{RH}, V_{RL}	V_{RH} or V_{RL} to GND	0	-	V_{CC}	V
Wiper Resistance	R_W	R_H - floating, $V_{RL} = 0V$, force I_W current to the wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$, $V_{CC} = 2.7V$ to $5.5V$	-	70	200	Ω
		$V_{CC} = 1.7V$	-	580	-	Ω
Terminal Capacitance	$C_H/C_L/C_W$	See DCP Macro Model	-	32	-	pF
Leakage on DCP Pins	I_{LkgDCP}	Voltage at pin from GND to V_{CC}	-0.4	< 0.1	0.4	μA
Resistor Noise Density	Noise	Wiper at middle point, T option	-	61	-	nV/ $\sqrt{Hz}$
Digital Feed-Through from Bus to Wiper	Feed Thru	Wiper at middle point	-	-65	-	dB
Power Supply Reject Ratio	PSRR	Wiper output change if V_{CC} change $\pm 10\%$; wiper at middle point	-	-75	-	dB
Voltage Divider Mode (0V at R_L; V_{CC} at R_H; measured at R_W, unloaded)						
Integral Non-linearity, Guaranteed Monotonic	INL ^[3]	T option	-0.5	± 0.15	+0.5	LSB ^[4]
Differential Non-linearity, Guaranteed Monotonic	DNL ^[5]	T option	-0.4	± 0.1	+0.4	LSB ^[4]
Full-scale Error	FSError ^[6]	T option	-2	-0.5	0	LSB ^[4]
Zero-scale Error	ZSError ^[7]	T option	0	0.4	2	LSB ^[4]
Ratiometric Temperature Coefficient	TC_V ^[8]	T option, Wiper Register set to 80 hex	-	2.3	-	ppm/ $^{\circ}C$
Large Signal Wiper Settling Time	-	From code 0 to FF hex	-	300	-	ns
-3dB Cutoff Frequency	f_{cutoff}	Wiper at middle point T option	-	120	-	kHz
RHEOSTAT Mode (Measurements between R_W and R_L pins with R_H not connected, or between R_W and R_H with R_L not connected)						
Integral Non-linearity, Guaranteed Monotonic	R_{INL} ^[9]	T option; $V_{CC} = 2.7V$ to $5.5V$	-1.0	± 0.3	+1.0	M l ^[10]
		T option; $V_{CC} = 1.7V$	-	2.1	-	M l ^[10]
Differential Non-linearity, Guaranteed Monotonic	R_{DNL} ^[11]	T option; $V_{CC} = 2.7V$ to $5.5V$	-0.5	± 0.15	+0.5	M l ^[10]
		T option; $V_{CC} = 1.7V$	-	± 0.35	-	M l ^[10]
Offset, Wiper at 0 Position	R_{offset} ^[12]	T option; $V_{CC} = 2.7V$ to $5.5V$	0	0.5	2	M l ^[10]
		T option; $V_{CC} = 1.7V$	-	1.1	-	M l ^[10]
Resistance Temperature Coefficient	TCR ^[13]	T option; Wiper register set between 32 hex and FF hex	-	75	-	ppm/ $^{\circ}C$

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

2. Typical values are for $T_A = +25^{\circ}C$ and 3.3V supply voltages.

3. $INL = [V(RW)_i - i \times LSB - V(RW)_0]/LSB$ for $i = 1$ to 255.

4. $LSB = [V(RW)_{255} - V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are $V(RW)$ for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.

5. $DNL = [V(RW)_i - V(RW)_{i-1}]/LSB - 1$, for $i = 1$ to 255. i is the DCP register setting.

6. FS error = $[V(RW)_{255} - V_{CC}]/LSB$.

7. ZS error = $V(RW)_0/LSB$.

8. $TC_V = \frac{\text{Max}(V(RW)_i) - \text{Min}(V(RW)_i)}{V(RW)_i(+25^{\circ}C)} \times \frac{10^6}{+165^{\circ}C}$

For $i = 16$ to 255 decimal, $T = -40^{\circ}C$ to $+125^{\circ}C$. $\text{Max}()$ is the maximum value of the wiper voltage and $\text{Min}()$ is the minimum value of the wiper voltage over the temperature range.

9. $R_{INL} = [RW_i - (MI \cdot i) - RW_0]/MI$, for $i = 16$ to 255 .
10. $MI = |RW_{255} - RW_0|/255$. MI is a minimum increment. RW_{255} and RW_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
11. $R_{DNL} = (RW_i - RW_{i-1})/MI - 1$, for $i = 16$ to 255 .
12. $R_{offset} = RW_0/MI$, when measuring between RW and RL .
 $R_{offset} = RW_{255}/MI$, when measuring between RW and RH .
13. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{Ri(+25^{\circ}C)} \times \frac{10^6}{+165^{\circ}C}$

For $i = 16$ to 255 , $T = -40^{\circ}C$ to $+125^{\circ}C$. $Max()$ is the maximum value of the resistance and $Min()$ is the minimum value of the resistance over the temperature range.

3.5 Operating Specifications

$V_{CC} = 2.7V$ to $5.5V$, $V_{LOGIC} = 1.2V$ to $5.5V$ across recommended operating conditions unless otherwise stated. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+125^{\circ}C$.**

Parameter	Symbol	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
V_{LOGIC} Supply Current (Write/Read)	I_{LOGIC}	$V_{LOGIC} = 5.5V$, $V_{CC} = 5.5V$, $f_{SCL} = 400$ kHz (for I ² C active read and write)	-	-	200	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, $f_{SCL} = 400$ kHz (for I ² C active read and write)	-	-	5	μA
V_{CC} Supply Current (Write/Read)	I_{CC}	$V_{LOGIC} = 5.5V$, $V_{CC} = 5.5V$	-	-	18	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$	-	-	10	μA
V_{LOGIC} Standby Current	$I_{LOGIC\ SB}$	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby	-	-	1.3	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby	-	-	0.4	μA
V_{CC} Standby Current	$I_{CC\ SB}$	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby	-	-	1.5	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby	-	-	1	μA
V_{LOGIC} Shutdown Current	$I_{LOGIC\ SHDN}$	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby	-	-	1.3	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby	-	-	0.4	μA
V_{CC} Shutdown Current	$I_{CC\ SHDN}$	$V_{LOGIC} = V_{CC} = 5.5V$, I ² C interface in standby	-	-	1.5	μA
		$V_{LOGIC} = 1.2V$, $V_{CC} = 1.7V$, I ² C interface in standby	-	-	1	μA
Wiper Response Time	t_{DCP}	T option; SCL rising edge of the acknowledge bit after data byte to wiper new position from 10% to 90% of the final value.	-	3.5	-	μs
Leakage Current, at Pins A0, A1, SDA, SCL	I_{LkgDig}	Voltage at pin from GND to V_{LOGIC}	-0.4	<0.1	0.4	μA
DCP Recall Time from Shutdown Mode	$t_{ShdnRec}$	SCL rising edge of the acknowledge bit after ACR data byte to wiper recalled position and RH connection	-	1.5	-	μs
V_{CC} , V_{LOGIC} Ramp Rate	V_{CC} , V_{LOGIC} Ramp ^[3]	Ramp monotonic at any level	0.01	-	50	V/ms

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Typical values are for $T_A = +25^{\circ}C$ and 3.3V supply voltages.
3. Renesas recommends ramping up both the V_{LOGIC} and the V_{CC} supplies at the same time. If this is not possible, Renesas recommends ramping up V_{LOGIC} first followed by V_{CC} .

3.6 Serial Interface Specifications

For SCL, SDA, A0, A1 Unless Otherwise Noted.

Parameter	Symbol	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
Input LOW Voltage	V_{IL}	-	-0.3	-	$0.3 \times V_{LOGIC}$	V
Input HIGH Voltage	V_{IH}	-	$0.7 \times V_{LOGIC}$	-	$V_{LOGIC} + 0.3$	V
SDA and SCL Input Buffer Hysteresis	Hysteresis	$V_{LOGIC} > 2V$	$0.05 \times V_{LOGIC}$	-	-	V
		$V_{LOGIC} < 2V$	$0.1 \times V_{LOGIC}$	-	-	
SDA Output Buffer LOW Voltage	V_{OL}	$I_{OL} = 3mA, V_{LOGIC} > 2V$	0	-	0.4	V
		$I_{OL} = 1.5mA, V_{LOGIC} < 2V$	-	-	$0.2 \times V_{LOGIC}$	V
SDA, SCL Pin Capacitance	C_{pin}	-	-	10	-	pF
SCL Frequency	f_{SCL}	-	-	-	400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{sp}	Any pulse narrower than the max spec is suppressed	-	-	50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling edge crossing 30% of V_{LOGIC} , until SDA exits the 30% to 70% of V_{LOGIC} window	-	-	900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing 70% of V_{LOGIC} during a STOP condition, to SDA crossing 70% of V_{LOGIC} during the following START condition	1300	-	-	ns
Clock LOW Time	t_{LOW}	Measured at the 30% of V_{LOGIC} crossing	1300	-	-	ns
Clock HIGH Time	t_{HIGH}	Measured at the 70% of V_{LOGIC} crossing	600	-	-	ns
START Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge; both crossing 70% of V_{LOGIC}	600	-	-	ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{LOGIC} to SCL falling edge crossing 70% of V_{LOGIC}	600	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{LOGIC} window, to SCL rising edge crossing 30% of V_{LOGIC}	100	-	-	ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0	-	-	ns
STOP Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{LOGIC} , to SDA rising edge crossing 30% of V_{LOGIC}	600	-	-	ns
STOP Condition Hold Time for Read or Write	$t_{HD:STO}$	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300	-	-	ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing 30% of V_{LOGIC} , until SDA enters the 30% to 70% of V_{LOGIC} window. $I_{OL} = 3mA, V_{LOGIC} > 2V$. $I_{OL} = 1.5mA, V_{LOGIC} < 2V$	0	-	-	ns
SDA and SCL Rise Time	t_R	From 30% to 70% of V_{LOGIC}	$20 + 0.1 \times C_b$	-	250	ns
SDA and SCL Fall Time	t_F	From 70% to 30% of V_{LOGIC}	$20 + 0.1 \times C_b$	-	250	ns
Capacitive Loading of SDA or SCL	C_b	Total on-chip and off-chip	10	-	400	pF
A1, A0 Setup Time	$t_{SU:A}$	Before START condition	600	-	-	ns
A1, A0 Hold Time	$t_{HD:A}$	After STOP condition	600	-	-	ns

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

2. Typical values are for $T_A = +25^\circ C$ and 3.3V supply voltages.

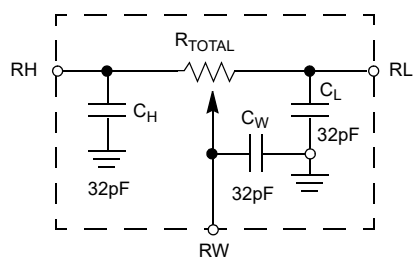


Figure 4. DCP Macro Model

4. Timing Diagrams

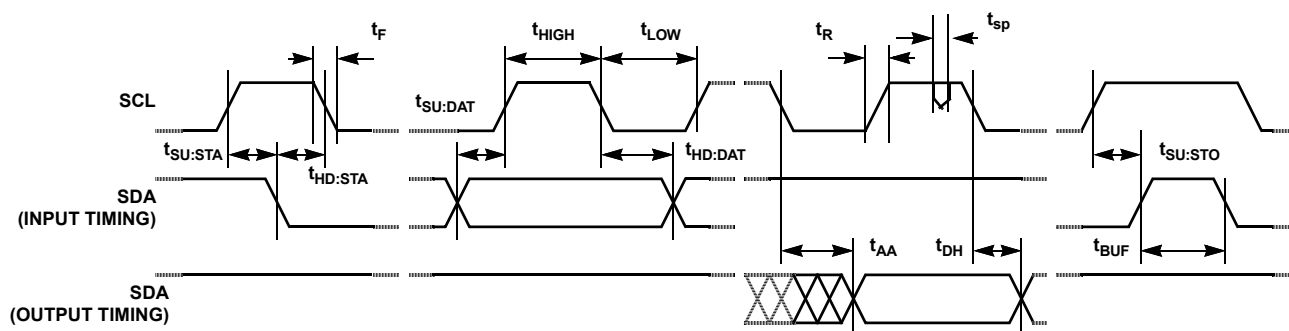


Figure 5. SDA vs SCL Timing

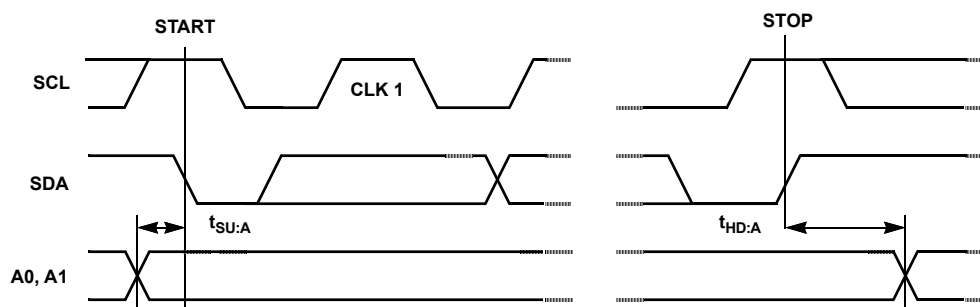


Figure 6. A0 and A1 Pin Timing

5. Typical Performance Curves

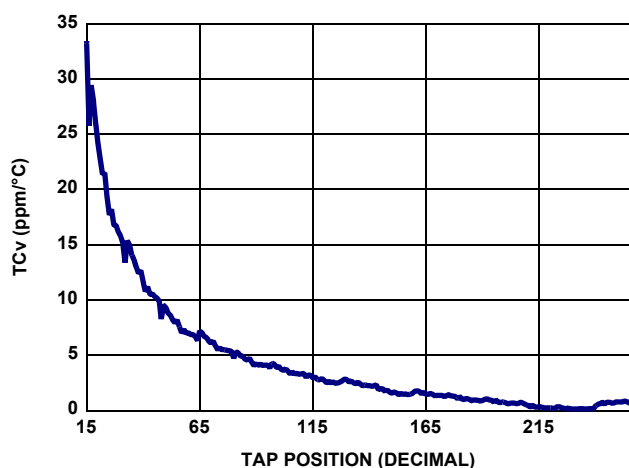


Figure 7. 100k TCv vs Tap Position

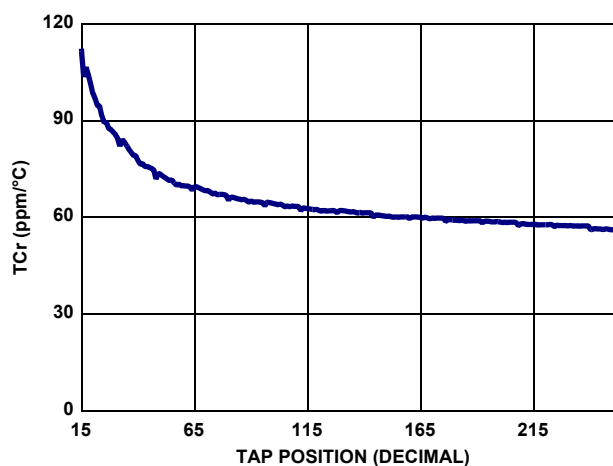


Figure 8. 100k TCr vs Tap Position

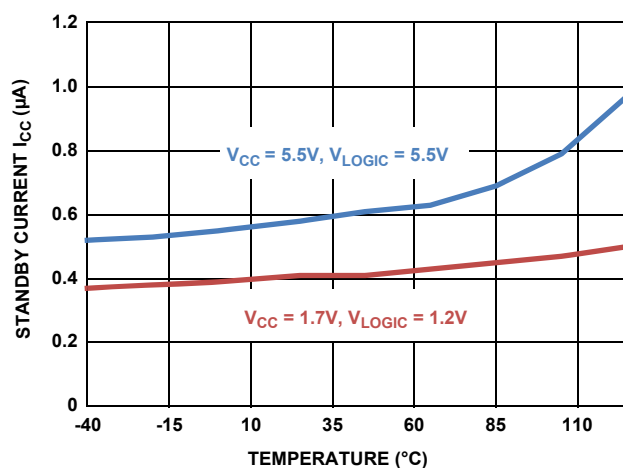


Figure 9. Standby Current vs Temperature

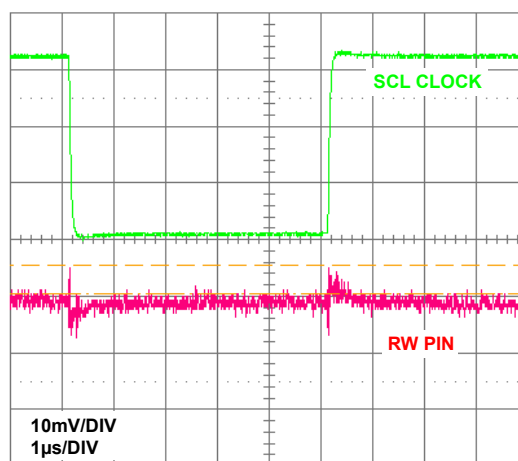


Figure 10. Wiper Digital Feed-Through

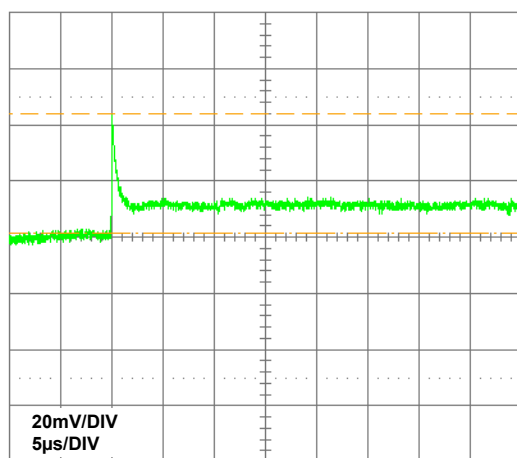


Figure 11. Wiper Transition Glitch

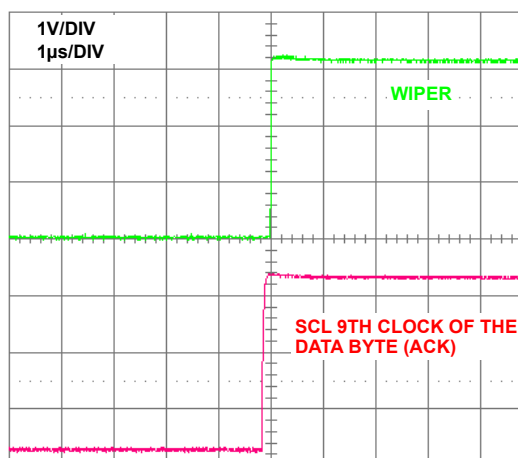


Figure 12. Wiper Large Signal Settling Time

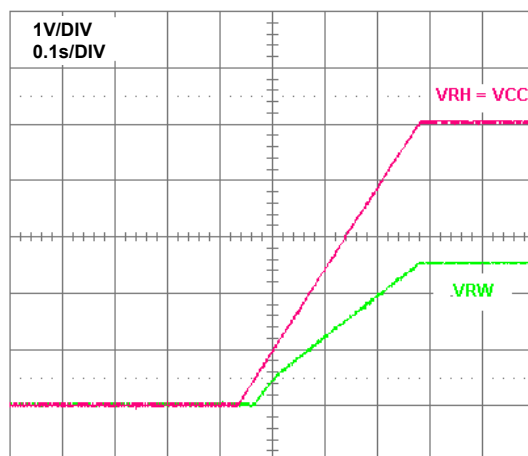


Figure 13. Power-On Start-Up in Voltage Divider Mode

6. Functional Pin Descriptions

6.1 Potentiometers Pins

6.1.1 RH and RL

The high (R_H) and low (R_L) terminals of the ISL23315 are equivalent to the fixed terminals of a mechanical potentiometer. R_H and R_L are referenced to the relative position of the wiper and not the voltage on the terminals. With WR set to 255 decimal, the wiper will be closest to R_H , and with the WR set to 0, the wiper is closest to R_L .

6.1.2 RW

RW is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

6.2 Bus Interface Pins

6.2.1 Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for I²C interface. It receives device address, wiper address and data from an I²C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

6.2.2 Serial Clock (SCL)

This input is the serial clock of the I²C serial interface. SCL requires an external pull-up resistor, since the master's SCL output is typically an open drain.

6.2.3 Device Address (A1, A0)

The address inputs are used to set the least significant 2 bits of the 7-bit I²C interface slave address. The slave address bits in the serial data stream must match the address input pins to initiate communication with the ISL23315. A maximum of four ISL23315 devices may occupy the I²C serial bus (see Table 3).

6.2.4 V_{LOGIC}

This input pin supplies the internal level translator for serial bus operation from 1.2V to 5.5V.

7. Principles of Operation

The ISL23315 is an integrated circuit incorporating one DCP with its associated registers and an I²C serial interface providing direct communication between a host and the potentiometer. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a make-before-break mode when the wiper changes tap positions.

Voltage at any DCP pins, R_H, R_L or R_W, should not exceed V_{CC} level under any conditions during power-up and normal operation.

The V_{LOGIC} pin needs to be connected to the I²C bus supply which allows reliable communication with a wide range of microcontrollers, independently of V_{CC}. This is extremely important in systems where the master supply has lower levels than DCP analog supply.

7.1 DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The R_W pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[7:0] = 00h), its wiper terminal (R_W) is closest to its “Low” terminal (R_L). When the WR register of a DCP contains all ones (WR[7:0] = FFh), its wiper terminal (R_W) is closest to its “High” terminal (R_H). As the value of the WR increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to R_L to the position closest to R_H. At the same time, the resistance between R_W and R_L increases monotonically, while the resistance between R_H and R_W decreases monotonically.

While the ISL23315 is being powered up, the WR is reset to 80h (128 decimal), which locates R_W roughly at the center between R_L and R_H.

The WR can be read or written to directly using the I²C serial interface as described in the following sections.

7.2 Memory Description

The ISL23315 contains two volatile 8-bit registers: Wiper Register (WR) and Access Control Register (ACR). The memory map of ISL23315 is shown in Table 1. The Wiper Register (WR) at address 0 contains current wiper position.

Table 1. Memory Map

Address (hex)	Volatile Register Name	Default Setting (hex)
10	ACR	40
0	WR	80

The Access Control Register (ACR) at address 10h contains information and control bits described in Table 2.

Table 2. Access Control Register (ACR)

Bit #	7	6	5	4	3	2	1	0
Name/value	0	SHDN	0	0	0	0	0	0

7.3 Shutdown Function

The $\overline{\text{SHDN}}$ bit (ACR[6]) disables or enables shutdown mode for all the DCP channels simultaneously. When this bit is 0, the DCP is forced to end-to-end open circuit and RW is connected to RL through a 2k Ω series resistor, as shown in Figure 14. Default value of the $\overline{\text{SHDN}}$ bit is 1.

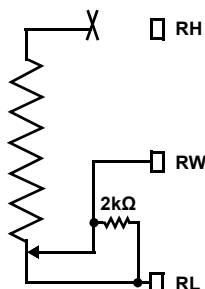


Figure 14. DCP Connection in Shutdown Mode

In the shutdown mode, the RW terminal is connected to RL through an approximately 2k Ω resistor, as shown in Figure 14. When the device enters shutdown, all current DCP WR settings are maintained. When the device exits shutdown, the wipers will return to the previous WR settings after a short settling time (see Figure 15).

In shutdown mode, if there is a glitch on the power supply which causes it to drop below 1.3V for more than 0.2 μs to 0.4 μs , the wipers will be RESET to their mid position. This is done to avoid an undefined state at the wiper outputs.

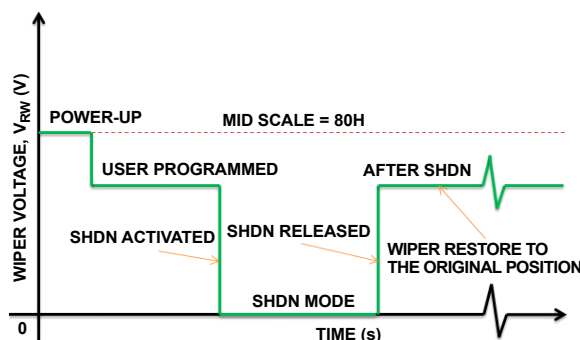


Figure 15. Shutdown Mode Wiper Response

7.4 I²C Serial Interface

The ISL23315 supports an I²C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL23315 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

7.5 Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 16). On power-up of the ISL23315, the SDA pin is in the input mode.

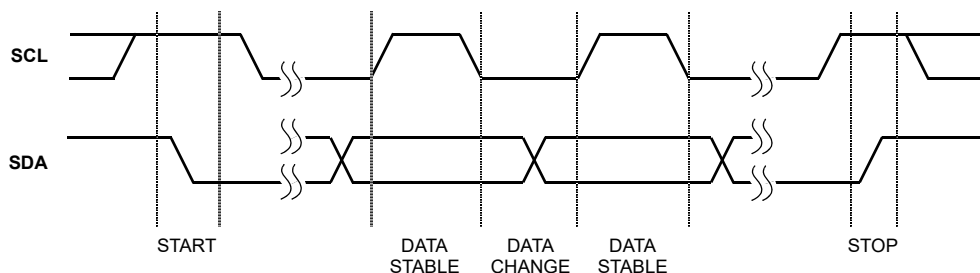


Figure 16. Valid Data Changes, Start and Stop Conditions

All I²C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The ISL23315 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 16). A START condition is ignored during the power-up of the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 16). A STOP condition at the end of a read operation or at the end of a write operation places the device in its standby mode.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 17).

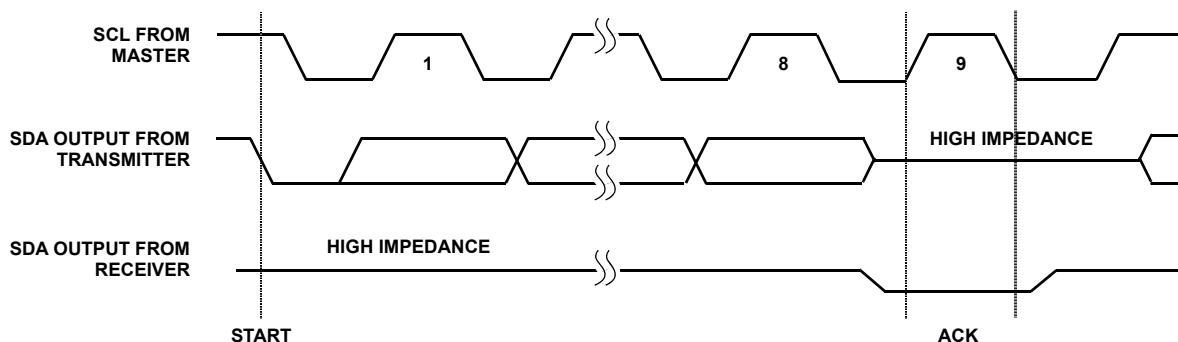


Figure 17. Acknowledge Response From Receiver

The ISL23315 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL23315 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 10100 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/Write bit. Its value is 1 for a Read operation and 0 for a Write operation (see Table 3).

Table 3. Identification Byte Format

1	0	1	0	0	A1 ^[1]	A0 ^[1]	R/W
(MSB)							(LSB)

1. Logic values at Pins A1 and A0, respectively.

7.6 Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL23315 responds with an ACK. The data is transferred from I²C block to the corresponding register at the 9th clock of the data byte and device enters its standby state (see Figure 17 and Figure 18).

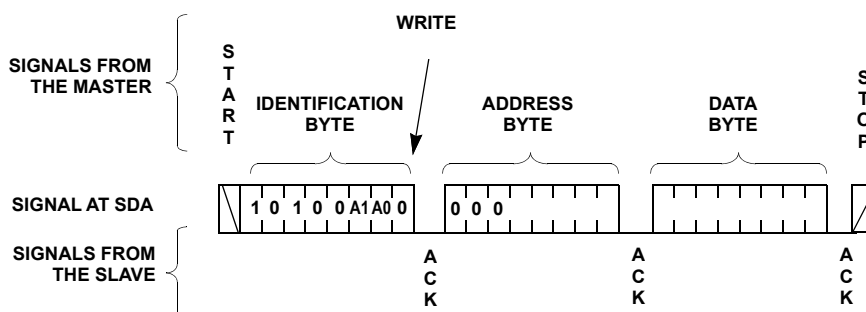


Figure 18. Byte Write Sequence

7.7 Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/W bit set to 0, an Address Byte, a second START, and a second Identification byte with the R/W bit set to 1. After each of the three bytes, the ISL23315 responds with an ACK; then the ISL23315 transmits Data Byte. The master terminates the read operation by issuing a NACK (ACK) and a STOP condition following the last bit of the last Data Byte (see Figure 19).

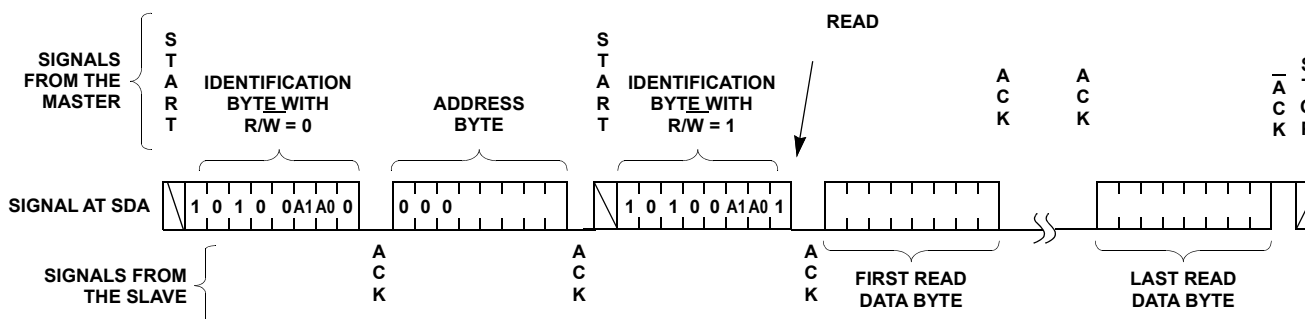


Figure 19. Read Sequence

8. Applications Information

8.1 V_{LOGIC} Requirements

It is recommended to keep V_{LOGIC} powered all the time during normal operation. In a case where turning V_{LOGIC} OFF is necessary, it is recommended to ground the V_{LOGIC} pin of the ISL23315. Grounding the V_{LOGIC} pin or both V_{LOGIC} and V_{CC} does not affect other devices on the same bus. It is good practice to put a 1μF capacitor in parallel with a 0.1μF decoupling capacitor as close to the V_{LOGIC} pin as possible.

8.2 V_{CC} Requirements and Placement

Renesas recommends placing a 1μF capacitor in parallel with a 0.1μF decoupling capacitor close to the V_{CC} pin.

8.3 Wiper Transition

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients, or overshoot/undershoot, resulting from the sudden transition from a very low impedance make to a much higher impedance break within a short period of time ($<1\mu\text{s}$). There are several code transitions such as 0Fh to 10h, 1Fh to 20h,..., EFh to FFh, produce larger transient glitches.

Note: All switching transients settle well within the settling time as stated in the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients. However, that also reduces the useful bandwidth of the circuit, therefore, it may not be a good solution for some applications. In such cases, use fast amplifiers in the signal chain for faster recovery.

9. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

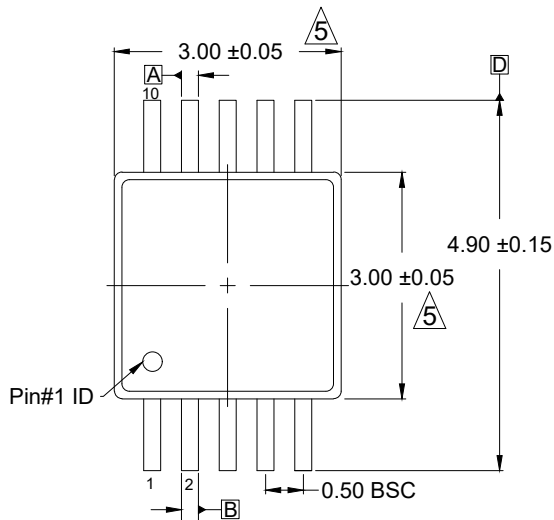
10. Ordering Information

Part Number ^[1]	Part Marking	Resistance Option (k Ω)	Package Description ^[2] (RoHS compliant)	Pkg. Dwg. #	Carrier Type ^[3]	Temp Range
ISL23315TFUZ ^[4]	3315T	100	10 Ld MSOP	M10.118	Tube	-40 to +125°C
ISL23315TFUZ-TK ^[4]	3315T	100	10 Ld MSOP	M10.118	Reel, 1K	-40 to +125°C
ISL23315TFRUZ-T7A ^[5]	HB	100	10 Ld 2.1×1.6 UTQFN	L10.2.1×1.6A	Reel, 250	-40 to +125°C
ISL23315TFRUZ-TK ^[5]	HB	100	10 Ld 2.1×1.6 UTQFN	L10.2.1×1.6A	Reel, 1K	-40 to +125°C

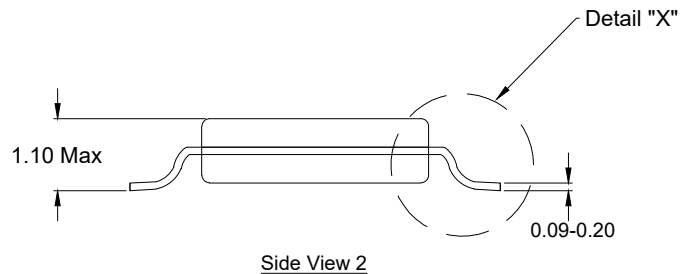
- For Moisture Sensitivity Level (MSL), see the [ISL23315](#) product page. For more information about MSL, see [TB363](#).
- For the Pb-Free Reflow Profile, see [TB493](#).
- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

11. Revision History

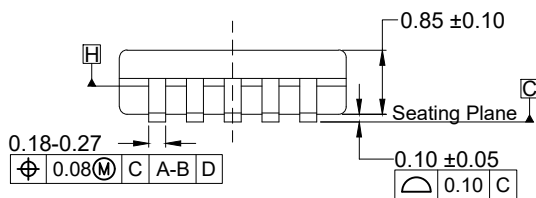
Revision	Date	Description
3.00	Oct 29, 2026	<ul style="list-style-type: none"> Applied latest template. Removed About Intersil section. Removed W (10k) and U (50k) versions as parts are obsolete. Updated POD M10.118 to the latest version; changes are as follows: <ul style="list-style-type: none"> Corrected typo in the side view 1 updating package thickness tolerance from ± 0.10 to ± 0.10.
2.00	Aug 12, 2015	<ul style="list-style-type: none"> Updated Ordering Information table. Changed Products section to About Intersil. Updated POD M10.118 from rev 0 to rev 1. Changes since rev0: Updated to new POD template. Added land pattern
1.00	Jul 29, 2011	<ul style="list-style-type: none"> Added "Shutdown Function" section and revised "VLOGIC Standby Current" and "VCC Shutdown Current" limits on page 6. On page 7, split "Wiper Response Time" up into 3 separate conditions for each option (W, U, T).
0.00	Dec 15, 2010	Initial release.



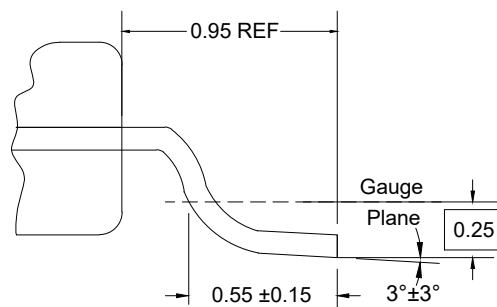
Top View



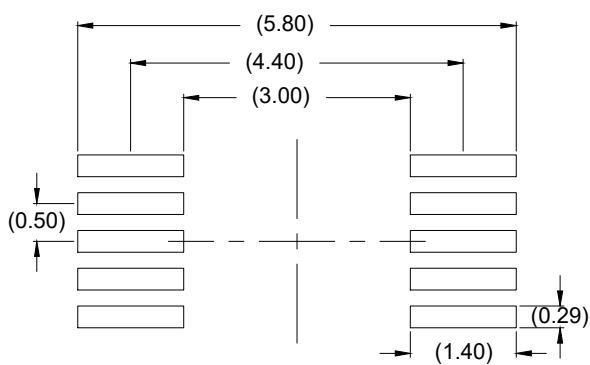
Side View 2



Side View 1



Detail "X"



Typical Recommended Land Pattern

Notes:

1. All Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and ASME Y14.5M-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in () are for reference only.

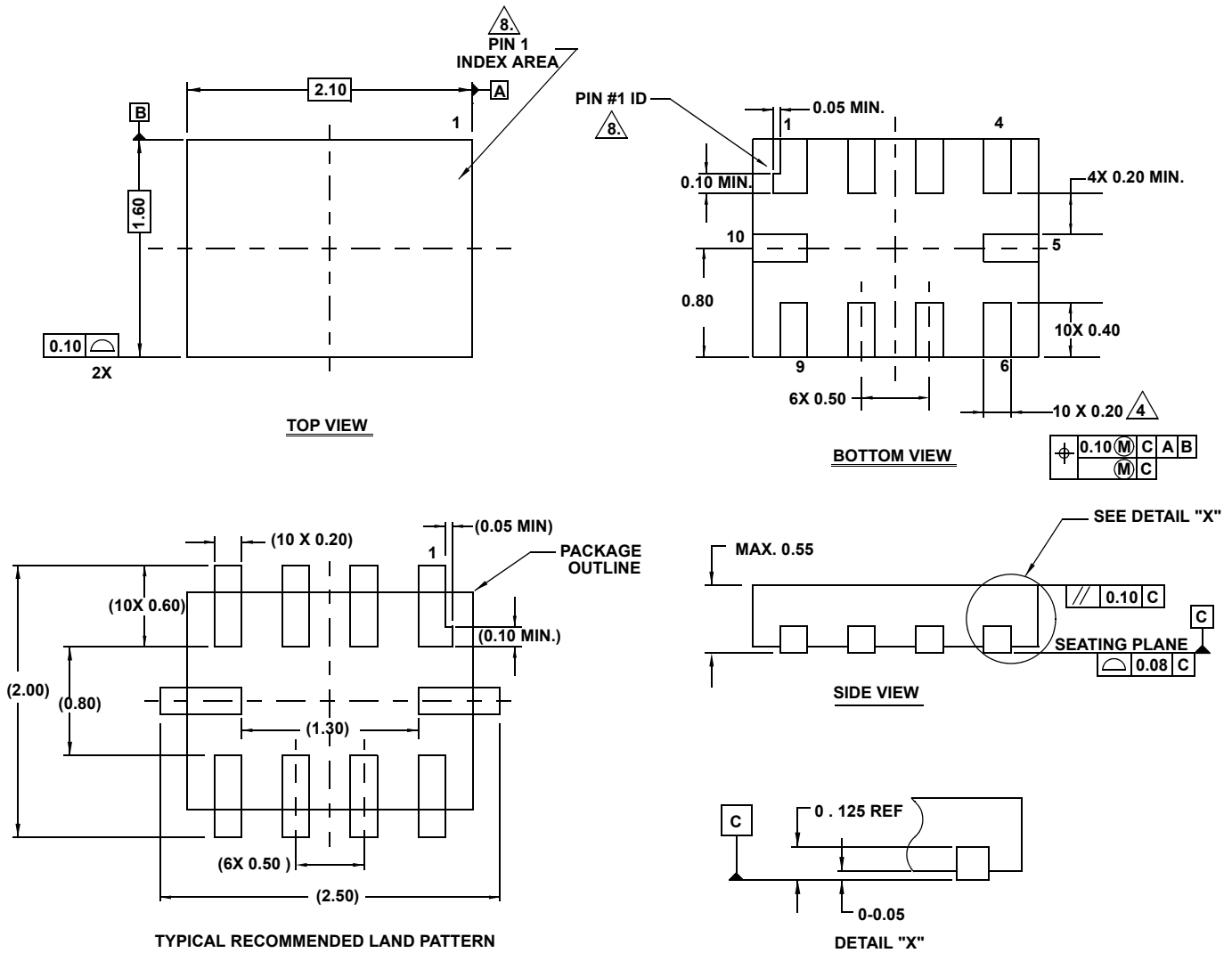
Plastic Packages for Integrated Circuits

Package Outline Drawing

L10.2.1X1.6A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

REV 5, 3/10



NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All Dimensions are in millimeters. Angles are in degrees. Dimensions in () for Reference Only.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Maximum package warpage is 0.05mm.
6. Maximum allowable burrs is 0.076mm in all directions.
7. Same as JEDEC MO-255UABD except:
No lead-pull-back, MIN. Package thickness = 0.45 not 0.50mm
Lead Length dim. = 0.45mm max. not 0.42mm.
8. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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