# ISL1561
Fixed Gain Dual Port Class-G Differential xDSL Line Driver

The ISL1561 is a fixed gain dual port class-G differential amplifier designed for driving full rate ADSL2+ and VDSL2 signals at very low power dissipation. The driver runs on a single +14V power supply and internally generates higher supply voltages when needed to enable power efficient operation for high peak-to-average ratio (PAR) ADSL2+ and VDSL2 signals.

In ADSL2+ mode of operation with full 19.8dBm transmit signal power across 100$\Omega$ line load, each port consumes only 520mW of power, while with 19.5dBm VDSL2 8b profile a port consumes 610mW of power. In VDSL2 17a mode of operation with 14.5dBm transmit power, a port will consume 411mW of power. These typical power consumption figures account for receiver hybrid loading effects and transformer losses.

The ISL1561 provides two ports of wideband, current feedback amplifiers optimized for low power consumption in xDSL systems. The drivers achieve an average upstream missing band power ratio (MBPR) distortion of better than -64dBc under 19.8dBm transmit signal power into 100$\Omega$ load. A three pin serial interface is used to program an 8-bit internal register to set each port's supply current with 0.5mA step size. This flexibility allows the DSP to optimize each port separately during modem training.

The device is supplied in a thermally-enhanced small footprint (4mmx4mm) 24 lead QFN package. The ISL1561 is specified for operation over the full -40°C to +85°C industrial temperature range and is Pb-free RoHS compliant.

## Features

- Internal fixed gain of 11.6V/V to transformer (see Figure 3)
- 360mA output drive capability
- 41.8V$_{P-P}$ differential output drive into 100$\Omega$ in class G mode
- VDSL2 8b profile MTPR of -64dBc
- VDSL2 17a profile MTPR of -60dBc
- ADSL2+, VDSL2 8b and 17a power consumption of 520mW, 610mW and 411mW respectively
- 8-bit programmable register to set supply current on each port
- 3 pin serial port interface

## Applications

- Dual port ADSL2+ and VDSL2 DSLAM

## Alternate Part
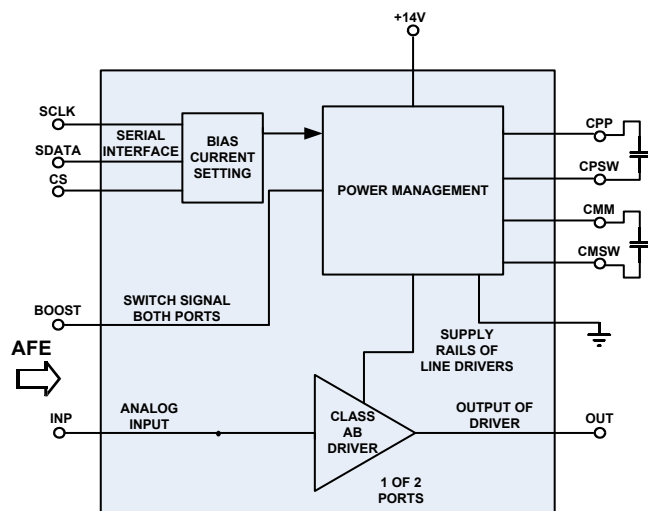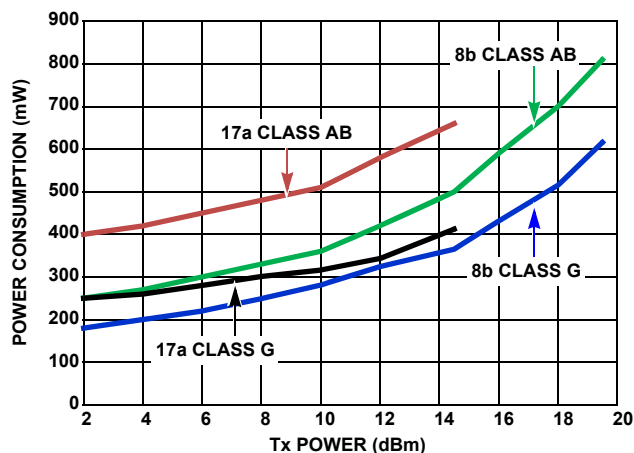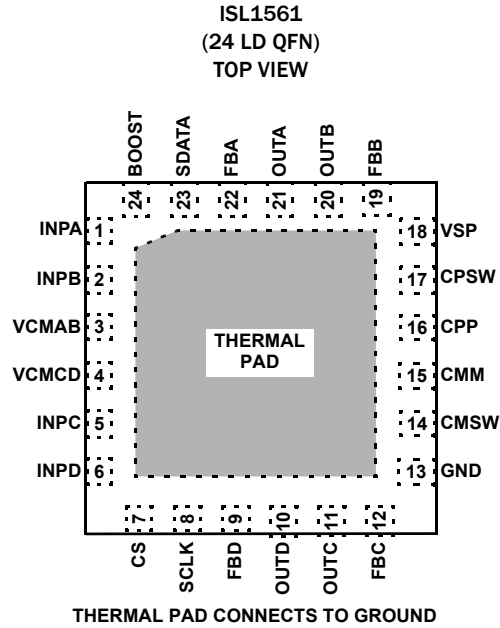
- ISL1591 Class AB VDSL Driver



FIGURE 1. BLOCK DIAGRAM



FIGURE 2. CLASS G+ vs CLASS AB DRIVER TOTAL POWER

# Pin Configuration

ISL1561
(24 LD QFN)
TOP VIEW



THERMAL PAD CONNECTS TO GROUND

# Pin Descriptions

| ISL1561 (24 Ld QFN) | PIN NAME | FUNCTION |
|---|---|---|
| 1 | INPA | Amplifier A non-inverting input |
| 2 | INPB | Amplifier B non-inverting input |
| 3 | VCMAB | Input common mode bias for port AB |
| 4 | VCMCD | Input common mode bias for port CD |
| 5 | INPC | Amplifier C non-inverting input |
| 6 | INPD | Amplifier D non-inverting input |
| 7 | CS | Chip select, low enables data input to logic |
| 8 | SCLK | Serial clock input |
| 9 | FBD | Feedback pin for amplifier D |
| 10 | OUTD | Amplifier D output |
| 11 | OUTC | Amplifier C output |
| 12 | FBC | Feedback pin for amplifier C |
| 13 | GND | Ground |
| 14 | CMSW | Internal negative boost supply |
| 15 | CMM | Internal negative supply |
| 16 | CPP | Internal positive supply |
| 17 | CPSW | Internal positive boost supply |
| 18 | VSP | Positive supply voltage |
| 19 | FBB | Feedback pin for amplifier B |
| 20 | OUTB | Amplifier B output |
| 21 | OUTA | Amplifier A output |
| 22 | FBA | Feedback pin for amplifier A |
| 23 | SDATA | Serial data write |
| 24 | BOOST | Class G control input |
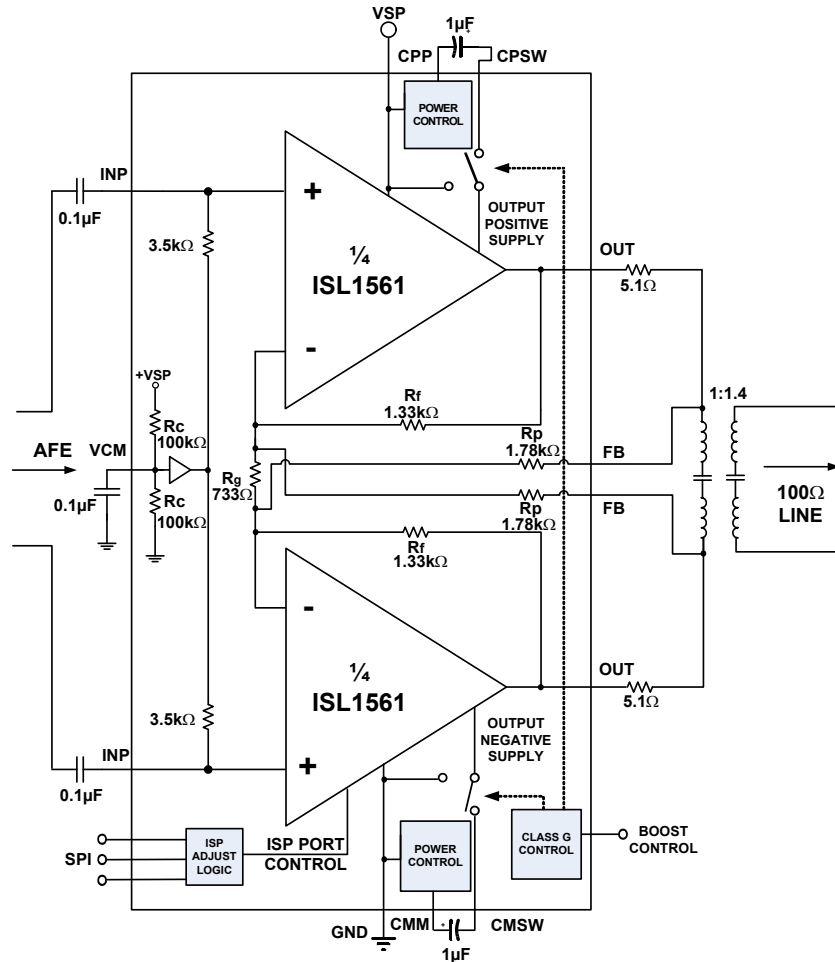
TYPICAL DIFFERENTIAL I/O LINE DRIVER (1 OF 2 PORTS)

**FIGURE 3. CONNECTION DIAGRAM**

# Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | OPERATING AMBIENT TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL1561IRZ | 15 61IRZ | -40 to +85 | 24 Ld QFN | L24.4x4H |
| ISL1561IRZ-T13 (Note 1) | 15 61IRZ | -40 to +85 | 24 Ld QFN | L24.4x4H |

NOTES:

1. Please refer to TB347 for details on reel specifications.

2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see device information page for ISL1561. For more information on MSL please see tech brief TB363.

RENESAS

## Absolute Maximum Ratings $(T_A = +25\degree C)$

$V_S+$ Voltage to GND . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-0.3V to +15V
Driver $V_{IN}+$ Voltage. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .GND to $V_S+$
SPI and Boost Pin Voltage to GND . . . . . . . . . . . . . . . . . . . . . . .-0.3V to +6V
$V_{CM}$ Voltage to GND . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .GND to $V_S+$
Current into any Input . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .8mA
Continuous Output Current for Long Term Reliability. . . . . . . . . . . . . . . .50mA
ESD Rating
   Human Body Model (Tested per JESD22-A114F). . . . . . . . . . . . . . . . . 3kV
   Machine Model (Tested per JESD22-A115C) . . . . . . . . . . . . . . . . . 300V
   Charge Device Model (Tested per JESD22-C101E). . . . . . . . . . . . . .1.5kV

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 24 Ld QFN Package (Notes 4, 5) | 44 | 5 |

Maximum Junction Temperature (Plastic Package) . . . . . . . . . . . . +150°C
Power Dissipation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . See Performance Curve
Storage Temperature Range. . . . . . . . . . . . . . . . . . . . . . . . . -40°C to +150°C
Pb-Free Reflow Profile . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . see link below
   http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Operating Conditions

Ambient Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . .-40°C to +85°C
Junction Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . .-40°C to +150°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications $V_{SP} = +14V$, $R_{L-DIFF} = 51\Omega$ differential (emulating transformer input load), Refer to Figure 3, $T_A = +25°C$. Ports tested separately unless otherwise indicated.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNIT |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| AV | | Gain Across the Load, $R_B = 5.1\Omega$ | | 11.6 | | V/V |
| BW | -3dB Bandwidth | $I_S = 14mA/port$, $V_O < 2V_{PP-DIFF}$ | | 110 | | MHz |
| | | $I_S = 10mA/port$, $V_O = 5V_{PP-DIFF}$ | | 70 | | MHz |
| Gain Flatness | Small Signal Gain Flatness | $I_S = 14mA/port$, 17.6MHz | | 0.3 | | dB |
| | | $I_S = 14mA/port$, 30MHz | | 0.9 | | dB |
| SR | Slew Rate | $V_{OUT} = 16V_{P-P-DIFF}$ (20% to 80%) | 560 | 1000 | | V/µs |
| 200kHz Harmonic Distortion | 2nd Harmonic | 10mA/port, $V_{OUT} = 10V_{P-P-DIFF}$ | | -95 | | dBc |
| | 3rd Harmonic | 10mA/port, $V_{OUT} = 10V_{P-P-DIFF}$ | | -83 | | dBc |
| | THD | 10mA/port, $V_{OUT} = 10V_{P-P-DIFF}$ | | -83 | | dBc |
| 4MHz Harmonic Distortion | 2nd Harmonic | 10mA/port, $V_{OUT} = 10V_{P-P-DIFF}$ | | -80 | | dBc |
| | 3rd Harmonic | 10mA/port, $V_{OUT} = 10V_{P-P-DIFF}$ | | -75 | | dBc |
| | THD | 10mA/port, $V_{OUT} = 10V_{P-P-DIFF}$ | | -74 | | dBc |
| MBPR | Average Missing-Band Power Ratio | 26kHz to 8MHz, 5kHz Tone Spacing, $P_{LINE} = 19.5dBm$, VDSL2+ 8b, US1 | | -64 | | dBc |
| $e_O$ | Output Voltage Noise | f = 1MHz, differential each port | | 110 | | nV/$\sqrt{Hz}$ |
| $e_{O-CM}$ | Common Mode Output Noise at each Port Pair | f = 1MHz | | 190 | | nV/$\sqrt{Hz}$ |
| **CONTROL FEATURES** | | | | | | |
| $V_{HIGH}$ | Input High Voltage | SCLK, SDATA, CS, BOOST inputs | 2.3 | | | V |
| $V_{LOW}$ | Input Low Voltage | SCLK, SDATA, CS, BOOST inputs | | | 0.8 | V |
| $I_{HIGH}$ | Input High Current for Pull-up Pins CS, BOOST | $V_{IN} = 3.3V$ | -28 | -23 | -18 | µA |
| $I_{HIGH}$ | Input High Current for Pull-down Pins SCLK, SDATA | $V_{IN} = 3.3V$ | 40 | 50 | 60 | µA |

## Electrical Specifications

$V_{SP}$ = +14V, $R_{L-DIFF}$ = 51$\Omega$ differential (emulating transformer input load), Refer to Figure 3, $T_A$ = +25°C. Ports tested separately unless otherwise indicated.(Continued)

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNIT |
|---|---|---|---|---|---|---|
| $I_{LOW}$ | Input Low Current for Pull-up Pins CS, BOOST | $V_{IN}$ = 0V | -88 | -73 | -58 | µA |
| $I_{LOW}$ | Input Low Current for Pull-down Pins SCLK, SDATA | $V_{IN}$ = 0V | -0.2 | 0 | +0.2 | µA |
| **SUPPLY CHARACTERISTICS** | | | | | | |
| $V_S$ | Operating Supply Voltage | | +10 | +14 | +14.7 | V |
| $V_{CPP}$ | Voltage on the CPP Pin | BOOST = 0V (Class AB) | | 7 | | V |
| $V_{CPSW}$ | Maximum Voltage on the CPSW Pin | BOOST = 0V (Class AB) | | 14 | | V |
| $V_{CMM}$ | Voltage on the CMM Pin | BOOST = 0V (Class AB) | | 7 | | V |
| $V_{CMSW}$ | Minimum Voltage on the CMSW Pin | BOOST = 0V (Class AB) | | 0 | | V |
| $I_{SP}$ | Positive Supply Current per Port | All outputs at 0V, BOOST = 0V, SDATA = 8'h7F for Registers 3 and 7 | 17.5 | 19.5 | 21.5 | mA |
| | | All outputs at 0V, BOOST = 0V, SDATA = 8'h1C for Registers 3 and 7 | 9.8 | 10.3 | 10.8 | mA |
| | | All outputs at 0V, BOOST = 0V, SDATA = 8'h0F for Registers 3 and 7 | 6.8 | 7.2 | 7.6 | mA |
| $I_{SP}$ (Power-down) | Supply Current per Port | All outputs at 0V, BOOST = 0V, SDATA = 8'h80 for Registers 3 and 7 | 2.0 | 2.5 | 3.0 | mA |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ | Loaded Output Swing High (Single-ended to GND) | $R_L$ = 51$\Omega$, Class AB (see Figure 3) | 11.9 | 12.4 | | V |
| | Loaded Output Swing High (Single-ended to GND) | $R_L$ = 51$\Omega$, Class AB (see Figure 3) | | 1.6 | 2.1 | V |
| $I_{OL}$ | Linear Output Current | $R_L$ = 10$\Omega$, f = 100kHz, THD = -60dBc (5$\Omega$ differential) | | ±360 | | mA |
| $V_{OS-DM}$ | Differential Output Offset Voltage | SDATA = 8'h1C | -125 | 18 | +125 | mV |
| $V_{OS-CM}$ | Common Mode Output Offset Voltage | SDATA = 8'h1C (Offset from input VCM) | 6.85 | | 7.09 | mV |
| **INPUT CHARACTERISTICS** | | | | | | |
| CMIR | Common Mode Input Range at each of the 4 Non-inverting Input Pins | Class AB | +4.5 | | +9.5 | V |
| CMRR | DC Common Mode Rejections for each Port. $V_{CM}$ = +4.5V to +9.5V | $V_{CM}$ to Differential Mode Output (Input Referred) $I_{SP}$ = 10mA/port | | 66 | | dB |
| | | $V_{CM}$ to Common Mode Output (Output Referred) $I_{SP}$ = 10mA/port | | 40 | | dB |
| PSRR | DC Power Supply Rejections for each Port to Differential Output (Input Referred) | +$V_S$ = +7V to +14V, GND = 0V, $I_{SP}$ = 10mA/port | | 74 | | dB |
| | DC Power Supply Rejections for each Port to Common Mode Output (Output Referred) | +$V_S$ = +7V to +14V, GND = 0V, $I_{SP}$ = 10mA/port | | 55 | | dB |
| RIN | Input Resistance | Differential | 5.0 | 6.0 | 7.1 | k$\Omega$ |
| **DIGITAL** | | | | | | |
| $f_{CLK}$ | Clock Frequency | | | 0.1 | 10 | MHz |

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

# Typical Performance Curves $V_{CC}$ = +14V, Rb = 5.1$\Omega$, Gain at the Load = 11.6V/V (Differential), $R_{LOAD}$ = 51$\Omega$, $T_A$ = +25°C, Unless otherwise noted.
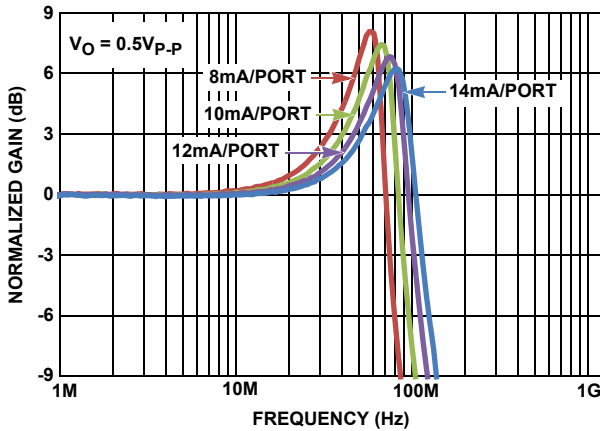


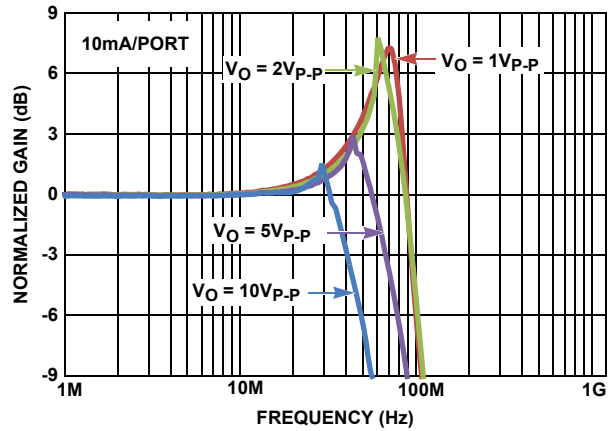FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE vs BIAS CURRENT



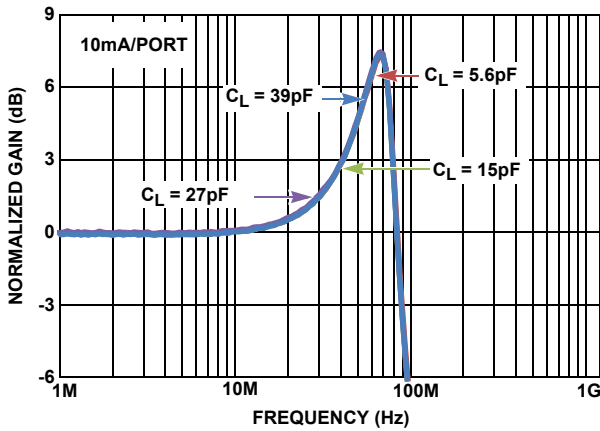FIGURE 5. LARGE SIGNAL FREQUENCY RESPONSE



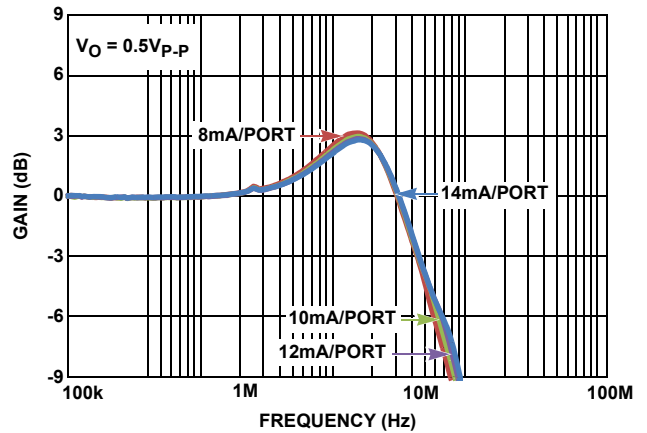FIGURE 6. SMALL SIGNAL FREQUENCY RESPONSE vs $C_{LOAD}$



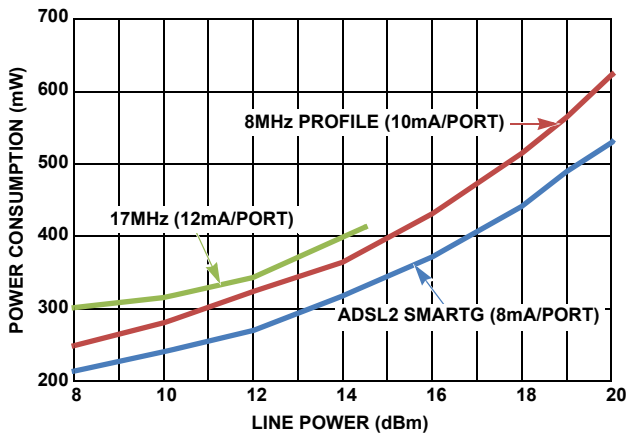FIGURE 7. COMMON MODE SMALL SIGNAL RESPONSE vs BIAS CURRENT
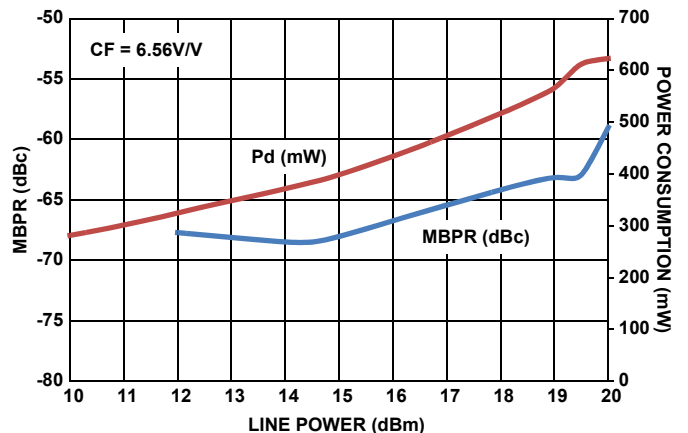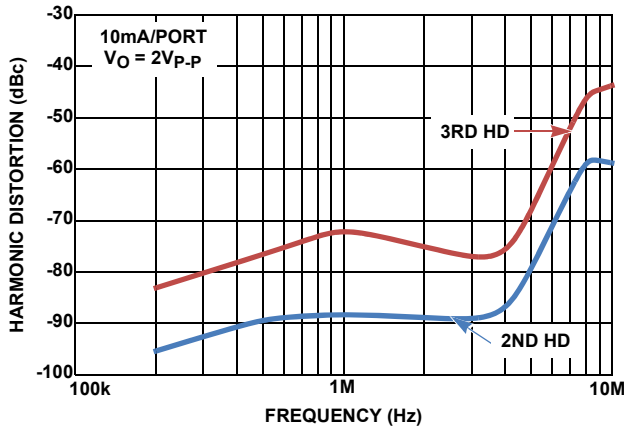


FIGURE 8. POWER CONSUMPTION vs LINE POWER



FIGURE 9. VDSL2+ 8b Avg. MBPR US1 vs LINE POWER

# Typical Performance Curves
$V_{CC}$ = +14V, Rb = 5.1$\Omega$, Gain at the Load = 11.6V/V (Differential), $R_{LOAD}$ = 51$\Omega$, $T_A$ = +25°C, Unless otherwise noted. (Continued)

FIGURE 10. HARMONIC DISTORTION vs FREQUENCY
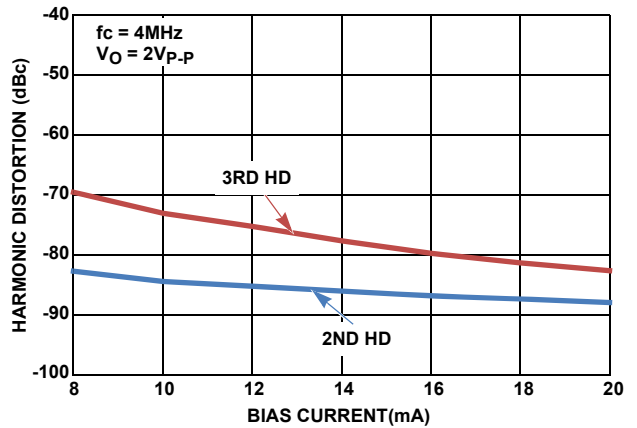
FIGURE 11. HARMONIC DISTORTION vs BIAS CURRENT
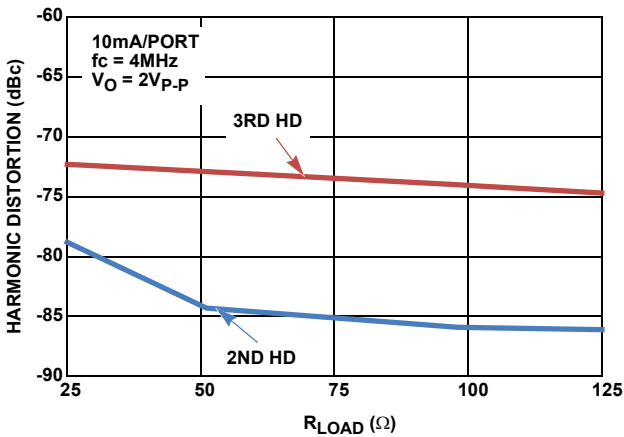
FIGURE 12. HARMONIC vs $R_{LOAD}$
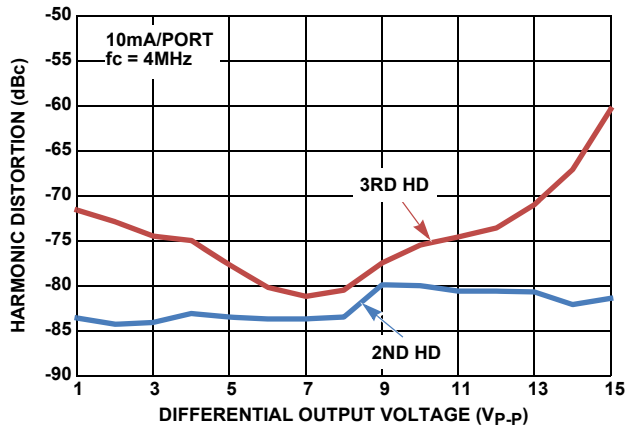
FIGURE 13. HARMONIC DISTORTION vs OUTPUT AMPLITUDE
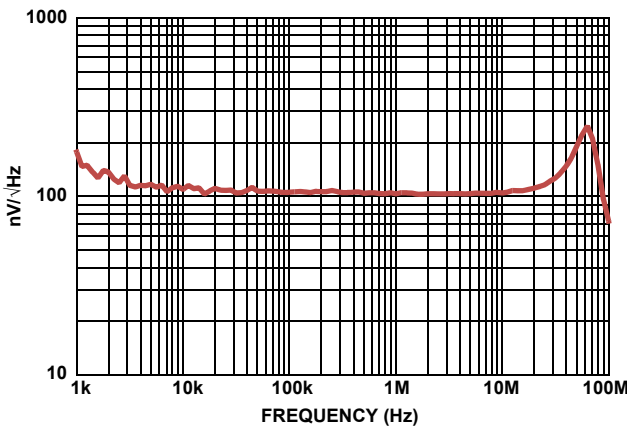
FIGURE 14. DIFFERENTIAL OUTPUT VOLTAGE NOISE
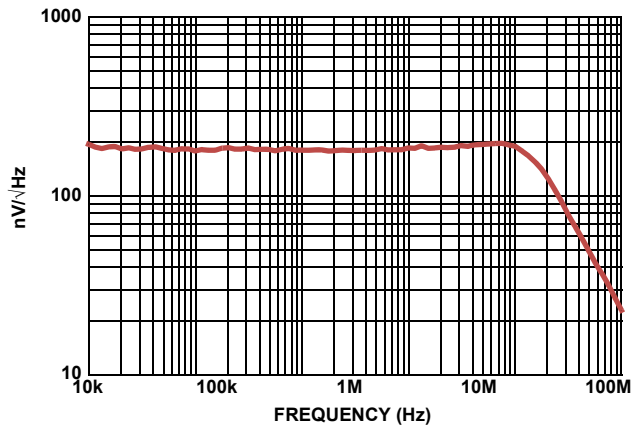
FIGURE 15. COMMON MODE OUTPUT VOLTAGE NOISE

# Typical Performance Curves
$V_{CC}$ = +14V, Rb = 5.1$\Omega$, Gain at the Load = 11.6V/V (Differential), $R_{LOAD}$ = 51$\Omega$, $T_A$ = +25°C, Unless otherwise noted. (Continued)
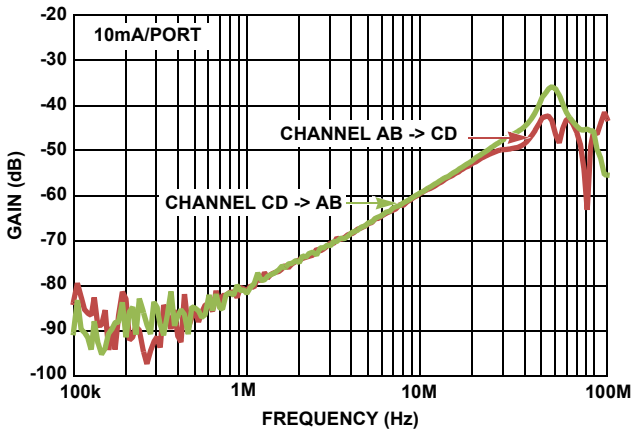


FIGURE 16. CHANNEL-TO-CHANNEL CROSSTALK
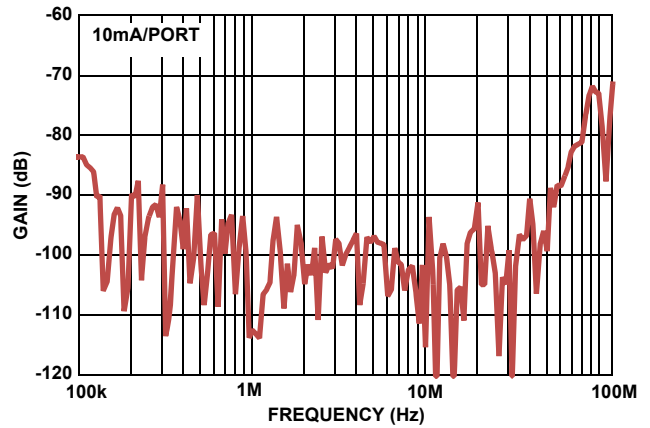


FIGURE 17. OFF-ISOLATION
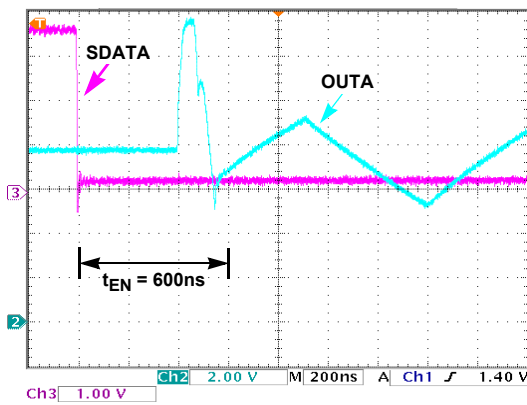


FIGURE 18. ENABLE RESPONSE
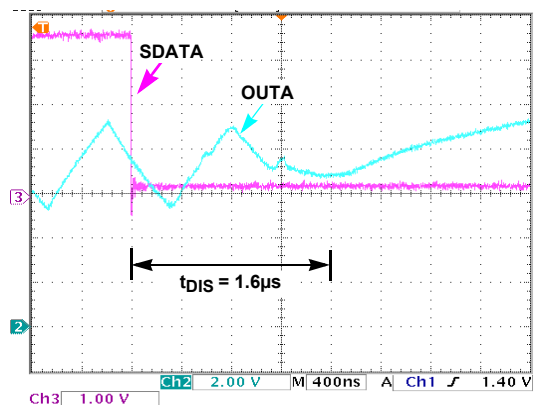


FIGURE 19. DISABLE RESPONSE
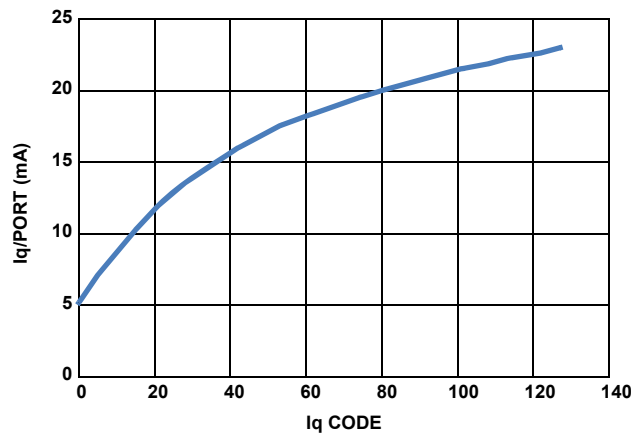


FIGURE 20. QUIESCENT CURRENT PER PORT vs CODES

# Typical Performance Curves
$V_{CC}$ = +14V, Rb = 5.1$\Omega$, Gain at the Load = 11.6V/V (Differential), $R_{LOAD}$ = 51$\Omega$, $T_A$ = +25°C, Unless otherwise noted. (Continued)
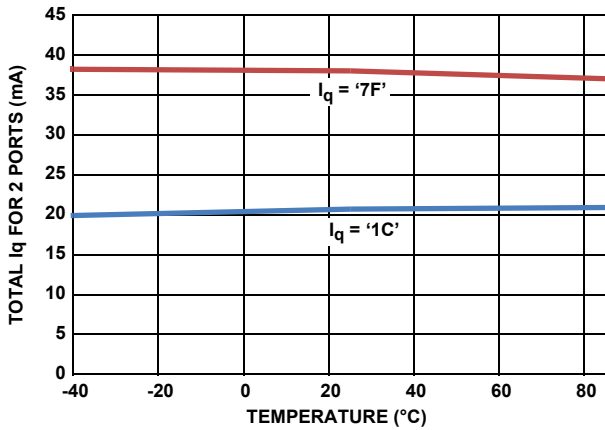


FIGURE 21. QUIESCENT CURRENT vs TEMPERATURE
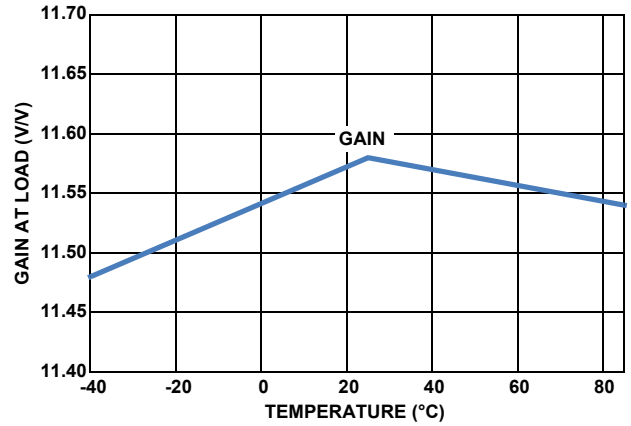


FIGURE 22. GAIN AT LOAD vs TEMPERATURE
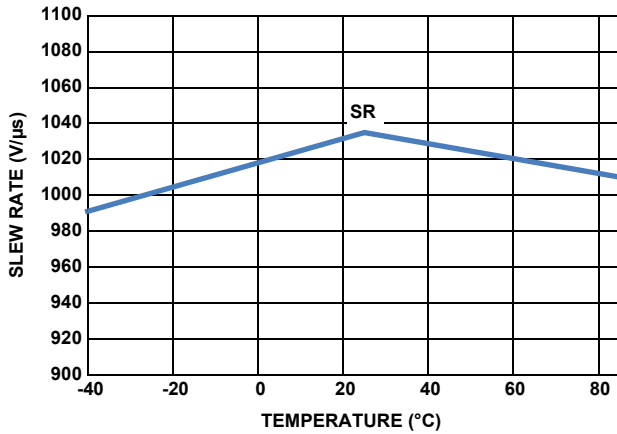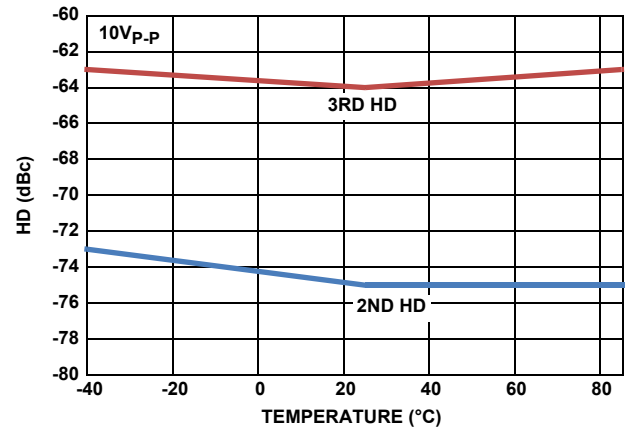


FIGURE 23. SLEW RATE vs TEMPERATURE



FIGURE 24. 4MHz HARMONIC DISTORTION vs TEMPERATURE



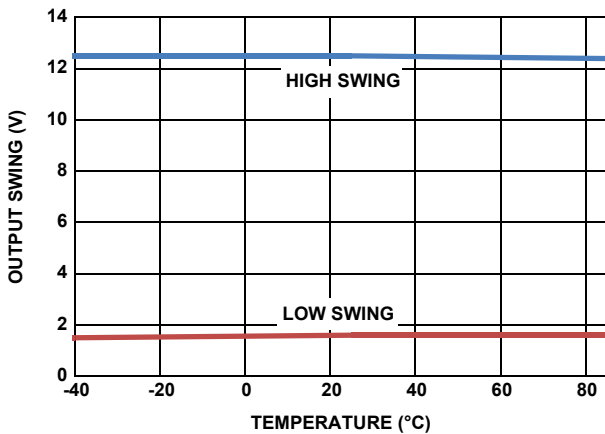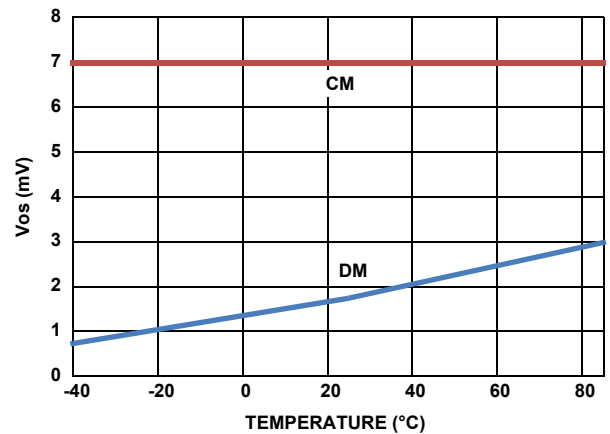FIGURE 25. OUTPUT SWING vs TEMPERATURE



FIGURE 26. OUTPUT OFFSET CM AND DM vs TEMPERATURE

## General Description

The ISL1561 is a class G amplifier designed to reduce power consumption in ADSL2+ and VDSL2 applications compared to class AB. With the high PAR used for xDSL signals, a supply voltage of +14V can be used for the majority of the small amplitude cycles while boosting to a supply voltage of +28V can be used for the few high amplitude cycles.

## Digital Interface

A 12-bit serial port interface is used to program ISL1561. The first bit defines the write (1'b1) and read (1'b0) operation to the register. The following 3-bit calls the registers. The last 8-bit programs the registers. Default start-up for ISL1561 is in disable mode with boost and CS pins having internal pull ups and SCLK and SDATA pins having internal pull downs. ISL1561 can only be programmed through the SPI when CS is set low.

# Register Listing

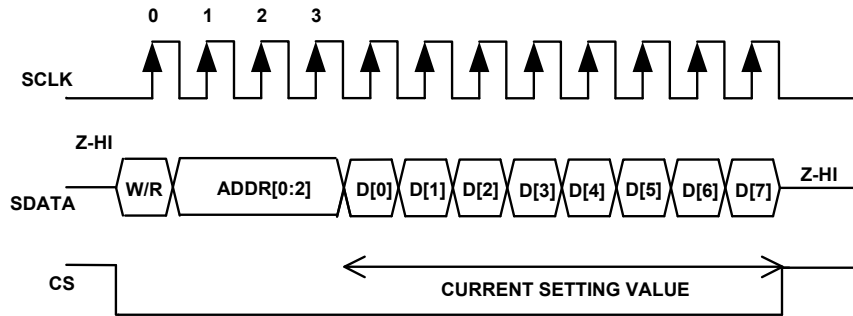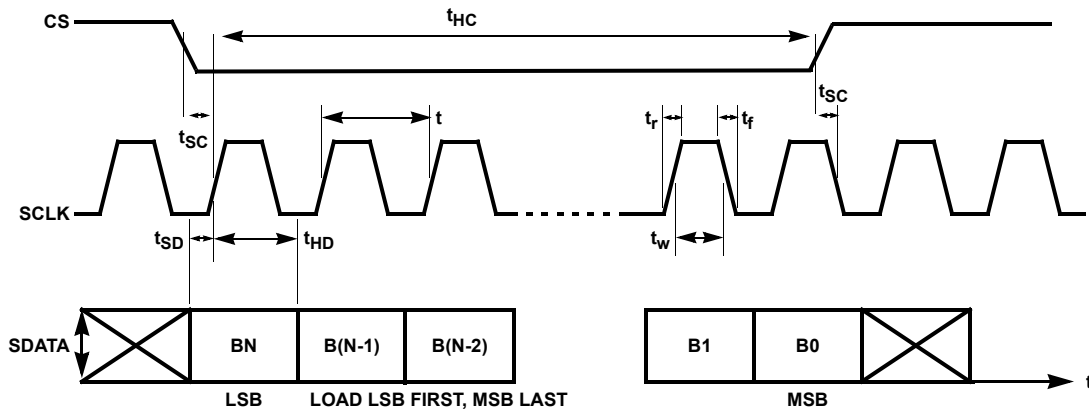| ADDRESS | FUNCTION | BIT | DESCRIPTION |
|---------|----------|-----|-------------|
| 3'h3 | Setting of quiescent current of port AB | [7] | Boost disable |
| | | [6:0] | Program quiescent current of port AB. |
| 3'h7 | Setting of quiescent current of port CD | [7] | Boost disable |
| | | [6:0] | Program quiescent current of port CD. |



FIGURE 27. 12 BITS SERIAL ADDRESSING DIAGRAM



FIGURE 28. 12 BITS SERIAL ADDRESSING DIAGRAM

**TABLE 1. SERIAL TIMING DIAGRAM**

| PARAMETER | RECOMMENDED OPERATING RANGE | DESCRIPTION |
|---|---|---|
| t | ≥100ns | Clock Period |
| $t_r/t_f$ | 0.05*t | Clock Rise/Clock Fall |
| $t_{HC}$ | ≥7ns | Data Hold Time |
| $t_{SD}$ | ≥10ns | Data Setup Time |
| $t_{HC}$ | ≥2.8ns | CS Hold Time |
| $t_{SC}$ | ≥0.5ns | CS Setup Time |
| $t_W$ | 0.50*t | Clock Pulse Width |

## Boost Control

Table 2 summarizes the logic of register MSB on boost operations followed by Figure 29 with the recommended look ahead timing for the boost signal.

**TABLE 2. REGISTER MSB ON BOOST OPERATION**

| Reg3 8'h[7] | Reg7 8'h[7] | BOOST PIN | BOOST OPERATION |
|---|---|---|---|
| 0 | X | 1 | 1 |
| X | 0 | 1 | 1 |
| 1 | 1 | X | 0 |
| X | X | 0 | 0 |

NOTE: X = do not care



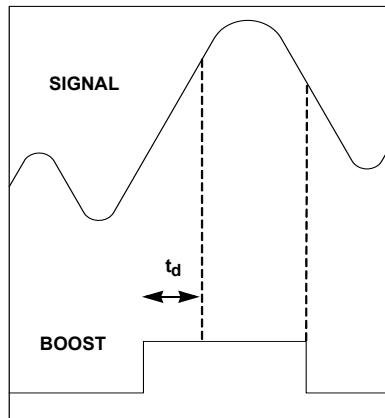**FIGURE 29. SERIAL TIMING DIAGRAM**

**TABLE 3. EXTERNAL BOOST SIGNAL TIMING PARAMETERS**

| PARAMETER | RECOMMENDED OPERATING RANGE | DESCRIPTION |
|---|---|---|
| $t_d$ | 100ns | Look ahead boost |

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| January 24, 2013 | FN7941.1 | Changed MIN/MAX specs for "Differential Output Offset Voltage" on page 5 from -75/75mV to -125/125mV. |
| November 21, 2012 | | Added resistor values to Figure 3 on page 3.<br>Edited table heading for columns 1 and 2 in Table 2 on page 11. |
| October 5, 2012 | FN7941.0 | Initial Release. |

# About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL1561

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

For additional products, see www.intersil.com/en/products.html

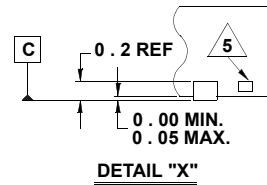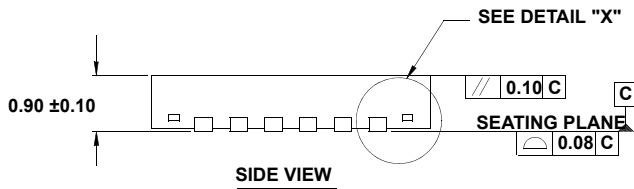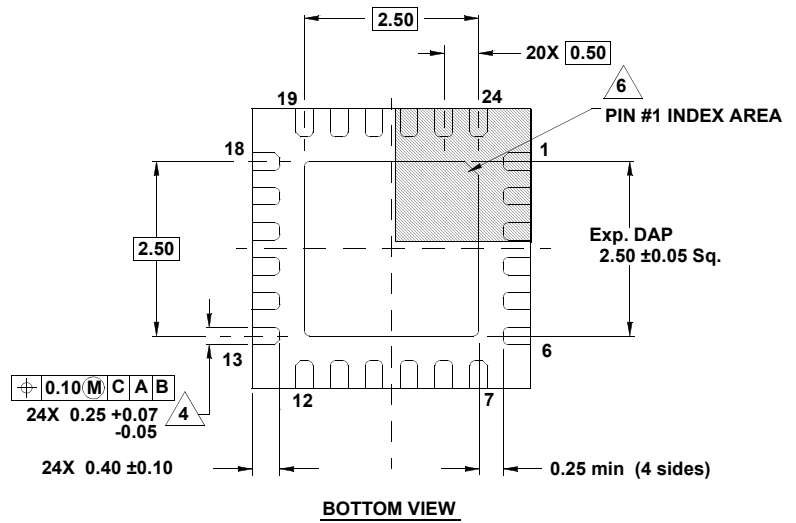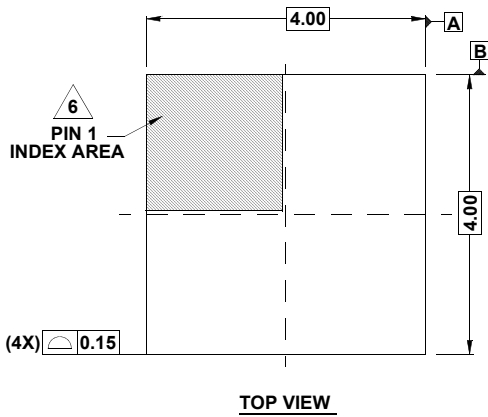For information regarding Intersil Corporation and its products, see www.intersil.com

# Package Outline Drawing

## L24.4x4H
**24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
Rev 0, 09/11

4.00 A

B

6
PIN 1
INDEX AREA

4.00

(4X) ⌒ 0.15

**TOP VIEW**

2.50

20X 0.50

6
PIN #1 INDEX AREA

19    24

18    1

2.50

Exp. DAP
2.50 ±0.05 Sq.

13    6

⊕ 0.10 Ⓜ C A B
24X 0.25 +0.07 -0.05    4

12    7

24X 0.40 ±0.10

0.25 min (4 sides)

**BOTTOM VIEW**

SEE DETAIL "X"

0.90 ±0.10

// 0.10 C    C

SEATING PLANE
⌒ 0.08 C

**SIDE VIEW**

C    0 . 2 REF    5

0 . 00 MIN.
0 . 05 MAX.

**DETAIL "X"**

( 3.80 )

( 2.50)

( 3.80 )

( 20X 0.50)

( 2.50 )

(24X .25)

( 24 X 0.60)

**TYPICAL RECOMMENDED LAND PATTERN**
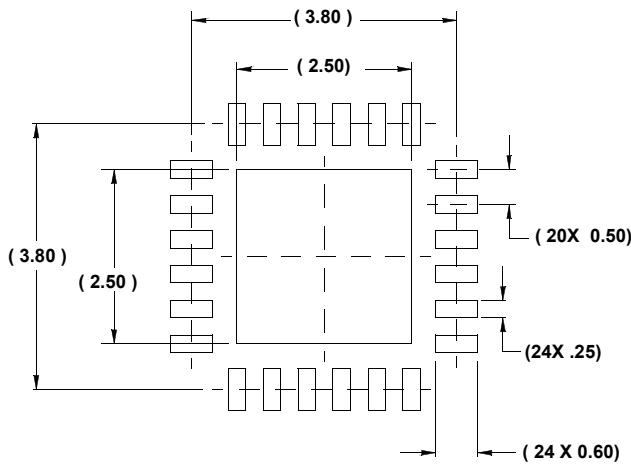
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. Compliant to JEDEC MO-220 VGGD-8

RENESAS