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High speed Serdes PHY macro Datasheet

10Gbps SerDes for TSMC 28nm HPC+

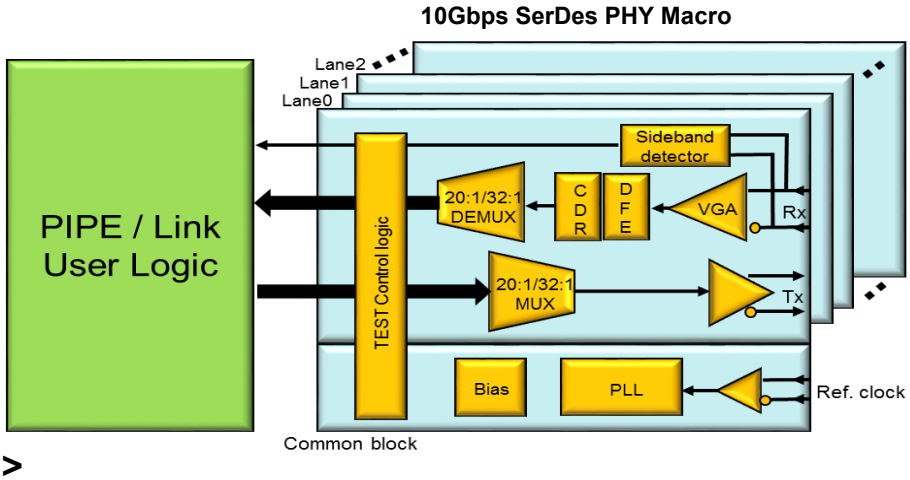
Overview

The Renesas SerDes PHY is useful analog transceiver hard macro for various high speed serial interface PHY layer of TSMC 28nm HPC+ process. This macro can be used as 1.25~10Gbps various high speed interface standards PHY.

Key Features

- Renesas SerDes PHY can be used for analog transceiver of following interface .
  - PCI Express 3.0 / USB3.1 gen2 superspeed / Serial ATA 3.1/ 10GKR / SGMII
- Multi-link support for area reduction in using multiple SerDes
- Technology is TSMC 28nm HPC+ 1p10M (5x2y2r).
- Supply voltage can be applied 0.90V for nominal and 1.0V for overdrive of core voltage, 1.8V for IO voltage.
- 3Tap FIR filter for Tx equalizer / Adaptive 5Tap DFE for Rx equalizer.
- Built-in differential input buffer for clean reference clock.

< Block Diagram >



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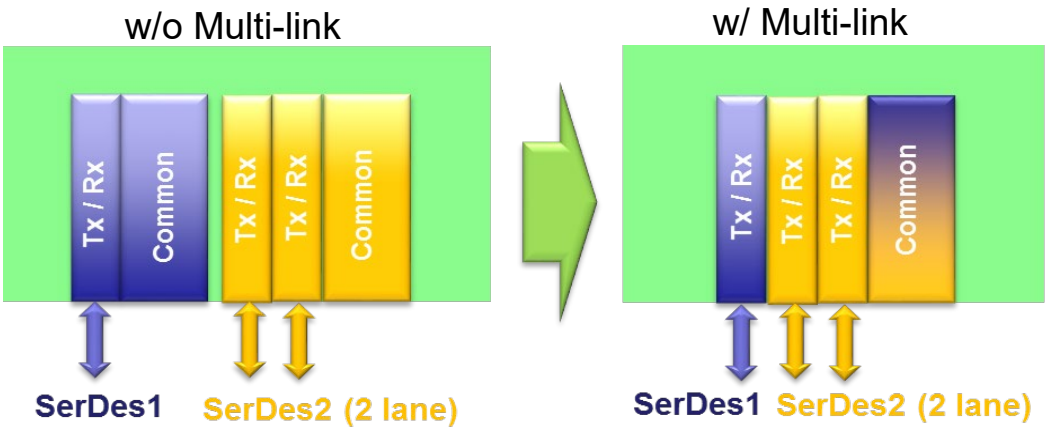

**This IP is contract design IP. Please contact for detail.*

*1 There are some restrictions for use case of these standards. Please contact and consult to Renesas Electronics for detail information before purchasing product.