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PLL Datasheet

Analog-PLL For Fractional Multiplying

Key Features

- Including Loop-filter
- VCO operating range : 2000MHz - 4000 MHz
- Output frequency range : 62.5MHz - 4000 MHz
- Input frequency range : 20MHz - 200 MHz
- Multiplying (Output freq. / PFD freq.) : 1.5625 - 200
- Divider
  7bit feedback divider, 3bit input divider and 3bit output divider
- 14 bit fractional accuracy
- Power-down Mode
- SSC Input is available (recommend triangle profile)

TECHNOLOGY

Process : TSMC 28nm HPC+
Available metallization technologies : 4X2Y2R and 5X2Y2R

OPERATING CONDITION

Parameter		Min	Max	Unit
Operating Voltage (AVDD)		1.62	1.98	V
Operating Voltage (VDD)		0.935	1.08	V
Junction Temperature		-40	125	℃
Input Clock	Duty	30	70	%
	Rise/Fall time	-	0.2	ns

**This IP is contract design IP. Please contact for detail.*

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