1.8V Standard Cell for TSMC 28nm HPC+

Overview

The Renesas 1.8V Standard Cell is useful library for low leak macro of TSMC 28nm HPC+ process. It's suitable for low-speed and low leak macro development.

Key Features

- 1.8VTr-cell is Low Leak very smaller than Core-Cells (5.6pA @2NAND)
- Gate Delay: 20ps@2NAND@Slow Condition
- Technology is TSMC 28nm HPC+.
- Electrical characteristic

Parameter	Min	Typ	Max	Unit
Operating Voltage(VCC)	1.65	1.8	1.95	V
Junction Temperature	-40	25	125	℃

- Cell Lineup

Type	Sub-Type	Cell	Drive	
			X1	X2
Combinational	Simple Logic	BUF	✓	✓
		INV	✓	✓
		2-NAND	✓	
		3-NAND	✓	
		4-NAND	✓	
		2-NOR	✓	
		3-NOR	✓	
		4-NOR	✓	
	Complex Logic	2to1 MUX	✓	
		2-XNOR	✓	
		2-XOR	✓	
Storage	Flip-Flop	D-F/F(with ResetBar)	✓	
		D-F/F(with ResetBar/SetBar)	✓	

**This IP is contract design IP. Please contact for detail.*